

## CMOS Presettable Up/Down Counter

Binary or BCD-Decade

High-Voltage Types (20-Volt Rating)

■ CD4029B consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single **CLOCK**, **CARRY-IN (CLOCK ENABLE)**, **BINARY/DECADE**, **UP/DOWN**, **PRESET ENABLE**, and four individual **JAM** signals. **Q1**, **Q2**, **Q3**, **Q4** and a **CARRY OUT** signal are provided as outputs.

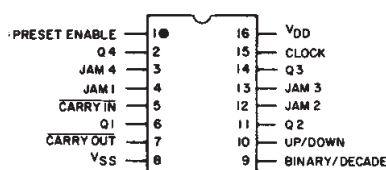
A high **PRESET ENABLE** signal allows information on the **JAM INPUTS** to preset the counter to any state asynchronously with the clock. A low on each **JAM** line, when the **PRESET-ENABLE** signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the **CARRY-IN** and **PRESET ENABLE** signals are low. Advancement is inhibited when the **CARRY-IN** or **PRESET ENABLE** signals are high. The **CARRY-OUT** signal is normally high and goes low when the counter reaches its maximum count in the **UP** mode or the minimum count in the **DOWN** mode provided the **CARRY-IN** signal is low. The **CARRY-IN** signal in the low state can thus be considered a **CLOCK ENABLE**. The **CARRY-IN** terminal must be connected to **V<sub>SS</sub>** when not in use.

Binary counting is accomplished when the **BINARY/DECADE** input is high; the counter counts in the decade mode when the **BINARY/DECADE** input is low. The counter counts up when the **UP/DOWN** input is high, and down when the **UP/DOWN** input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Fig. 17.

Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

The CD4029B-series types are supplied in 16-lead ceramic dual-in-line plastic packages (E suffix), and in chip form (H suffix).

CD4029B Terminal Diagram



92CS-24472R1

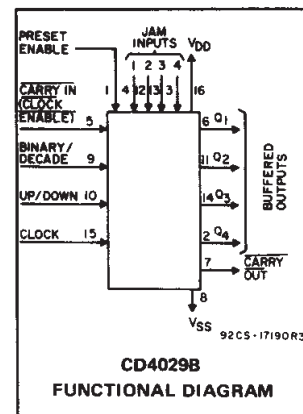
# CD4029B Types

### Features:

- Medium-speed operation . . . 8 MHz (typ.)  
@  $C_L = 50$  pF and  $V_{DD} - V_{SS} = 10$  V
- Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- "Preset Enable" and individual "Jam" inputs provided
- Binary or decade up/down counting
- BCD outputs in decade mode
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of  $1 \mu A$  at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range)  
1 V at  $V_{DD} = 5$  V  
2 V at  $V_{DD} = 10$  V  
2.5 V at  $V_{DD} = 15$  V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Programmable binary and decade counting/frequency synthesizers-BCD output
- Analog to digital and digital to analog conversion
- Up/Down binary counting
- Magnitude and sign generation
- Up/Down decade counting
- Difference counting



**RECOMMENDED OPERATING CONDITIONS** at  $T_A = 25^\circ C$ , Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC                                                    | $V_{DD}$<br>(V) | LIMITS |      | UNITS   |
|-------------------------------------------------------------------|-----------------|--------|------|---------|
|                                                                   |                 | Min.   | Max. |         |
| Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) | —               | 3      | 18   | V       |
| Setup Time $t_{SU}$ :<br>Carry-In                                 | 5               | 200    | —    | ns      |
|                                                                   | 10              | 70     | —    |         |
|                                                                   | 15              | 60     | —    |         |
| U/D or B/D                                                        | 5               | 340    | —    |         |
|                                                                   | 10              | 140    | —    |         |
|                                                                   | 15              | 100    | —    |         |
| Clock Pulse Width, $t_W$                                          | 5               | 180    | —    |         |
|                                                                   | 10              | 90     | —    |         |
|                                                                   | 15              | 60     | —    |         |
| Preset Enable Pulse Width, $t_W$                                  | 5               | 130    | —    |         |
|                                                                   | 10              | 70     | —    |         |
|                                                                   | 15              | 50     | —    |         |
| Clock Input Frequency, $f_{CL}$                                   | 5               | —      | 2    | MHz     |
|                                                                   | 10              | —      | 4    |         |
|                                                                   | 15              | —      | 5.5  |         |
| Clock Rise and Fall Time, $t_{rCL}$ , $t_{fCL}$                   | 5               | —      | —    | $\mu s$ |
|                                                                   | 10              | —      | 15   |         |
|                                                                   | 15              | —      | —    |         |

## CD4029B Types

### MAXIMUM RATINGS, Absolute-Maximum Values:

|                                                                                           |                                                    |
|-------------------------------------------------------------------------------------------|----------------------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )                                                     | ..... -0.5V to +20V                                |
| Voltages referenced to $V_{SS}$ Terminal)                                                 |                                                    |
| INPUT VOLTAGE RANGE, ALL INPUTS                                                           | ..... -0.5V to $V_{DD} + 0.5V$                     |
| DC INPUT CURRENT, ANY ONE INPUT                                                           | ..... $\pm 10\text{mA}$                            |
| POWER DISSIPATION PER PACKAGE ( $P_D$ ):                                                  |                                                    |
| For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ .....                               | 500mW                                              |
| For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ .....                              | Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR                                                  |                                                    |
| FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ .....               | 100mW                                              |
| OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....                                               | $-55^\circ\text{C}$ to $+125^\circ\text{C}$        |
| STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) .....                                             | $-65^\circ\text{C}$ to $+150^\circ\text{C}$        |
| LEAD TEMPERATURE (DURING SOLDERING):                                                      |                                                    |
| At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79\text{mm}$ ) from case for 10s max ..... | $+265^\circ\text{C}$                               |

### STATIC ELECTRICAL CHARACTERISTICS

| CHARAC-<br>TERISTIC                                         | CONDITIONS            |                        |                        | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|-------------------------------------------------------------|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|                                                             | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>DD</sub><br>(V) | -55                                   | -40   | +85   | +125  | +25   |                   |      |       |
|                                                             |                       |                        |                        |                                       |       |       |       | Min.  | Typ.              | Max. |       |
| Quiescent<br>Device<br>Current,<br>I <sub>DD</sub> Max.     | —                     | 0,5                    | 5                      | 5                                     | 5     | 150   | 150   | —     | 0.04              | 5    | μA    |
|                                                             | —                     | 0,10                   | 10                     | 10                                    | 10    | 300   | 300   | —     | 0.04              | 10   |       |
|                                                             | —                     | 0,15                   | 15                     | 20                                    | 20    | 600   | 600   | —     | 0.04              | 20   |       |
|                                                             | —                     | 0,20                   | 20                     | 100                                   | 100   | 3000  | 3000  | —     | 0.08              | 100  |       |
| Output Low<br>(Sink) Current<br>I <sub>OL</sub> Min.        | 0.4                   | 0,5                    | 5                      | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | —    | mA    |
|                                                             | 0.5                   | 0,10                   | 10                     | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | —    |       |
|                                                             | 1.5                   | 0,15                   | 15                     | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | —    |       |
| Output High<br>(Source)<br>Current,<br>I <sub>OH</sub> Min. | 4.6                   | 0,5                    | 5                      | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | —    | mA    |
|                                                             | 2.5                   | 0,5                    | 5                      | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | —    |       |
|                                                             | 9.5                   | 0,10                   | 10                     | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | —    |       |
|                                                             | 13.5                  | 0,15                   | 15                     | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              | —    |       |
| Output Voltage:<br>Low-Level,<br>V <sub>OL</sub> Max.       | —                     | 0,5                    | 5                      | 0.05                                  |       |       |       | —     | 0                 | 0.05 | V     |
|                                                             | —                     | 0,10                   | 10                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
|                                                             | —                     | 0,15                   | 15                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
| Output<br>Voltage:<br>High-Level,<br>V <sub>OH</sub> Min.   | —                     | 0,5                    | 5                      | 4.95                                  |       |       |       | 4.95  | 5                 | —    | V     |
|                                                             | —                     | 0,10                   | 10                     | 9.95                                  |       |       |       | 9.95  | 10                | —    |       |
|                                                             | —                     | 0,15                   | 15                     | 14.95                                 |       |       |       | 14.95 | 15                | —    |       |
| Input Low<br>Voltage<br>V <sub>IL</sub> Max.                | 0.5,4.5               | —                      | 5                      | 1.5                                   |       |       |       | —     | —                 | 1.5  | V     |
|                                                             | 1,9                   | —                      | 10                     | 3                                     |       |       |       | —     | —                 | 3    |       |
|                                                             | 1.5,13.5              | —                      | 15                     | 4                                     |       |       |       | —     | —                 | 4    |       |
| Input High<br>Voltage,<br>V <sub>IH</sub> Min.              | 0.5,4.5               | —                      | 5                      | 3.5                                   |       |       |       | 3.5   | —                 | —    | V     |
|                                                             | 1,9                   | —                      | 10                     | 7                                     |       |       |       | 7     | —                 | —    |       |
|                                                             | 1.5,13.5              | —                      | 15                     | 11                                    |       |       |       | 11    | —                 | —    |       |
| Input Current<br>I <sub>IN</sub> Max.                       | —                     | 0,18                   | 18                     | ±0.1                                  | ±0.1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0.1 | μA    |

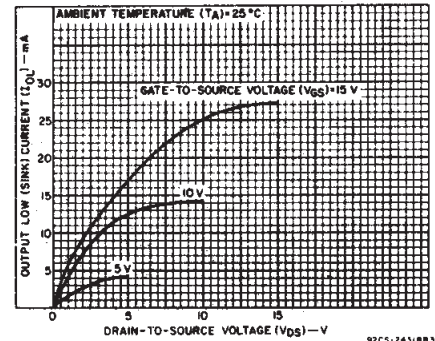


Fig. 1 - Typical output low (sink) current characteristics.

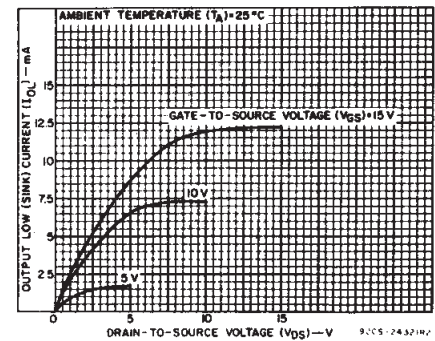


Fig. 2 - Minimum output low (sink) current characteristics.

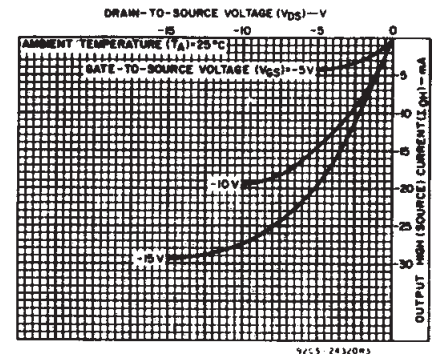


Fig. 3 - Typical output high (source) current characteristics.

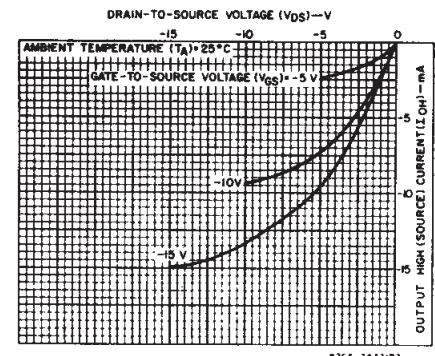


Fig. 4 - Minimum output high (source) current characteristics.

# CD4029B Types

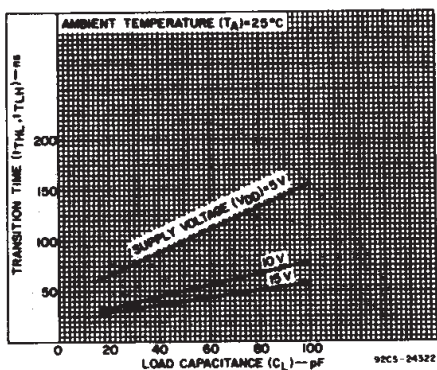


Fig. 5 - Typical transition time as a function of load capacitance.

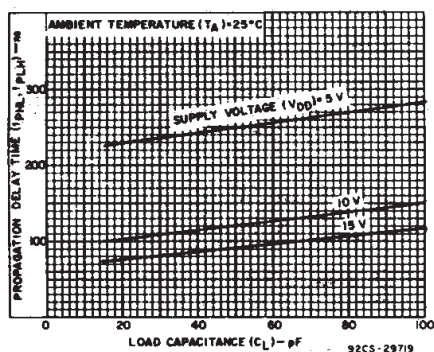


Fig. 6 - Typical propagation delay times as a function of load capacitance (Q output).

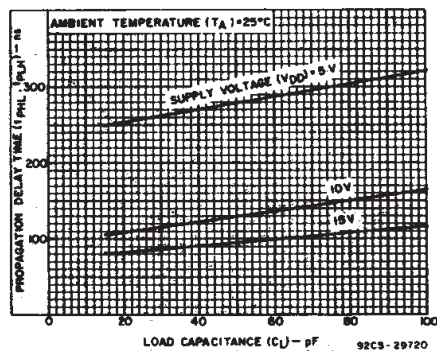


Fig. 7 - Typical propagation delay time as a function of load capacitance (carry output).

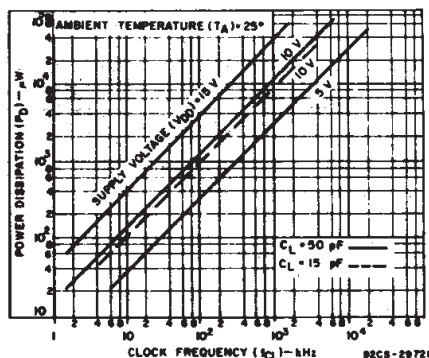


Fig. 8 - Typical power dissipation as a function of frequency.

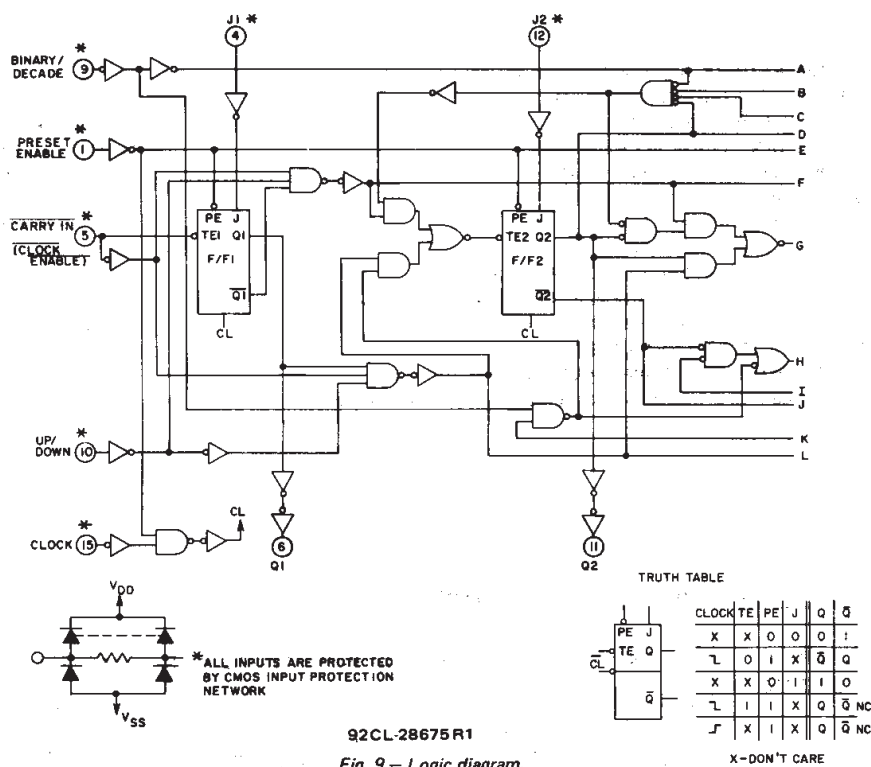


Fig. 9 - Logic diagram.

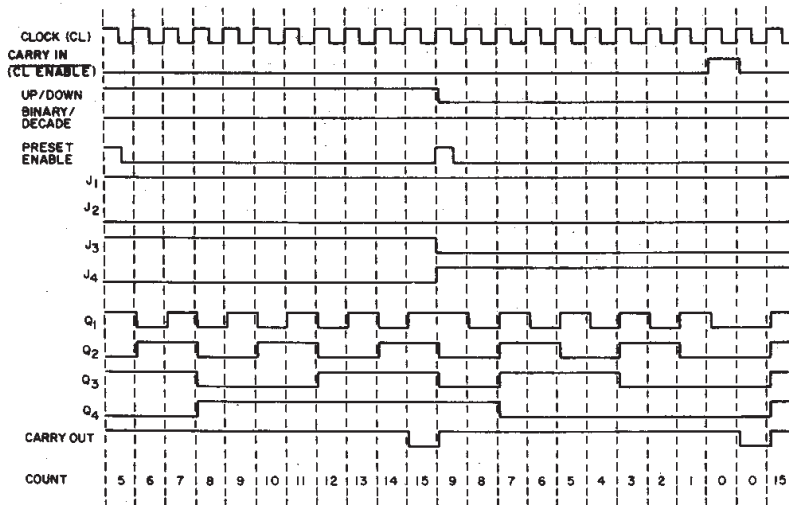
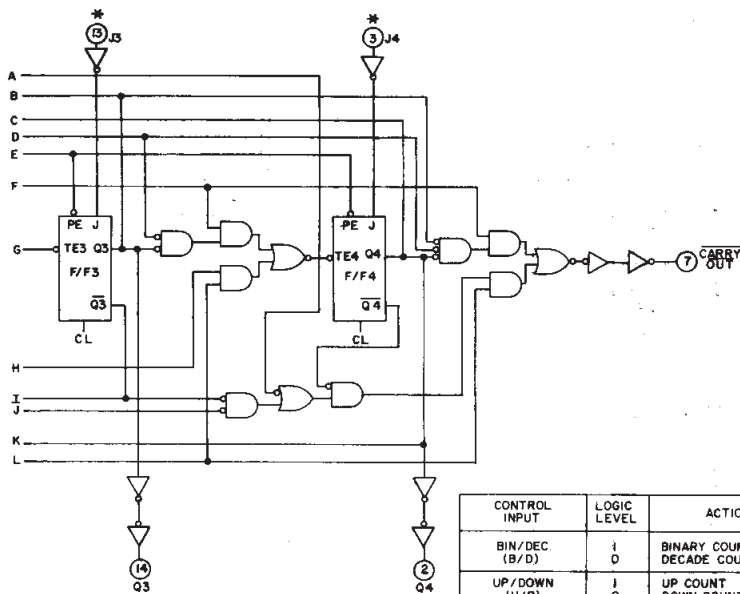


Fig. 10 - Timing diagram-binary mode.

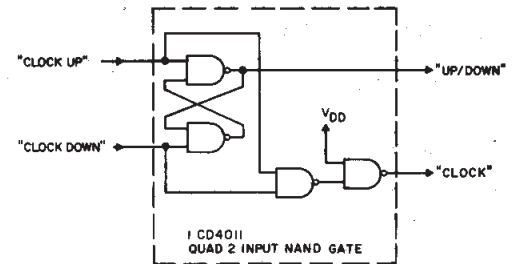
## CD4029B Types



| CONTROL INPUT                   | LOGIC LEVEL | ACTION                                                                                              |
|---------------------------------|-------------|-----------------------------------------------------------------------------------------------------|
| BIN/DEC. (B/D)                  | 1<br>0      | BINARY COUNT<br>DECADE COUNT                                                                        |
| UP/DOWN (U/D)                   | 1<br>0      | UP COUNT<br>DOWN COUNT                                                                              |
| PRESET ENABLE (PE)              | 1<br>0      | JAM IN<br>NO JAM                                                                                    |
| CARRY IN (CT)<br>(CLOCK ENABLE) | 1<br>0      | NO COUNTER<br>ADVANCE AT POS.<br>CLOCK TRANSITION<br>ADVANCE COUNTER<br>AT POS. CLOCK<br>TRANSITION |

92CL-26675-01

Fig. 9 – Logic diagram (cont'd).

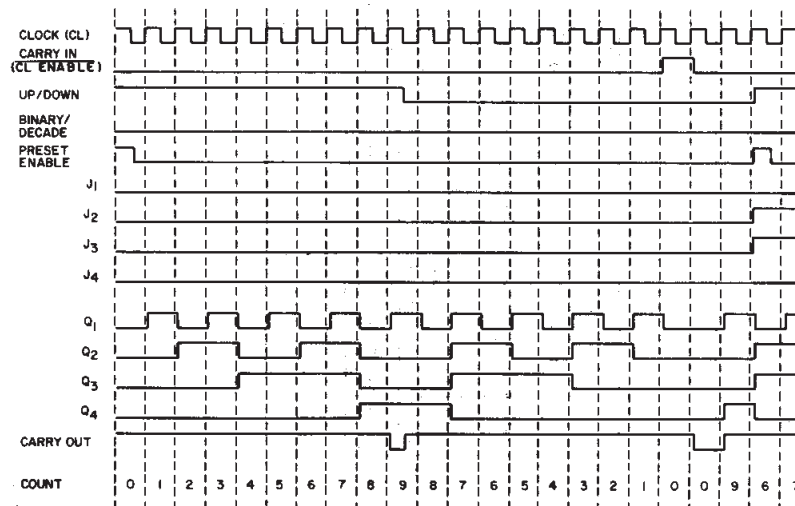


92CS-17195R2

Fig. 11 – Conversion of clock up, clock down input signals to clock and up/down input signals.

The CD4029B CLOCK and UP/DOWN inputs are used directly in most applications. In applications where CLOCK UP and CLOCK DOWN inputs are provided, conversion to the CD4029B CLOCK and UP/DOWN inputs can easily be realized by use of the circuit in Fig. 11.

CD4029B changes count on positive transitions of CLOCK UP or CLOCK DOWN inputs. For the gate configuration shown below, when counting up the CLOCK DOWN input must be maintained high and conversely when counting down the CLOCK UP input must be maintained high.



92CM-17193R3

Fig. 12 – Timing diagram-decade mode.

## CD4029B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20\text{ ns}$ ,  
 $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC                                                              | TEST CONDITIONS | LIMITS              |      |      | UNITS |      |
|-----------------------------------------------------------------------------|-----------------|---------------------|------|------|-------|------|
|                                                                             |                 | V <sub>DD</sub> (V) | Min. | Typ. |       | Max. |
| Clocked Operation                                                           |                 |                     |      |      |       |      |
| Propagation Delay Time: t <sub>PHL</sub> , t <sub>PLH</sub><br>Q Output     | Any Input       | 5                   | —    | 250  | 500   | ns   |
| Carry Output                                                                |                 | 10                  | —    | 120  | 240   |      |
|                                                                             |                 | 15                  | —    | 90   | 180   |      |
|                                                                             |                 | 5                   | —    | 280  | 560   |      |
| Transition Time:<br>Q Outputs, Carry Output                                 |                 | 10                  | —    | 130  | 260   |      |
|                                                                             |                 | 15                  | —    | 95   | 190   |      |
|                                                                             |                 | 5                   | —    | 100  | 200   |      |
| Minimum Clock Pulse Width, t <sub>W</sub>                                   |                 | 10                  | —    | 50   | 100   |      |
|                                                                             |                 | 15                  | —    | 40   | 80    |      |
|                                                                             |                 | 5                   | —    | 90   | 180   |      |
| Clock Rise & Fall Time, t <sub>rCL</sub> , t <sub>fCL</sub> **              |                 | 10                  | —    | 45   | 90    |      |
|                                                                             |                 | 15                  | —    | 30   | 60    |      |
|                                                                             |                 | 5                   | —    | —    | 15    |      |
| Minimum Setup Times, t <sub>S</sub> *<br>B/D or U/D                         |                 | 10                  | —    | —    | 15    |      |
|                                                                             |                 | 15                  | —    | —    | 15    |      |
|                                                                             |                 | 5                   | —    | 170  | 340   |      |
| Maximum Clock Input Frequency, f <sub>CL</sub>                              |                 | 10                  | —    | 70   | 140   |      |
|                                                                             |                 | 15                  | —    | 50   | 100   |      |
|                                                                             |                 | 5                   | 2    | 4    | —     |      |
| Input Capacitance, C <sub>IN</sub>                                          |                 | 10                  | 4    | 8    | —     |      |
|                                                                             |                 | 15                  | 5.5  | 11   | —     |      |
|                                                                             | Any Input       | —                   | 5    | 7.5  | pF    |      |
| Preset Enable                                                               |                 |                     |      |      |       |      |
| Propagation Delay Time: t <sub>PHL</sub> , t <sub>PLH</sub><br>Q Outputs    | Any Input       | 5                   | —    | 235  | 470   | ns   |
| Carry Output                                                                |                 | 10                  | —    | 100  | 200   |      |
|                                                                             |                 | 15                  | —    | 80   | 160   |      |
|                                                                             |                 | 5                   | —    | 320  | 640   |      |
| Minimum Preset Enable Pulse Width, t <sub>W</sub>                           |                 | 10                  | —    | 145  | 290   |      |
|                                                                             |                 | 15                  | —    | 105  | 210   |      |
|                                                                             |                 | 5                   | —    | 65   | 130   |      |
| Minimum Preset Enable Removal<br>Time, t <sub>rem</sub> *                   |                 | 10                  | —    | 35   | 70    |      |
|                                                                             |                 | 15                  | —    | 25   | 50    |      |
|                                                                             |                 | 5                   | —    | 100  | 200   |      |
| Carry Input                                                                 |                 | 10                  | —    | 55   | 110   |      |
|                                                                             |                 | 15                  | —    | 40   | 80    |      |
|                                                                             |                 | Carry Input         |      |      |       |      |
| Propagation Delay Time: t <sub>PHL</sub> , t <sub>PLH</sub><br>Carry Output | Any Input       | 5                   | —    | 170  | 340   | ns   |
| Min. HOLD Time<br>t <sub>H</sub> *** Carry In                               |                 | 10                  | —    | 70   | 140   |      |
|                                                                             |                 | 15                  | —    | 50   | 100   |      |
|                                                                             |                 | 5                   | —    | 25   | 50    |      |
| Min Set-Up Time<br>t <sub>S</sub> *** Carry In                              |                 | 10                  | —    | 15   | 30    |      |
|                                                                             |                 | 15                  | —    | 12   | 25    |      |
|                                                                             |                 | 5                   | —    | 100  | 200   |      |
|                                                                             |                 | 10                  | —    | 35   | 70    |      |
|                                                                             |                 | 15                  | —    | 30   | 60    |      |

\* From Up/Down, Binary/Decode, Carry In, or Preset Enable Control Inputs to Clock Edge.

\*\* If more than one unit is cascaded in the parallel clocked application,  $t_{rCL}$  should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load. This measurement was made with a decoupling capacitor ( $>1\text{ }\mu\text{F}$ ) between  $V_{DD}$  and  $V_{SS}$ .

\*\*\*From Carry In to Clock Edge

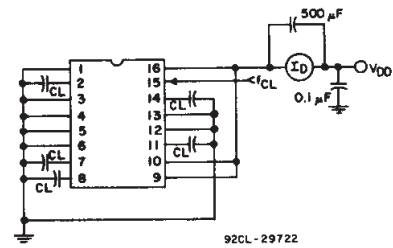


Fig. 13 — Power dissipation test circuit.

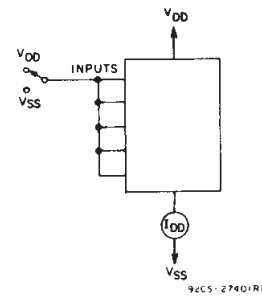


Fig. 14 — Quiescent device current test circuit.

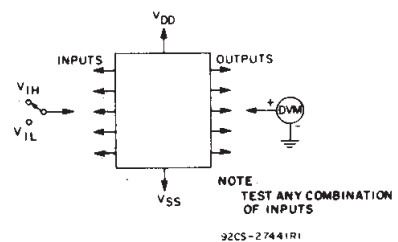


Fig. 15 — Input voltage test circuit.

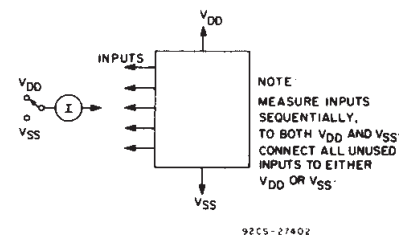
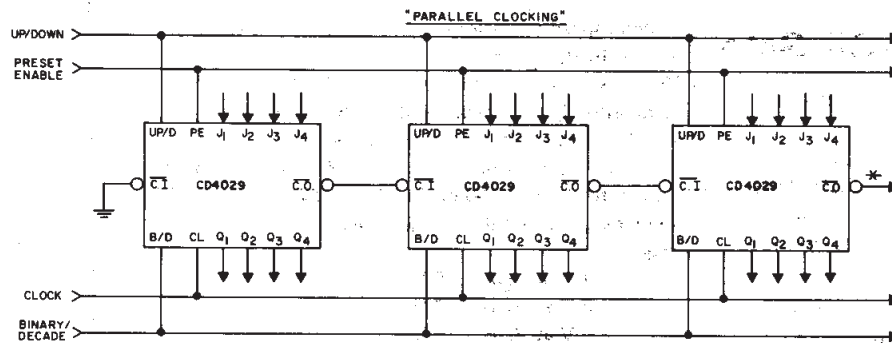
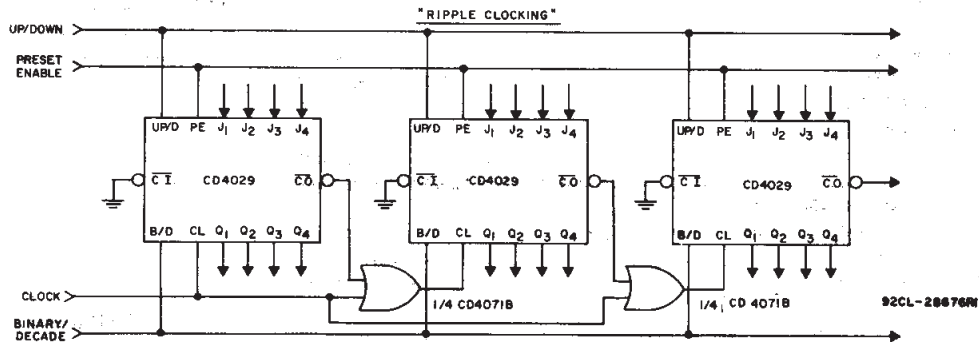


Fig. 16 — Input current test circuit.

## CD4029B Types



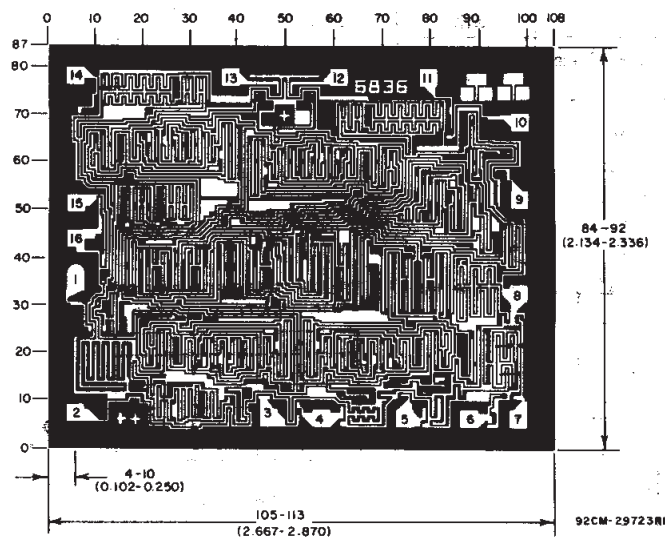
\* CARRY OUT lines at the 2nd, 3rd, etc., stages may have a negative-going glitch pulse resulting from differential delays of different CD4029B IC's. These negative-going glitches do not affect proper CD4029B operation. However, if the CARRY OUT signals are used to trigger other edge-sensitive logic devices, such as FF's or counters, the CARRY OUT signals should be gated with the clock signal using a 2-input OR gate such as CD4071B.



### Ripple Clocking Mode:

The Up/Down control can be changed at any count. The only restriction on changing the Up/Down control is that the clock input to the first counting stage must be high. For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages, and  $\overline{C.O.}$  is connected directly to the CL input of the next stage with  $\overline{C.I.}$  grounded.

Fig. 17 — Cascading counter packages.



### Chip dimensions and pad layout for CD4029B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

## **IMPORTANT NOTICE**

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