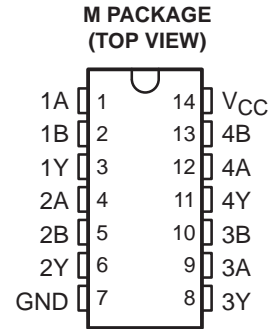


CD74ACT32-Q1 QUADRUPLE 2-INPUT POSITIVE-OR GATE

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- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Inputs Are TTL-Voltage Compatible
- Buffered Inputs
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ±24-mA Output Drive Current
– Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design



† Contact factory for details. Q100 qualification data available on request.

description/ordering information

The CD74ACT32 is a quadruple 2-input positive-OR gate. This device performs the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = A + B$ in positive logic.

ORDERING INFORMATION

T _A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Tape and reel	CD74ACT32QM96Q1	ACT32Q

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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CD74ACT32-Q1

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 2)	86°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	$T_A = 25^\circ\text{C}$		-40°C to 125°C		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	V
V_O Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		-24		-24	mA
I_{OL} Low-level output current		24		24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		10		10	ns/V

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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QUADRUPLE 2-INPUT POSITIVE-OR GATE

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		–40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –50 μA	4.5 V	4.4	4.4	V	
		I _{OH} = –24 mA	4.5 V	3.94	3.7		
		I _{OH} = –50 mA [†]	5.5 V		3.85		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 50 μA	4.5 V	0.1	0.1	V	
		I _{OL} = 24 mA	4.5 V	0.36	0.5		
		I _{OL} = 50 mA [†]	5.5 V		1.65		
I _I	V _I = V _{CC} or GND	5.5 V	±0.1	±1	μA		
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	4	80	μA		
ΔI _{CC} [‡]	V _I = V _{CC} – 2.1 V	4.5 V to 5.5 V	2.4	3	mA		
C _i			10	10	pF		

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75-Ω transmission-line drive capability at 125°C.

[‡] Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

ACT INPUT LOAD TABLE

INPUT	UNIT LOAD
All	0.42

Unit load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 125°C		UNIT
			MIN	MAX	
t _{PLH}	A or B	Y	3	12.1	ns
t _{PHL}			3	12.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TYP	UNIT
C _{pd} Power dissipation capacitance	47	pF

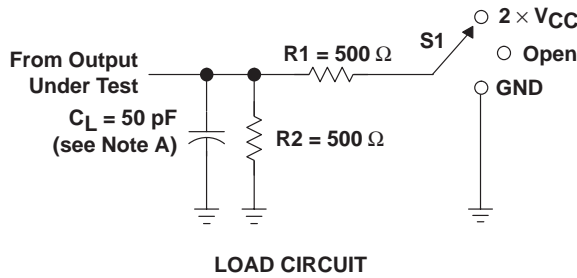


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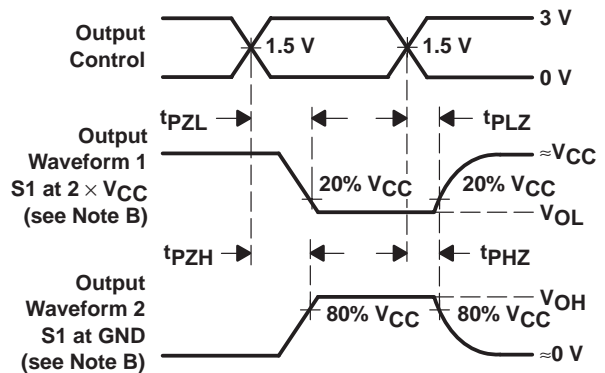
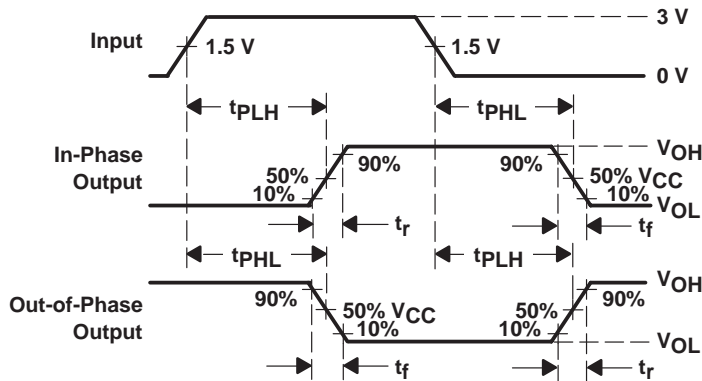
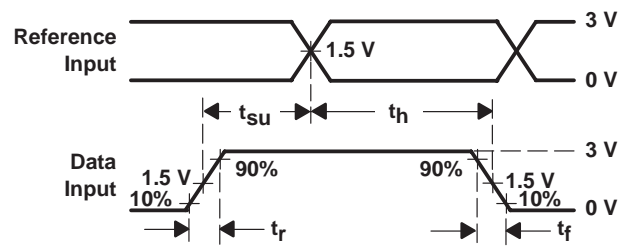
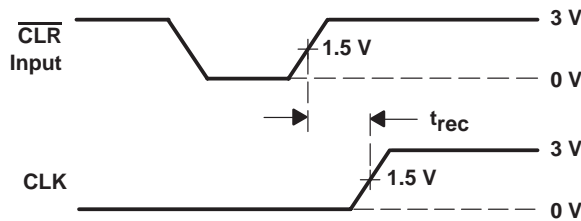
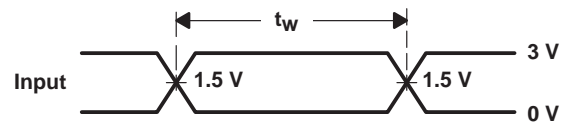
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

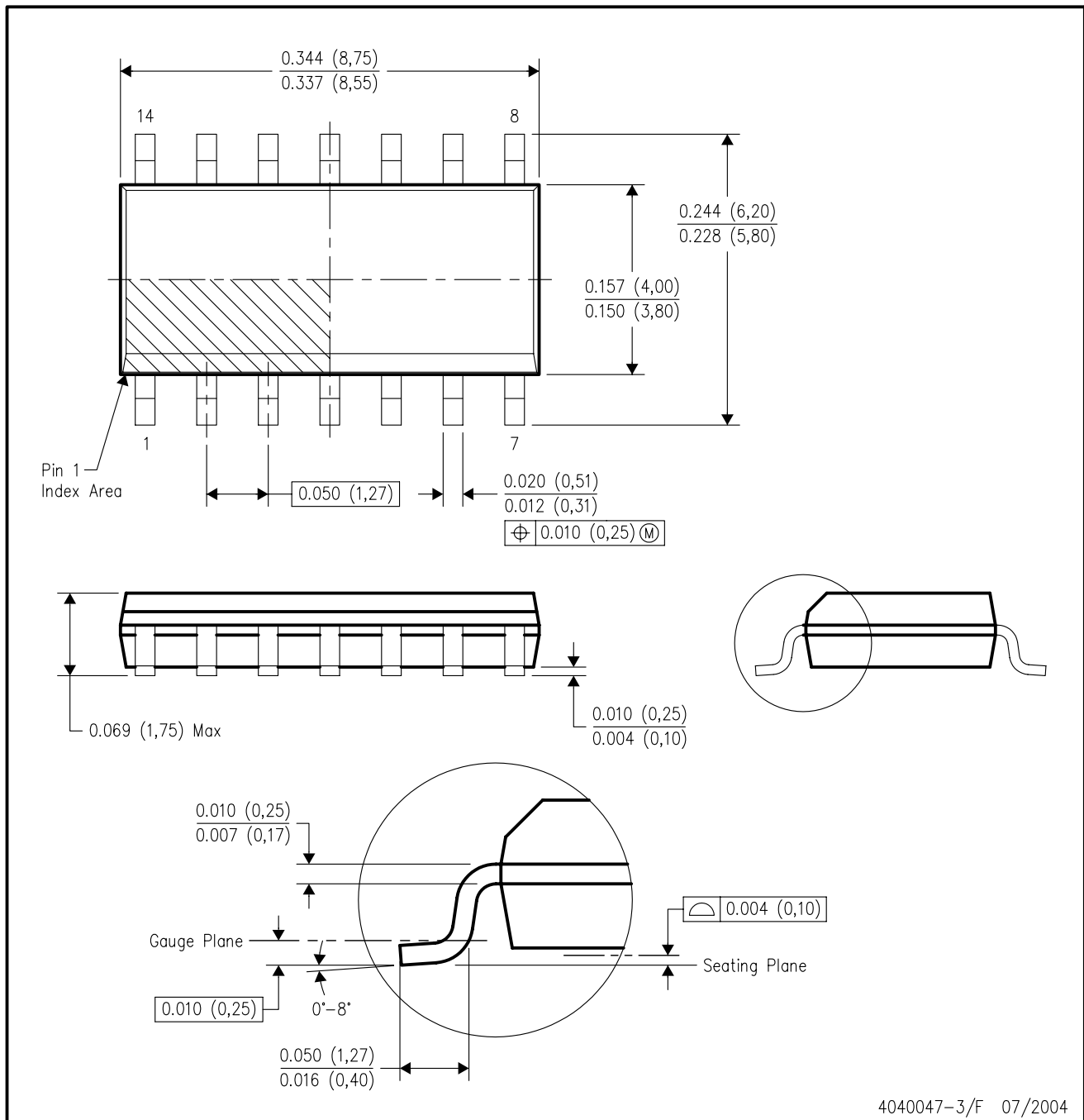


- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. Phase relationships between waveforms are arbitrary.
 - For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

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