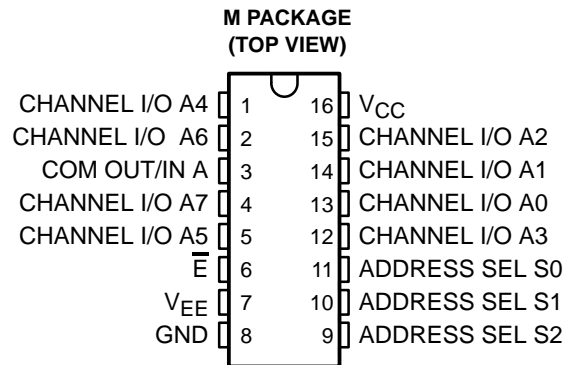


- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Wide Analog Input Voltage Range of ±5 V Max**
- **Low ON Resistance**
 - 70 Ω Typical ($V_{CC} - V_{EE} = 4.5\text{ V}$)
 - 40 Ω Typical ($V_{CC} - V_{EE} = 9\text{ V}$)
- **Low Crosstalk Between Switches**
- **Fast Switching and Propagation Speeds**
- **Break-Before-Make Switching**
- **Operation Control Voltage = 2 V to 6 V**
- **Switch Voltage = 0 V to 10 V**
- **High Noise Immunity $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} , $V_{CC} = 5\text{ V}$**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



description

This device is a digitally controlled analog switch that utilizes silicon gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

This analog multiplexer/demultiplexer controls analog voltages that may vary across the voltage supply range (i.e., V_{CC} to V_{EE}). These bidirectional switches allow any analog input to be used as an output and vice versa. The switches have low ON resistance and low OFF leakages. In addition, the device has an enable control (\bar{E}) that, when high, disables all switches to their OFF state.

ORDERING INFORMATION

T _A	PACKAGE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – M Tape and reel	CD74HC4051MM96EP	HC4051MEP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

CD74HC4051-EP ANALOG MULTIPLEXER/DEMULTIPLEXER

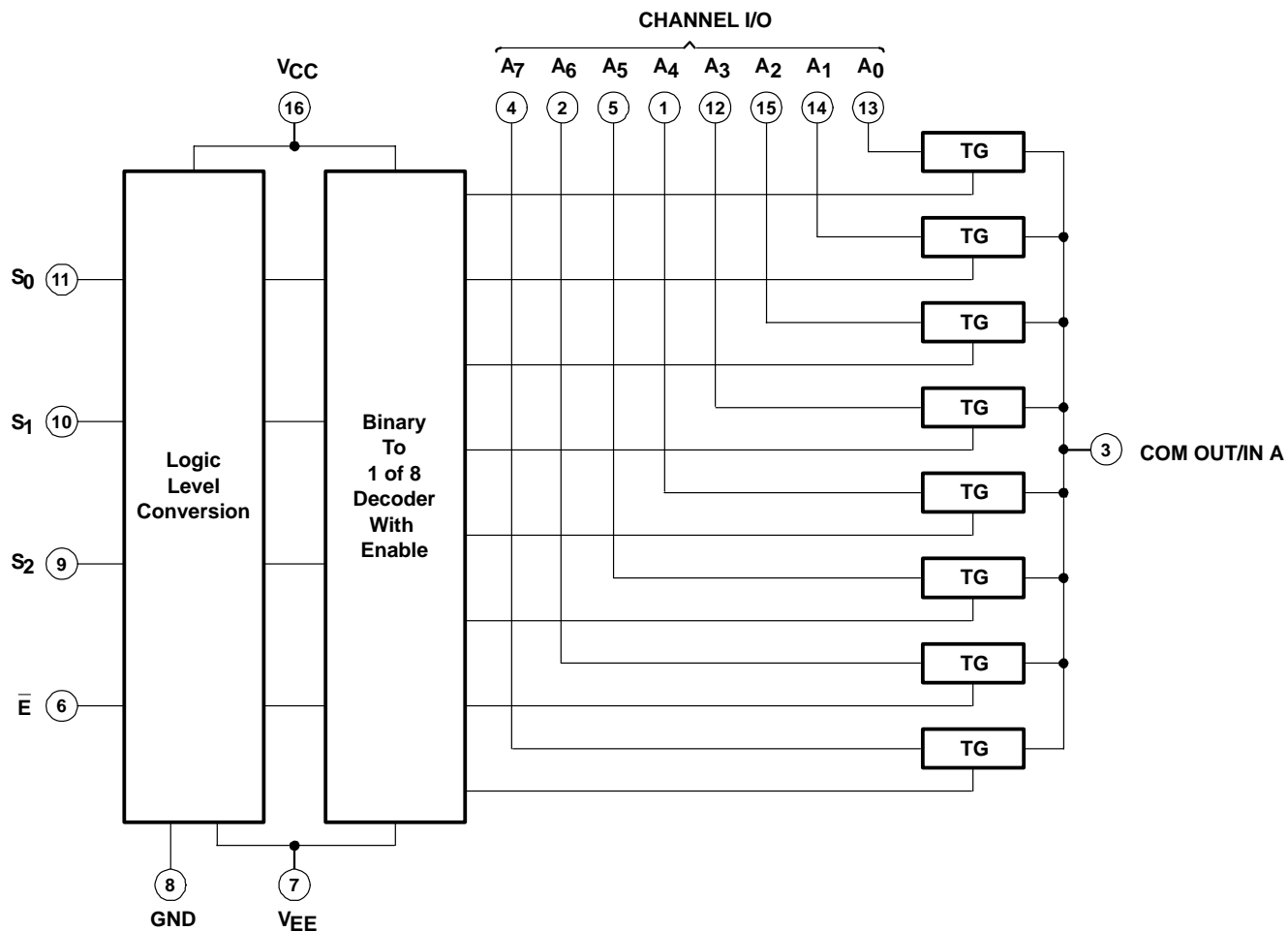
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FUNCTION TABLE

\bar{E}	INPUTS			ON CHANNEL(S)
	S ₂	S ₁	S ₀	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

X = Don't care

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC} - V_{EE}$ (see Note 1)	-0.5 V to 10.5 V
Supply voltage range, V_{CC}	-0.5 V to 7 V
Supply voltage range, V_{EE}	+0.5 V to -7 V
Input clamp current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	± 20 mA
Output clamp current, I_{OK} ($V_O < V_{EE} - 0.5$ V or $V_O > V_{CC} + 0.5$ V)	± 20 mA
Switch current ($V_I > V_{EE} - 0.5$ V or $V_I < V_{CC} + 0.5$ V)	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
V_{EE} current, I_{EE}	-20 mA
Package thermal impedance, θ_{JA} (see Note 2): M package	73°C/W
Maximum junction temperature, T_J	150°C
Lead temperature (during soldering):	
At distance $1/16 \pm 1/32$ inch ($1,59 \pm 0,79$ mm) from case for 10 s max	300°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages referenced to GND unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT	
V_{CC}	Supply voltage (see Note 4)	2	6	V	
	Supply voltage, $V_{CC} - V_{EE}$ (see Figure 1)	2	10	V	
V_{EE}	Supply voltage, (see Note 4 and Figure 2)	0	-6	V	
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5	V	
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0.5	V	
		$V_{CC} = 4.5$ V	1.35		
		$V_{CC} = 6$ V	1.8		
V_I	Input control voltage	0	V_{CC}	V	
V_{IS}	Analog switch I/O voltage	V_{EE}	V_{CC}	V	
t_t	Input transition (rise and fall) time	$V_{CC} = 2$ V	0	1000	ns
		$V_{CC} = 4.5$ V	0	500	
		$V_{CC} = 6$ V	0	400	
T_A	Operating free-air temperature	-55	125	°C	

- NOTES: 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
4. In certain applications, the external load resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6 V (calculated from r_{ON} values shown in electrical characteristics table). No V_{CC} current flows through R_L if the switch current flows into the COM OUT/IN A terminal.

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recommended operating area as a function of supply voltages

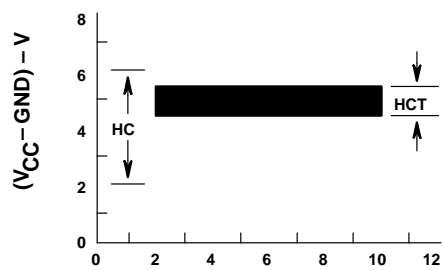


Figure 1

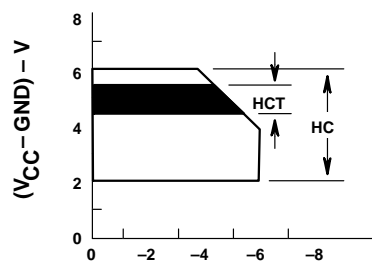


Figure 2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{EE}	V _{CC}	T _A = 25°C			T _A = -55°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
r _{on}	I _O = 1 mA, V _I = V _{IH} or V _{IL} , See Figure 8	V _{IS} = V _{CC} or V _{EE}	0 V	4.5 V	70	160		240	Ω
			0 V	6 V	60	140		210	
			-4.5 V	4.5 V	40	120		180	
		V _{IS} = V _{CC} to V _{EE}	0 V	4.5 V	90	180		270	
			0 V	6 V	80	160		240	
			-4.5 V	4.5 V	45	130		195	
Δr _{on}	Between any two channels	0 V	4.5 V	10				Ω	
		0 V	6 V	8.5					
		-4.5 V	4.5 V	5					
I _{Iz}	For switch OFF: When V _{IS} = V _{CC} , V _{OS} = V _{EE} ; When V _{IS} = V _{EE} , V _{OS} = V _{CC} For switch ON: All applicable combinations of V _{IS} and V _{OS} voltage levels, V _I = V _{IH} or V _{IL}	0 V	6 V		±0.2		±2	μA	
		-5 V	5 V		±0.4		±4		
I _{IL}	V _I = V _{CC} or GND	0 V	6 V		±0.1		±1	μA	
I _{CC}	I _O = 0, V _I = V _{CC} or GND	When V _{IS} = V _{EE} , V _{OS} = V _{CC}	0 V	6 V		8		160	μA
		When V _{IS} = V _{CC} , V _{OS} = V _{EE}	-5 V	5 V		16		320	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{EE}	V _{CC}	T _A = 25°C		T _A = -55°C TO 125°C		UNIT
						MIN	MAX	MIN	MAX	
t _{pd}	IN	OUT	C _L = 15 pF		5 V		4			ns
			C _L = 50 pF	0 V	2 V		60		90	ns
					4.5 V		12		18	
					6 V		10		15	
-4.5 V	4.5 V		8		12					
t _{en}	ADDRESS SEL or \bar{E}	OUT	C _L = 15 pF		5 V		19			ns
			C _L = 50 pF	0 V	2 V		225		340	
					4.5 V		45		68	
					6 V		38		57	
-4.5 V	4.5 V		32		48					
t _{dis}	ADDRESS SEL or \bar{E}	OUT	C _L = 15 pF		5 V		19			ns
			C _L = 50 pF	0 V	2 V		225		340	
					4.5 V		45		68	
					6 V		38		57	
-4.5 V	4.5 V		32		48					
C _I	Control		C _L = 50 pF				10		10	pF

operating characteristics, V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns

PARAMETER	TYP	UNIT
C _{pd} Power dissipation capacitance (see Note 5)	50	pF

NOTE 5: C_{pd} is used to determine the dynamic power consumption, per package.

$$P_D = C_{pd} V_{CC}^2 f_I + \sum (C_L + C_S) V_{CC}^2 f_O$$

f_O = output frequency

f_I = input frequency

C_L = output load capacitance

C_S = switch capacitance

V_{CC} = supply voltage

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analog channel characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{EE}	V_{CC}	MIN	TYP	MAX	UNIT
C_I	Switch input capacitance				5		pF
C_{COM}	Common output capacitance				25		pF
f_{max}	Minimum switch frequency response at -3 dB	-2.25 V	2.25 V		145		MHz
		-4.5 V	4.5 V		180		
Sine-wave distortion	See Figure 4	-2.25 V	2.25 V		0.035		%
		-4.5 V	4.5 V		0.018		
\bar{E} or ADDRESS SEL to switch feed-through noise	See Figure 5, and Notes 7 and 8	-2.25 V	2.25 V		(TBD)		mV
		-4.5 V	4.5 V		(TBD)		
Switch OFF signal feed through	See Figure 6 and Figure 10, and Notes 7 and 8	-2.25 V	2.25 V		-73		dB
		-4.5 V	4.5 V		-75		

- NOTES: 6. Adjust input voltage to obtain 0 dBm at V_{OS} for $f_{IN} = 1$ MHz.
 7. V_{IS} is centered at $(V_{CC} - V_{EE})/2$.
 8. Adjust input for 0 dBm.

PARAMETER MEASUREMENT INFORMATION

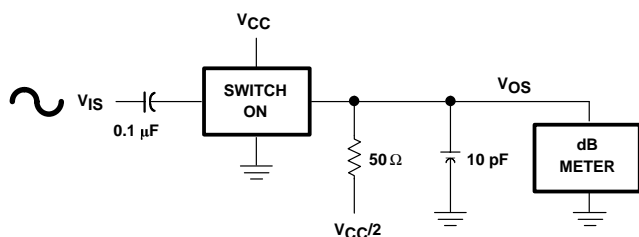


Figure 3. Frequency-Response Test Circuit

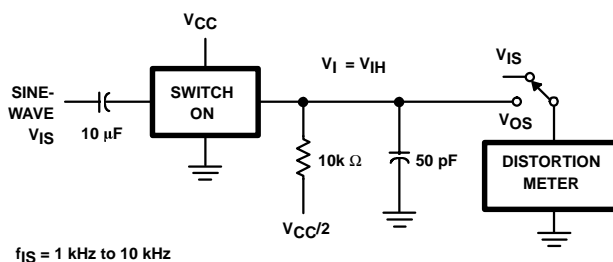


Figure 4. Sine-Wave Distortion Test Circuit

PARAMETER MEASUREMENT INFORMATION

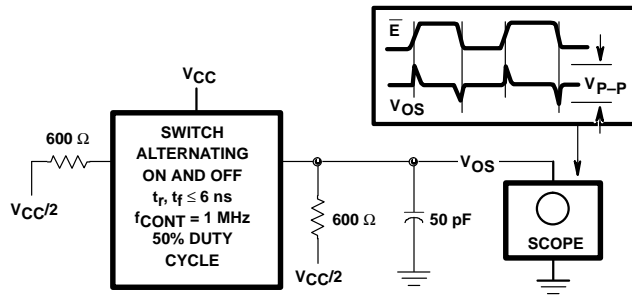


Figure 5. Control to Switch Feed-Through Noise Test Circuit

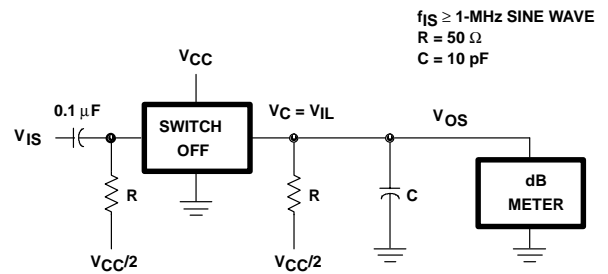
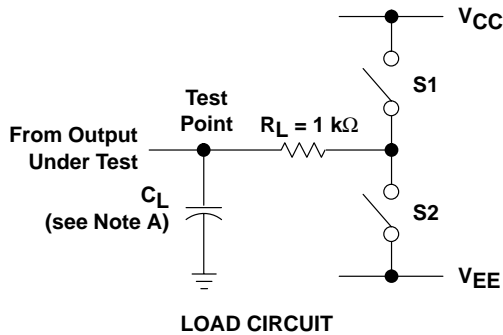
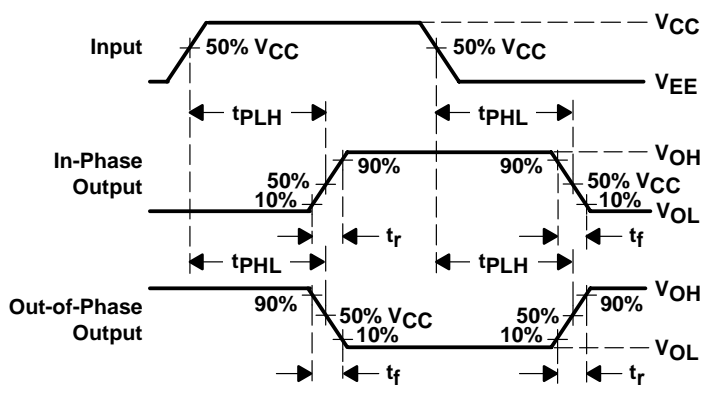


Figure 6. Switch OFF Signal Feed-Through Test Circuit

PARAMETER MEASUREMENT INFORMATION

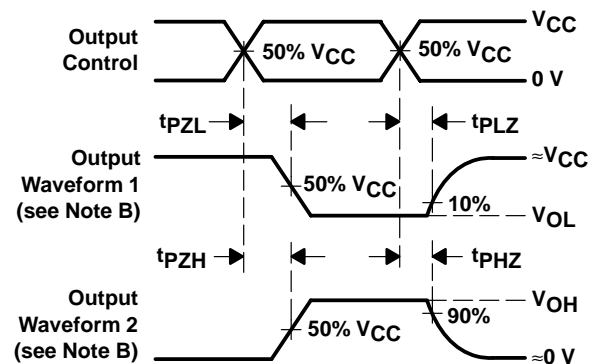


PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd}		Open	Open



VOLTAGE WAVEFORMS

PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS

OUTPUT ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 6\text{ ns}$, $t_f = 6\text{ ns}$.
 D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 E. The outputs are measured one at a time with one input transition per measurement.
 F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 G. t_{PZL} and t_{PZH} are the same as t_{en} .
 H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 7. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

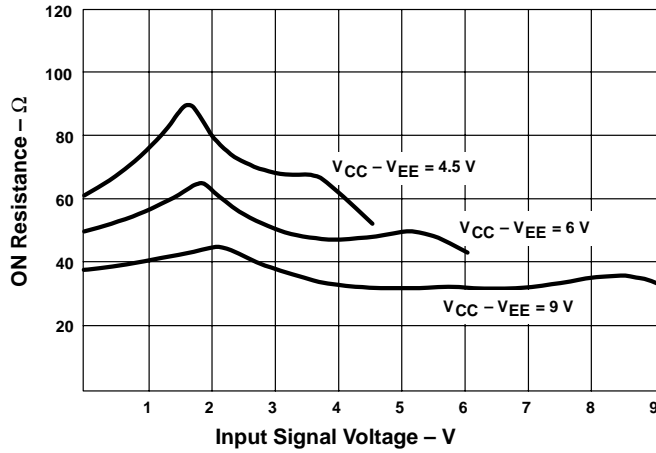


Figure 8. Typical ON Resistance vs Input Signal Voltage

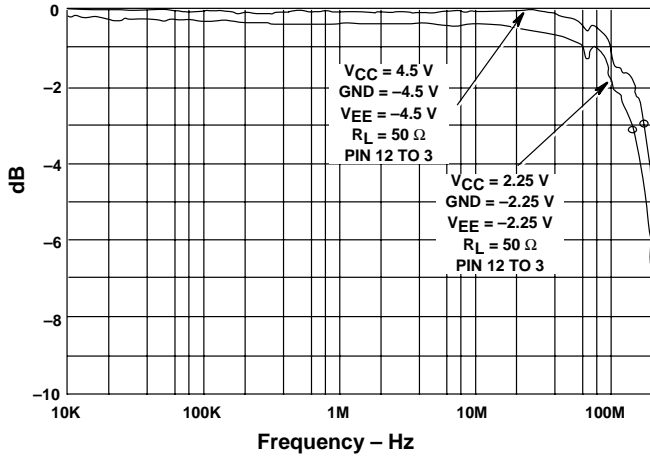


Figure 9. Channel ON Bandwidth

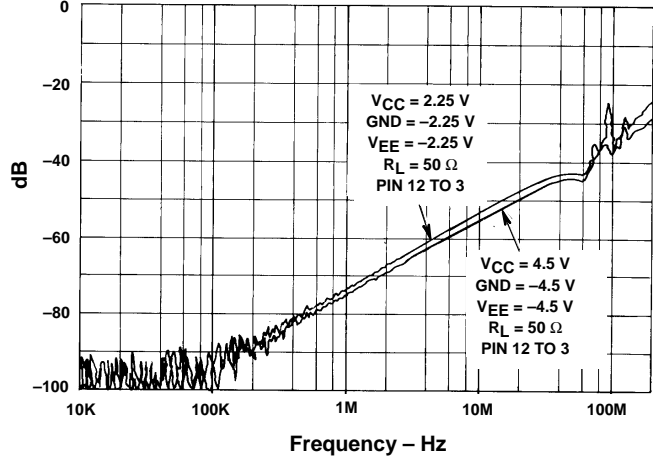


Figure 10. Channel OFF Feed Through

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74HC4051MM96EP	ACTIVE	SOIC	D	16	2500	None	Call TI	Level-1-220C-UNLIM
V62/03606-01XE	ACTIVE	SOIC	D	16	2500	None	Call TI	Level-1-220C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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