

CDCV857

2.5-V PHASE LOCK LOOP CLOCK DRIVER

SCAS645A – AUGUST 2000 – REVISED OCTOBER 2000

- Phase-Lock Loop Clock Driver for Double Data-Rate Synchronous DRAM Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 60 to 200 MHz
- Low Jitter (cyc–cyc): ± 75 ps
- Distributes One Differential Clock Input to Ten Differential Outputs
- Three-State Outputs When the Input Differential Clocks Are <20 MHz
- Operates From Dual 2.5-V Supplies
- 48-Pin TSSOP Package
- Consumes < 200- μ A Quiescent Current
- External Feedback PIN ($\overline{\text{FBIN}}$, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Input Clocks

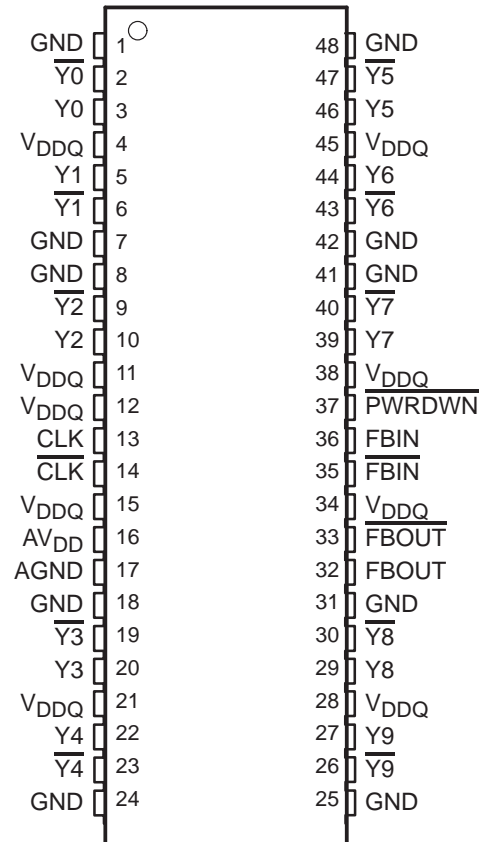
description

The CDCV857 is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to ten differential pairs of clock outputs (Y[0:9], $\overline{\text{Y}}[0:9]$) and one differential pair of feedback clock output (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the clock inputs (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), and the analog power input (AV_{DD}). When $\overline{\text{PWRDWN}}$ is high, the outputs switch in phase and frequency with CLK. When $\overline{\text{PWRDWN}}$ is low, all outputs are disabled to high impedance state (3-state), and the PLL is shut down (low power mode). The device also enters this low power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit will detect the low frequency condition and after applying a >20 MHz input signal this detection circuit turns on the PLL again and enables the outputs.

When AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes. The CDCV857 is also able to track spread spectrum clocking for reduced EMI.

Since the CDCV857 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCV857 is characterized for operation from 0°C to 85°C.

**DGG PACKAGE
(TOP VIEW)**



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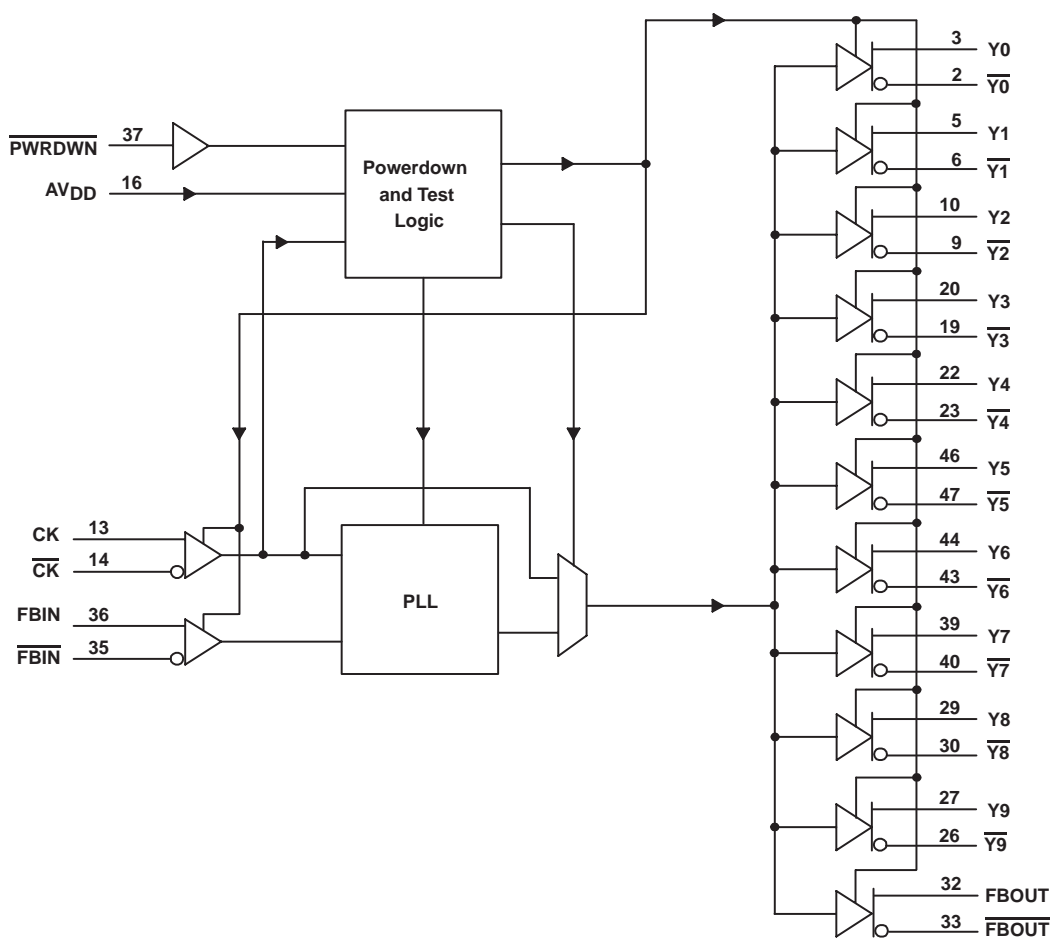
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FUNCTION TABLE
(Select Functions)

INPUTS				OUTPUTS				PLL
AVDD	PWRDWN	CLK	CLK	Y[0:9]	Y[0:9]	FBOUT	FBOUT	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	<20 MHz	<20 MHz	Z	Z	Z	Z	Off

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	17		Ground for 2.5-V analog supply
AV _{DD}	16		2.5-V Analog supply
CLK, $\overline{\text{CLK}}$	13, 14	I	Differential clock input
$\overline{\text{FBIN}}$, FBIN	35, 36	I	Feedback differential clock input
F $\overline{\text{BOUT}}$, FBOUT	32, 33	O	Feedback differential clock output
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48		Ground
$\overline{\text{PWRDWN}}$	37	I	Output enable for Y and $\overline{\text{Y}}$
V _{DDQ}	4, 11, 12, 15, 21, 28, 34, 38, 45		2.5-V Supply
Y[0:9]	3, 5, 10, 20, 22, 27, 29, 39, 44, 46	O	Buffered output copies of input clock, CLK
$\overline{\text{Y}}$ [0:9]	2, 6, 9, 19, 23, 26, 30, 40, 43, 47	O	Buffered output copies of input clock, $\overline{\text{CLK}}$

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V _{DDQ} , AV _{DD}	0.5 V to 3.6 V
Input voltage range, V _I (see Notes 1 and 2)	–0.5 V to V _{DDQ} 0.5 V
Output voltage range, V _O (see Notes 1 and 2)	–0.5 V to V _{DDQ} 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DDQ})	±50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DDQ})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{DDQ})	±50 mA
Continuous current to GND or V _{DDQ}	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
Storage temperature range T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 3.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

		MIN	TYP	MAX	UNIT
Supply voltage, V_{DDQ} , AV_{DD}		2.3		2.7	V
Low level input voltage, V_{IL}	CLK, $\overline{\text{CLK}}$, FBIN, $\overline{\text{FBIN}}$			$V_{DDQ}/2 - 0.18$	V
	PWRDWN	-0.3		0.7	
High level input voltage, V_{IH}	CLK, $\overline{\text{CLK}}$, FBIN, $\overline{\text{FBIN}}$	$V_{DDQ}/2 + 0.18$			V
	PWRDWN	1.7		$V_{DDQ} + 0.3$	
DC input signal voltage (see Note 5)		-0.3		V_{DDQ}	V
Differential input signal voltage, V_{ID} (see Note 6)	DC CLK, FBIN	0.36		$V_{DDQ} + 0.6$	V
	AC CLK, FBIN	0.7		$V_{DDQ} + 0.6$	
Output differential cross-voltage, V_{OX} (see Note 7)		$V_{DDQ}/2 - 0.2$	$V_{DDQ}/2$	$V_{DDQ}/2 + 0.2$	V
Input differential pair cross-voltage, V_{IX} (see Note 7)		$V_{DDQ}/2 - 0.2$		$V_{DDQ}/2 + 0.2$	V
High-level output current, I_{OH}				-12	mA
Low-level output current, I_{OL}				12	mA
Input slew rate, SR		1		4	V/ns
Operating free-air temperature, T_A		0		85	°C

- NOTES:
4. Unused inputs must be held high or low to prevent them from floating.
 5. DC input signal voltage specifies the allowable dc execution of differential input.
 6. Differential input signal voltage specifies the differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input level and V_{CP} is the complementary input level.
 7. Differential cross-point voltage is expected to track variations of V_{CC} and is the voltage at which the differential signals must be crossing.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IK}	Input voltage	All inputs	V _{DDQ} = 2.3 V, I _I = -18 mA			-1.2	V
V _{OH}	High-level output voltage		V _{DDQ} = min to max, I _{OH} = -1 mA	V _{DDQ} - 0.1			V
			V _{DDQ} = 2.3 V, I _{OH} = -12 mA	1.7			
V _{OL}	Low-level output voltage		V _{DDQ} = min to max, I _{OL} = 1 mA			0.1	V
			V _{DDQ} = 2.3 V, I _{OL} = 12 mA			0.6	
I _{OH}	High-level output current		V _{DDQ} = 2.3 V, V _O = 1 V	-18	-32		mA
I _{OL}	Low-level output current		V _{DDQ} = 2.3 V, V _O = 1.2 V	26	35		mA
V _O	Output voltage swing		Differential outputs are terminated with 120 Ω	1.1		V _{DDQ} - 0.4	V
V _{OX}	Output differential cross-voltage§			V _{DDQ} /2 - 0.2	V _{DDQ} /2	V _{DDQ} /2 + 0.2	
I _I	Input current		V _{DDQ} = 2.7 V, V _I = 0 V to 2.7 V			±10	μA
I _{OZ}	High-impedance-state output current		V _{DDQ} = 2.7 V, V _O = V _{DDQ} or GND			±10	μA
I _{DDPD}	Power down current on V _{DDQ} + AV _{DD}		CLK and $\overline{\text{CLK}}$ = 0 MHz; $\overline{\text{PWRDWN}}$ = Low; Σ of I _{DD} and AI _{DD}		100	200	μA
I _{DD}	Dynamic current on V _{DDQ}	all outputs loaded as shown in Figure 3	f _O = 200 MHz		275	330	mA
			f _O = 167 MHz		250	300	
AI _{DD}	Supply current on AV _{DD}		f _O = 200 MHz		10	12	mA
			f _O = 167 MHz		8	10	
C _I	Input capacitance		V _{CC} = 2.5 V, V _I = V _{CC} or GND	2	2.5	3	pF
C _O	Output capacitance		V _{CC} = 2.5 V, V _O = V _{CC} or GND	2.5	3	3.5	pF

† All typical values are at respective nominal V_{DDQ}.

‡ The value of V_{OC} is expected to be |V_{TR} + V_{CPI}|/2. In case of each clock directly terminated by a 120-Ω resistor, where V_{TR} is the true input signal voltage and V_{CPI} is the complementary input signal voltage.

§ Differential cross-point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signals must be crossing.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f _{CK}	Operating clock frequency	60	200	MHz
	Application clock frequency			
Input clock duty cycle		40%	60%	
Stabilization time¶ (PLL mode)			10	μs
Stabilization time¶ (Bypass mode)			30	ns

¶ Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.



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switching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT	
t_{PLH}^{\ddagger}	Low to high level propagation delay time	Test mode/CLK to any output		4.5		ns	
t_{PHL}^{\ddagger}	High-to low level propagation delay time	Test mode/CLK to any output		4.5		ns	
$t_{jit(per)}^{\S}$	Jitter (period), See Figure 6	66 MHz	-90		90	ps	
		100/133/167/200 MHz	-75		75	ps	
$t_{jit(cc)}^{\S}$	Jitter (cycle-to-cycle), See Figure 3	66 MHz	-180		180	ps	
		100/133/167/200 MHz	-75		75	ps	
$t_{jit(hper)}^{\S}$	Half-period jitter, See Figure 7	66 MHz	-160		160	ps	
		100/133/167/200 MHz	-100		100	ps	
$t_{slr(i)}$	Input clock slew rate, See Figure 8		1		4	V/ns	
$t_{slr(o)}$	Output clock slew rate, See Figure 8		1		2	V/ns	
$t_{d(\emptyset)}^{\S}$	Dynamic phase offset (this includes jitter), See Figure 4(b)	SSC off	66 MHz	-180		180	ps
			100/133 MHz	-130		130	
			167/200 MHz	-90		90	
		SSC on	66 MHz	-230		230	
			100/133 MHz	-170		170	
			167/200 MHz	-100		100	
$t_{(\emptyset)}$	Static phase offset, See Figure 4(a)	66/100/133/167 MHz	-100		100	ps	
		200 MHz	-150		50	ps	
$tsk(o)^{\parallel}$	Output skew, See Figure 5				75	ps	
t_r, t_f	Output rise and fall times (20% – 80%)	Load: 120 Ω /14 pF	650		900	ps	

[†] All typical values are at a respective nominal V_{DDQ} .

[‡] Refers to transition of noninverting output.

[§] This parameter is assured by design but can not be 100% production tested.

^{||} All differential output pins are terminated with 120 Ω /14 pF.

PARAMETER MEASUREMENT INFORMATION

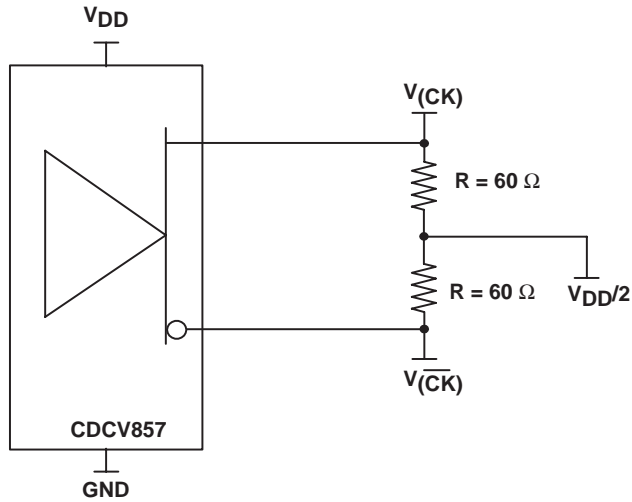
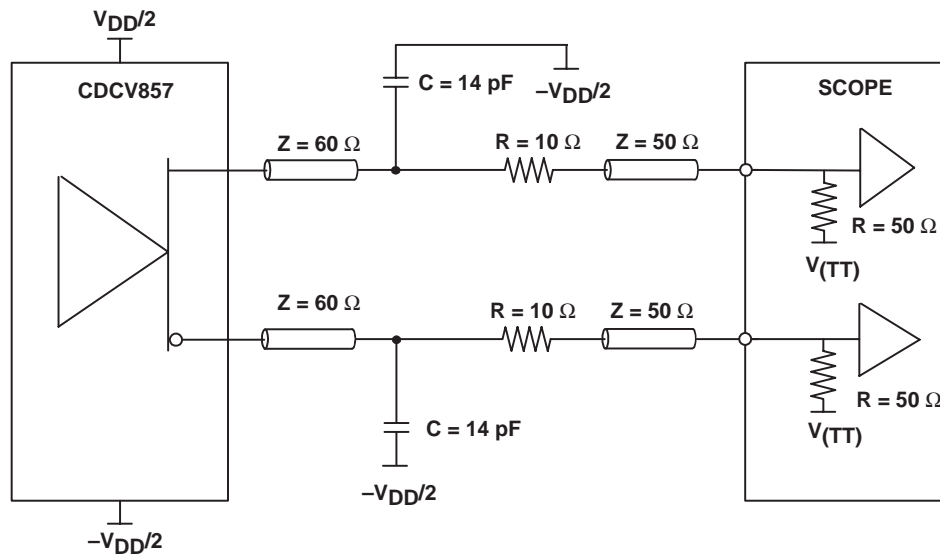


Figure 1. IBIS Model Output Load (used for slew rate measurement)



NOTE: $V_{(TT)} = \text{GND}$

Figure 2. Output Load Test Circuit

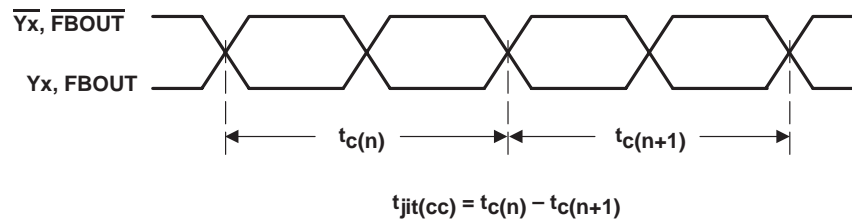
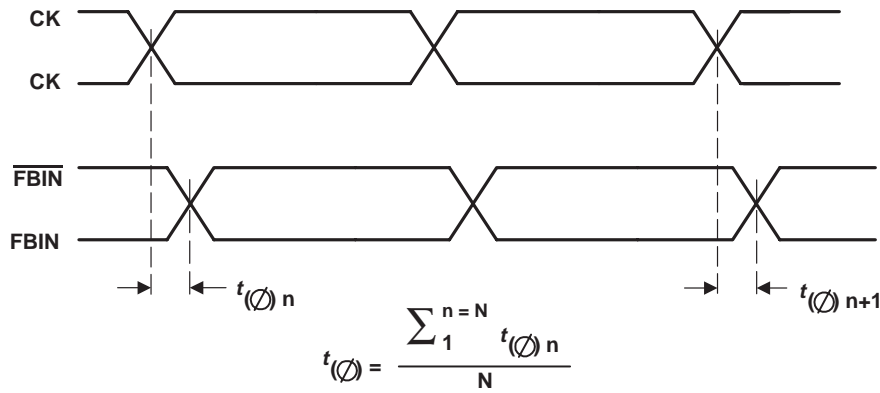


Figure 3. Cycle-to-Cycle Jitter

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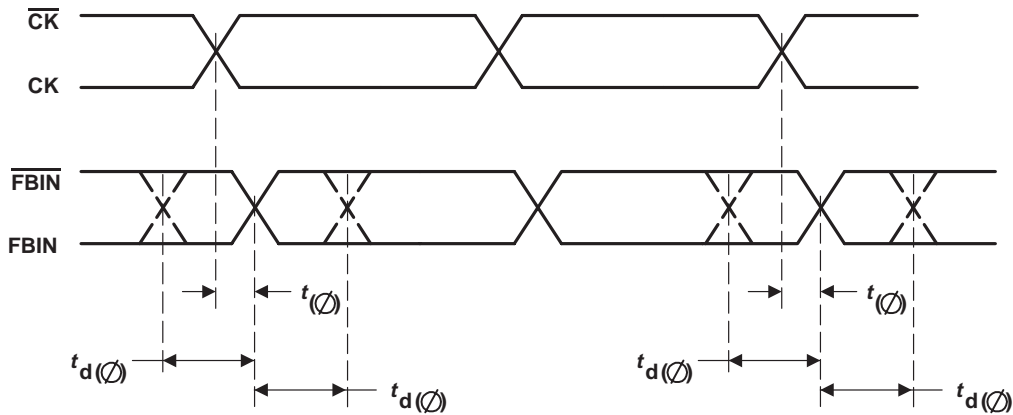
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PARAMETER MEASUREMENT INFORMATION



(N is a large number of samples)

(a) Static Phase Offset



(b) Dynamic Phase Offset

Figure 4. Phase Offset

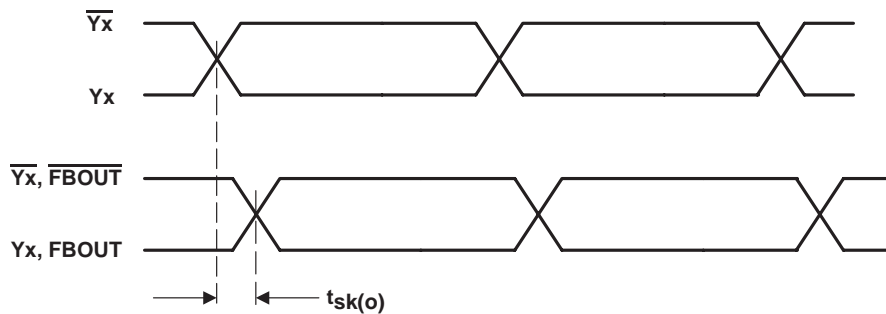


Figure 5. Output Skew

PARAMETER MEASUREMENT INFORMATION

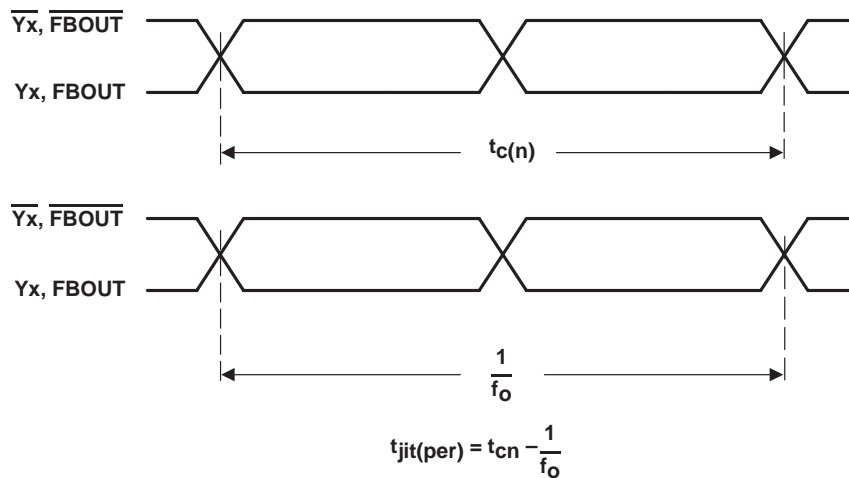


Figure 6. Period Jitter

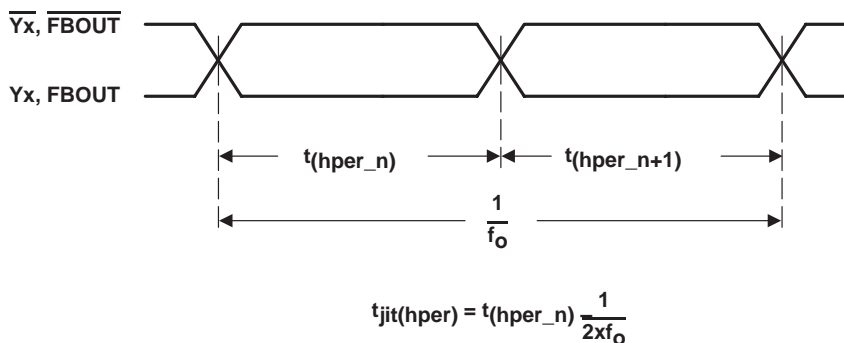


Figure 7. Half-Period Jitter

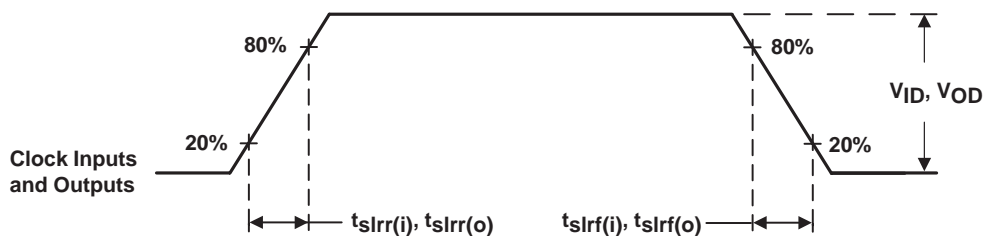


Figure 8. Input and Output Slew Rates

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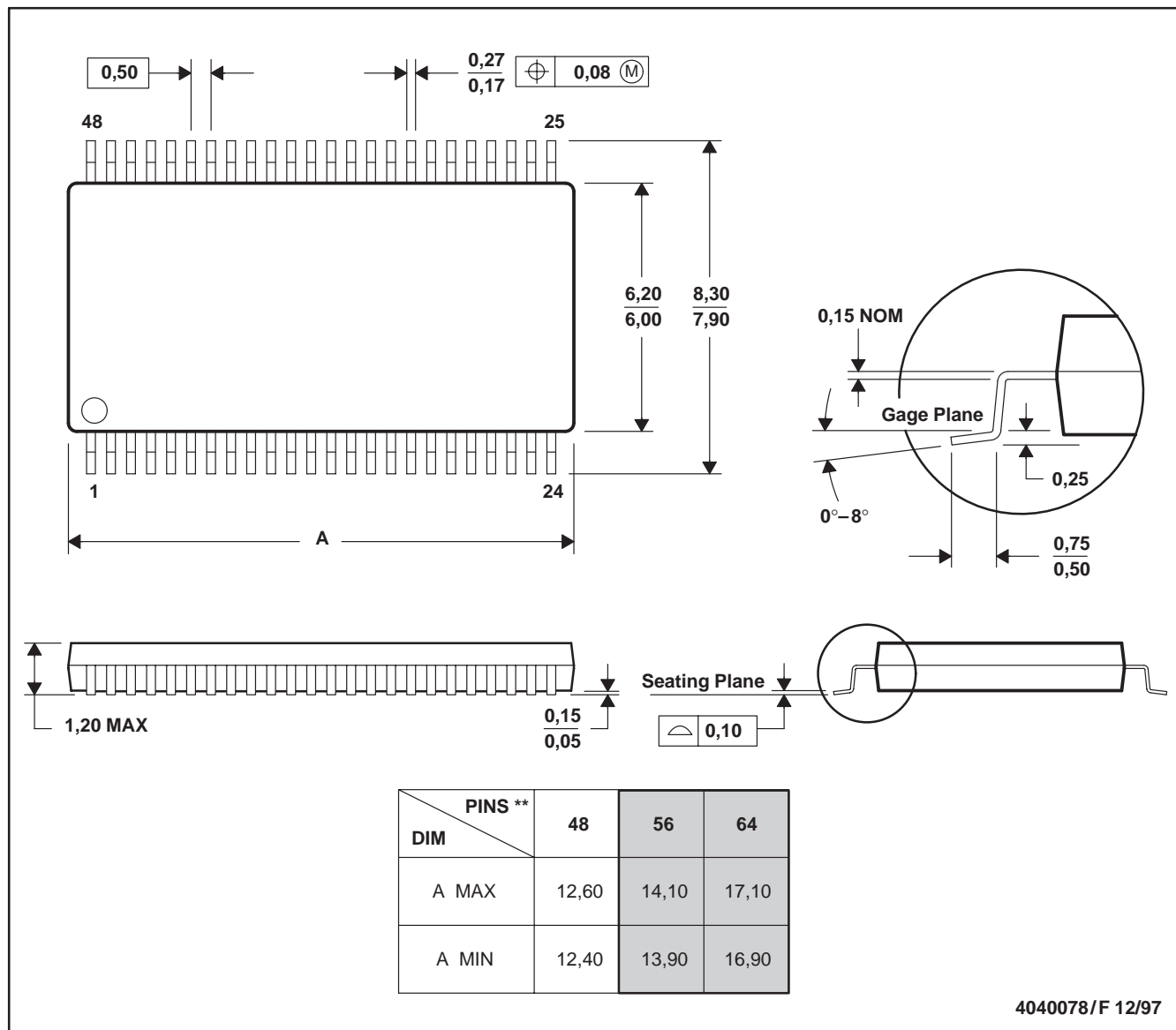
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MECHANICAL DATA

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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