

# CDCVF857

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

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- **Recommended Applications:**
  - DDR Memory Modules (DDR400/333/266/200)
  - Zero Delay Fan-Out Buffer
- **Spread Spectrum Clock Compatible**
- **Operating Frequency: 60 MHz to 220 MHz**
- **Low Jitter (Cycle-Cycle):  $\pm 35$  ps**
- **Low Static Phase Offset:  $\pm 50$  ps**
- **Low Jitter (Period):  $\pm 30$  ps**
- **1-To-10 Differential Clock Distribution (SSTL2)**
- **Best in Class for  $V_{OX} = V_{DD}/2 \pm 0.1$  V**
- **Operates From Dual 2.6-V or 2.5-V Supplies**
- **Available in a 40-Pin MLF Package, 48-Pin TSSOP Package, 56-Ball MicroStar Junior™ BGA Package**
- **Consumes  $< 100\text{-}\mu\text{A}$  Quiescent Current**
- **External Feedback Pins (FBIN,  $\overline{\text{FBIN}}$ ) Are Used to Synchronize the Outputs to the Input Clocks**
- **Meets/Exceeds JEDEC Standard (JESD82–1) For DDRI-200/266/333 Specification**
- **Meets/Exceeds Proposed DDRI-400 Specification (JESD82–1A)**
- **Enters Low-Power Mode When No CLK Input Signal Is Applied or PWRDWN Is Low**

### description

The CDCVF857 is a high-performance, low-skew, low-jitter, zero-delay buffer that distributes a differential clock input pair (CLK,  $\overline{\text{CLK}}$ ) to 10 differential pairs of clock outputs (Y[0:9],  $\overline{\text{Y}}[0:9]$ ) and one differential pair of feedback clock outputs (FBOU,  $\overline{\text{FBOU}}$ ). The clock outputs are controlled by the clock inputs (CLK,  $\overline{\text{CLK}}$ ), the feedback clocks (FBIN,  $\overline{\text{FBIN}}$ ), and the analog power input ( $\text{AV}_{\text{DD}}$ ). When PWRDWN is high, the outputs switch in phase and frequency with CLK. When PWRDWN is low, all outputs are disabled to a high-impedance state (3-state) and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit detects the low frequency condition and, after applying a  $>20$ -MHz input signal, this detection circuit turns the PLL on and enables the outputs.

When  $\text{AV}_{\text{DD}}$  is strapped low, the PLL is turned off and bypassed for test purposes. The CDCVF857 is also able to track spread spectrum clocking for reduced EMI.

Because the CDCVF857 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCVF857 is characterized for both commercial and industrial temperature ranges.

#### AVAILABLE OPTIONS

T <sub>A</sub>	TSSOP (DGG)	40-Pin MLF	56-Ball BGA †
–40°C to 85°C	CDCVF857DGG	CDCVF857RTB	CDCVF857GQL

† Maximum load recommended is 12 pf for 200 MHz. At 12-pf load, maximum T<sub>A</sub> allowed is 70°C.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# CDCVF857

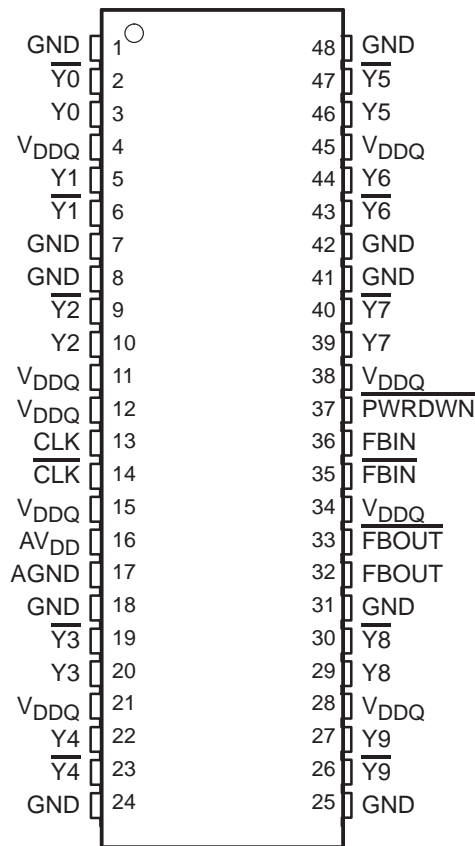
## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

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**FUNCTION TABLE**  
(Select Functions)

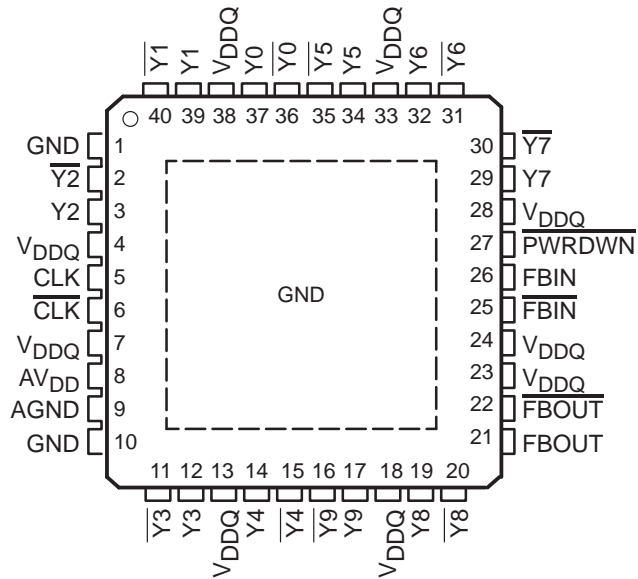
INPUTS				OUTPUTS				PLL
AVDD	PWRDWN	CLK	CLK	Y[0:9]	Y[0:9]	FBOUT	FBOUT	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	<20 MHz	<20 MHz	Z	Z	Z	Z	Off

**DGG PACKAGE**  
(TOP VIEW)



48-pin TSSOP (MO-153-ED)

**RTB PACKAGE**  
(TOP VIEW)

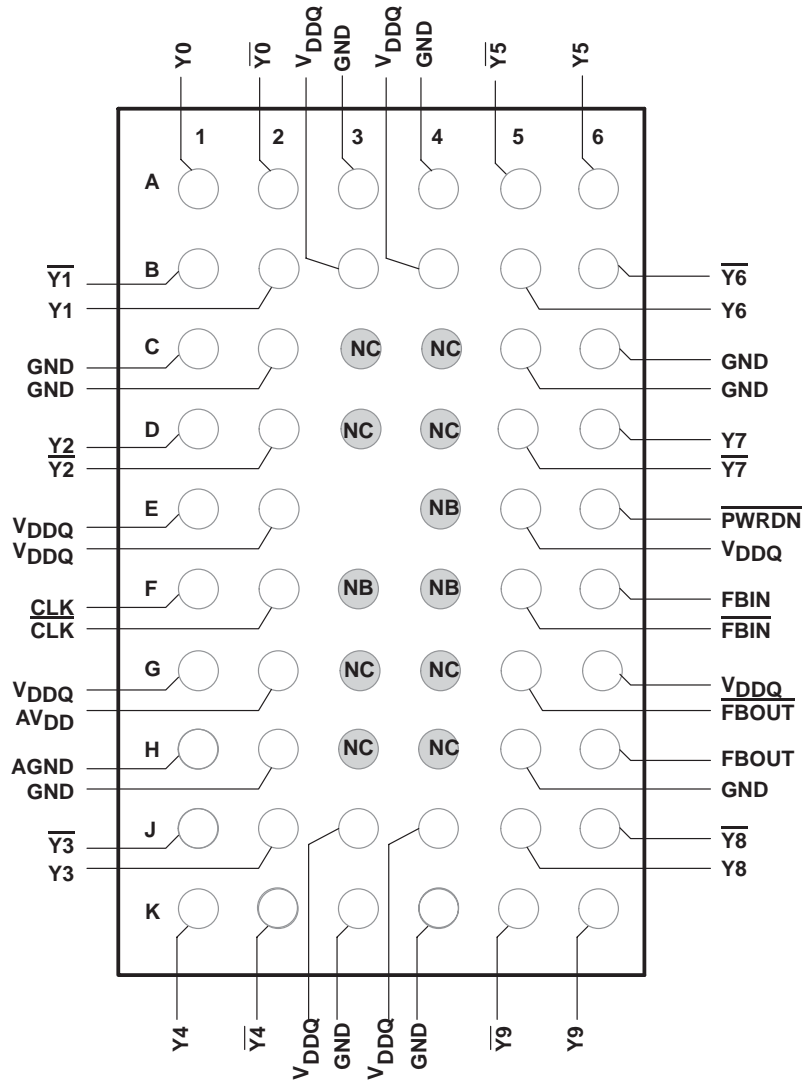


40-pin HP-VFQFP-N (6,0 x 6,0-mm Body Size,  
0,5-mm Pitch, M0#220, Variation VJJD-2,  
E2 = D2 = 2,9 mm ± 0,15 mm) Package Pinouts

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**MicroStar™ Junior (GQL) Package  
(TOP VIEW)**



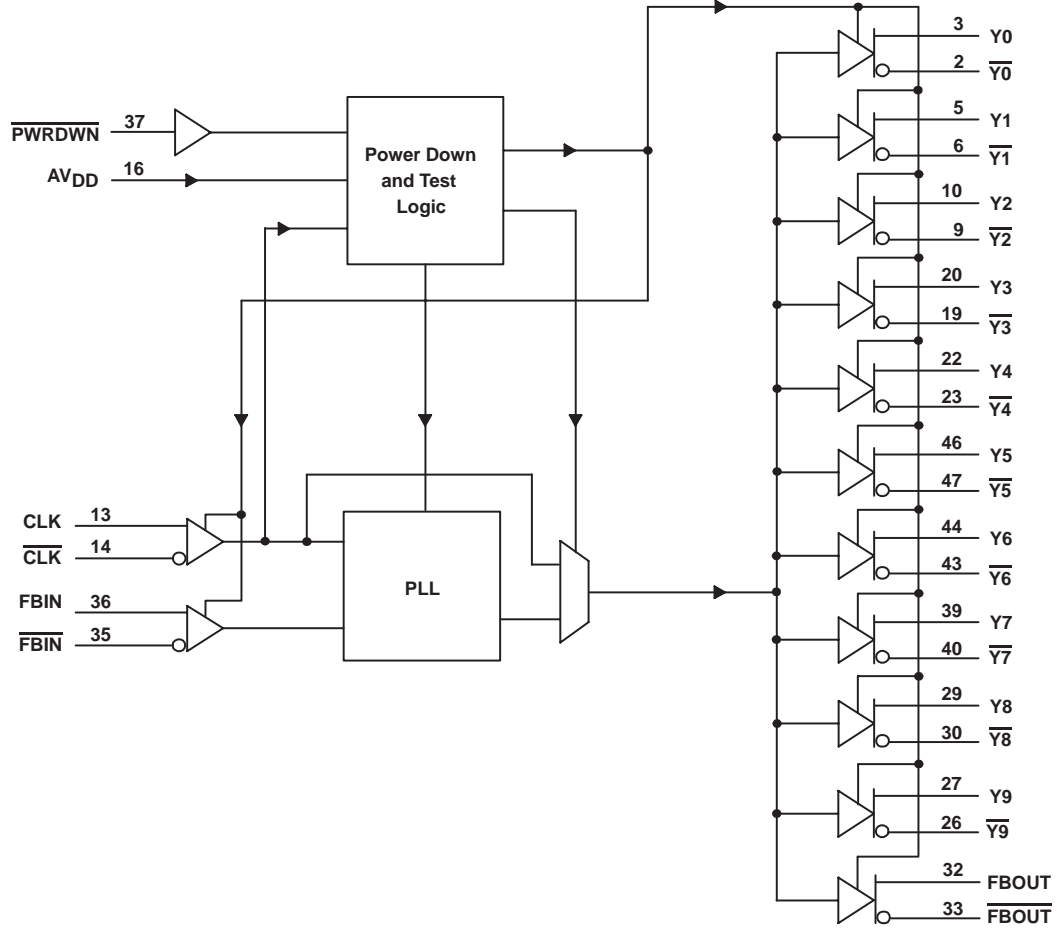
NB = No ball  
NC = No connection

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### functional block diagram



### Terminal Functions

NAME	TERMINAL				DESCRIPTION
	DGG	RTB	GQL		
AGND	17	9	H1		Ground for 2.5-V analog supply
AV <sub>DD</sub>	16	8	G2		2.5-V analog supply
CLK, $\overline{\text{CLK}}$	13, 14	5, 6	F1, F2	I	Differential clock input
$\overline{\text{FBIN}}$ , FBIN	35, 36	25, 26	F5, F6	I	Feedback differential clock input
FBO <sub>UT</sub> , $\overline{\text{FBOU}}$	32, 33	21, 22	H6, G5	O	Feedback differential clock output
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	1, 10	A3, A4, C1, C2, C5, C6, H2, H5, K3, K4		Ground
$\overline{\text{PWRDWN}}$	37	27	E6	I	Output enable for Y and $\overline{\text{Y}}$
V <sub>DDQ</sub>	4, 11, 12, 15, 21, 28, 34, 38, 45	4, 7, 13, 18, 23, 24, 28, 33, 38	B3, B4, E1, E2, E5, G1, G6, J3, J4		2.5-V supply
Y0, $\overline{\text{Y0}}$	3, 2	37, 36	A1, A2	O	Buffered output copies of input clock, CLK, $\overline{\text{CLK}}$
Y1, $\overline{\text{Y1}}$	5, 6	39, 40	B2, B1	O	
Y2, $\overline{\text{Y2}}$	10, 9	3, 2	D1, D2	O	
Y3, $\overline{\text{Y3}}$	20, 19	12, 11	J2, J1	O	
Y4, $\overline{\text{Y4}}$	22, 23	14, 15	K1, K2	O	
Y5, $\overline{\text{Y5}}$	46, 47	34, 35	A6, A5	O	
Y6, $\overline{\text{Y6}}$	44, 43	32, 31	B5, B6	O	
Y7, $\overline{\text{Y7}}$	39, 40	29, 30	D6, D5	O	
Y8, $\overline{\text{Y8}}$	29, 30	19, 20	J5, J6	O	
Y9, $\overline{\text{Y9}}$	27, 26	17, 16	K6, K5	O	

#### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>DDQ</sub> , AV <sub>DD</sub>	0.5 V to 3.6 V
Input voltage range, V <sub>I</sub> (see Notes 1 and 2)	-0.5 V to V <sub>DDQ</sub> + 0.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	-0.5 V to V <sub>DDQ</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DDQ</sub> )	±50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DDQ</sub> )	±50 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>DDQ</sub> )	±50 mA
Continuous current to GND or V <sub>DDQ</sub>	±100 mA
Storage temperature range T <sub>stg</sub>	-65°C to 150°C

$\theta_{JA}$  For TSSOP (DGG) Package (see Note 3)

$\theta_{JA}$  For MLF Package

$\theta_{JA}$  For GQL Package (see Note 4)

$\theta_{JA}$ For TSSOP (DGG) Package (see Note 3)			$\theta_{JA}$ For MLF Package		$\theta_{JA}$ For GQL Package (see Note 4)	
Airflow	Low K	High K	Airflow	With 4 Thermal Vias	Airflow	High K
0 ft/min	89.1°C/W	70°C/W	0 ft/min	44.7°C/W	0 ft/min	132.2°C/W
150 ft/min	78.5°C/W	65.3°C/W	150 ft/min		150 ft/min	126.4°C/W

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
  2. This value is limited to 3.6 V maximum.
  3. The package thermal impedance is calculated in accordance with JESD 51.
  4. Connecting the NC-balls (C3, C4, D3, D4, G3, G4, H3, H4) to a ground plane improves the  $\theta_{JA}$  to 114.8°C/W (0 airflow).

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### recommended operating conditions (see Note 5)

			MIN	TYP	MAX	UNIT
Supply voltage	V <sub>DDQ</sub>	PC1600 – PC3200	2.3		2.7	V
	AV <sub>DD</sub>		V <sub>DDQ</sub> – 0.12		2.7	
Low-level input voltage, V <sub>IL</sub>	CLK, $\overline{\text{CLK}}$ , FBIN, $\overline{\text{FBIN}}$				V <sub>DDQ</sub> /2 – 0.18	V
	PWRDWN		–0.3		0.7	
High-level input voltage, V <sub>IH</sub>	CLK, $\overline{\text{CLK}}$ , FBIN, $\overline{\text{FBIN}}$		V <sub>DDQ</sub> /2 + 0.18			V
	PWRDWN		1.7		V <sub>DDQ</sub> + 0.3	
DC input signal voltage (see Note 5)			–0.3		V <sub>DDQ</sub> + 0.3	V
Differential input signal voltage, V <sub>ID</sub> (see Note 6)	dc	CLK, FBIN	0.36		V <sub>DDQ</sub> + 0.6	V
	ac	CLK, FBIN	0.7		V <sub>DDQ</sub> + 0.6	
Input differential pair cross voltage, V <sub>IX</sub> (see Notes 7 and 8)			V <sub>DDQ</sub> /2 – 0.2		V <sub>DDQ</sub> /2 + 0.2	V
High-level output current, I <sub>OH</sub>					–12	mA
Low-level output current, I <sub>OL</sub>					12	mA
Input slew rate, SR			1		4	V/ns
Operating free-air temperature, T <sub>A</sub>			–40		85	°C

- NOTES: 5. The unused inputs must be held high or low to prevent them from floating.  
6. The dc input signal voltage specifies the allowable dc execution of the differential input.  
7. The differential input signal voltage specifies the differential voltage |V<sub>TR</sub> – V<sub>CP</sub>| required for switching, where V<sub>TR</sub> is the true input level and V<sub>CP</sub> is the complementary input level.  
8. The differential cross-point voltage is expected to track variations of V<sub>CC</sub> and is the voltage at which the differential signals must be crossing.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP <sup>†</sup>	MAX	UNIT
V <sub>IK</sub>	Input voltage	All inputs	V <sub>DDQ</sub> = 2.3 V, I <sub>I</sub> = –18 mA				–1.2	V
V <sub>OH</sub>	High-level output voltage		V <sub>DDQ</sub> = min to max, I <sub>OH</sub> = –1 mA		V <sub>DDQ</sub> – 0.1			V
			V <sub>DDQ</sub> = 2.3 V, I <sub>OH</sub> = –12 mA		1.7			
V <sub>OL</sub>	Low-level output voltage		V <sub>DDQ</sub> = min to max, I <sub>OL</sub> = 1 mA				0.1	V
			V <sub>DDQ</sub> = 2.3 V, I <sub>OL</sub> = 12 mA				0.6	
V <sub>OD</sub>	Output voltage swing <sup>‡</sup>		Differential outputs are terminated with 120 Ω /C <sub>L</sub> = 14 pF (See Figure 3)		1.1		V <sub>DDQ</sub> – 0.4	V
V <sub>OX</sub>	Output differential cross-voltage <sup>§</sup>				V <sub>DDQ</sub> /2 – 0.1	V <sub>DDQ</sub> /2	V <sub>DDQ</sub> /2 + 0.1	
I <sub>I</sub>	Input current		V <sub>DDQ</sub> = 2.7 V, V <sub>I</sub> = 0 V to 2.7 V				±10	μA
I <sub>OZ</sub>	High-impedance state output current		V <sub>DDQ</sub> = 2.7 V, V <sub>O</sub> = V <sub>DDQ</sub> or GND				±10	μA
I <sub>DDPD</sub>	Power-down current on V <sub>DDQ</sub> + AV <sub>DD</sub>		CLK and $\overline{\text{CLK}}$ = 0 MHz; PWRDWN = Low; Σ of I <sub>DD</sub> and A <sub>I</sub> DD			20	100	μA
A <sub>I</sub> DD	Supply current on AV <sub>DD</sub>		f <sub>O</sub> = 170 MHz			6	8	mA
			f <sub>O</sub> = 200 MHz			8	10	
C <sub>I</sub>	Input capacitance		V <sub>DDQ</sub> = 2.5 V, V <sub>I</sub> = V <sub>DDQ</sub> or GND		2	2.5	3.5	pF

<sup>†</sup> All typical values are at a respective nominal V<sub>DDQ</sub>.

<sup>‡</sup> The differential output signal voltage specifies the differential voltage |V<sub>TR</sub> – V<sub>CP</sub>|, where V<sub>TR</sub> is the true output level and V<sub>CP</sub> is the complementary output level.

<sup>§</sup> The differential cross-point voltage is expected to track variations of V<sub>DDQ</sub> and is the voltage at which the differential signals must be crossing.



**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I <sub>DD</sub>	Dynamic current on V <sub>DDQ</sub>	Without load	f <sub>O</sub> = 170 MHz	120	140	mA
			f <sub>O</sub> = 200 MHz	125	150	
		Differential outputs terminated with 120 Ω/C <sub>L</sub> = 0 pF	f <sub>O</sub> = 170 MHz	220	270	
			f <sub>O</sub> = 200 MHz	230	280	
		Differential outputs terminated with 120 Ω/C <sub>L</sub> = 14 pF	f <sub>O</sub> = 170 MHz	280	330	
			f <sub>O</sub> = 200 MHz	300	350	
ΔC	Part-to-part input capacitance variation	V <sub>DDQ</sub> = 2.5 V, V <sub>I</sub> = V <sub>DDQ</sub> or GND			1	pF
C <sub>I(Δ)</sub>	Input capacitance difference between CLK and CKB, FBIN, and FBINB	V <sub>DDQ</sub> = 2.5 V, V <sub>I</sub> = V <sub>DDQ</sub> or GND			0.25	pF

† All typical values are at a respective nominal V<sub>DDQ</sub>.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature**

		MIN	MAX	UNIT
f <sub>CLK</sub>	Operating clock frequency	60	220	MHz
	Application clock frequency	90	220	
Input clock duty cycle		40%	60%	
Stabilization time† (PLL mode)			10	μs
Stabilization time‡ (bypass mode)			30	ns

† The time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK and V<sub>DD</sub> must be applied. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

‡ A recovery time is required when the device goes from power-down mode into bypass mode (AVDD at GND).

**switching characteristics**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> §	Low-to-high level propagation delay time	Test mode/CLK to any output		3.5		ns
t <sub>PHL</sub> §	High-to-low level propagation delay time	Test mode/CLK to any output		3.5		ns
t <sub>jit(per)</sub> ¶	Jitter (period), See Figure 7	100 MHz (PC1600)	-65		65	ps
		133/167/200 MHz (PC2100/2700/3200)	-30		30	
t <sub>jit(cc)</sub> ¶	Jitter (cycle-to-cycle), See Figure 4	100 MHz (PC1600)	-50		50	ps
		133/167/200 MHz (PC2100/2700/3200)	-35		35	
t <sub>jit(hper)</sub> ¶	Half-period jitter, See Figure 8	100 MHz (PC1600)	-100		100	ps
		133/167/200 MHz (PC2100/2700/3200)	-75		75	
t <sub>slr(o)</sub>	Output clock slew rate, See Figure 9	Load: 120 Ω/14 pF		1	2	V/ns
t(∅)	Static phase offset, See Figure 5	100/133/167/200 MHz		-50	50	ps
t <sub>sk(o)</sub>	Output skew, See Figure 6	Load: 120 Ω/14 pF	100/133/167/200 MHz		40	ps

§ Refers to the transition of the noninverting output.

¶ This parameter is assured by design but can not be 100% production tested.

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## PARAMETER MEASUREMENT INFORMATION

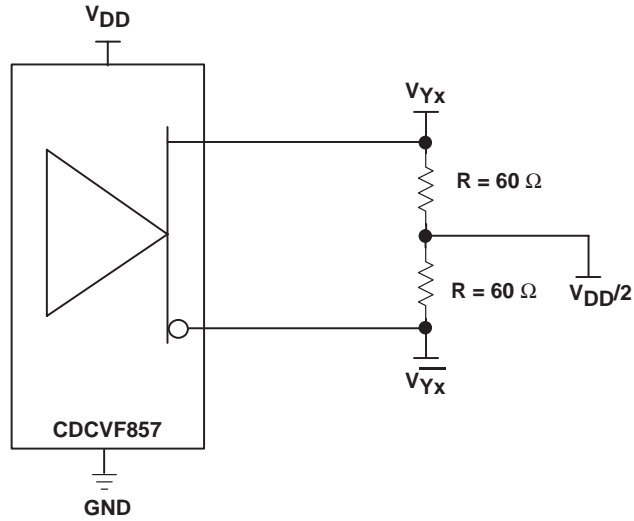


Figure 1. IBIS Model Output Load

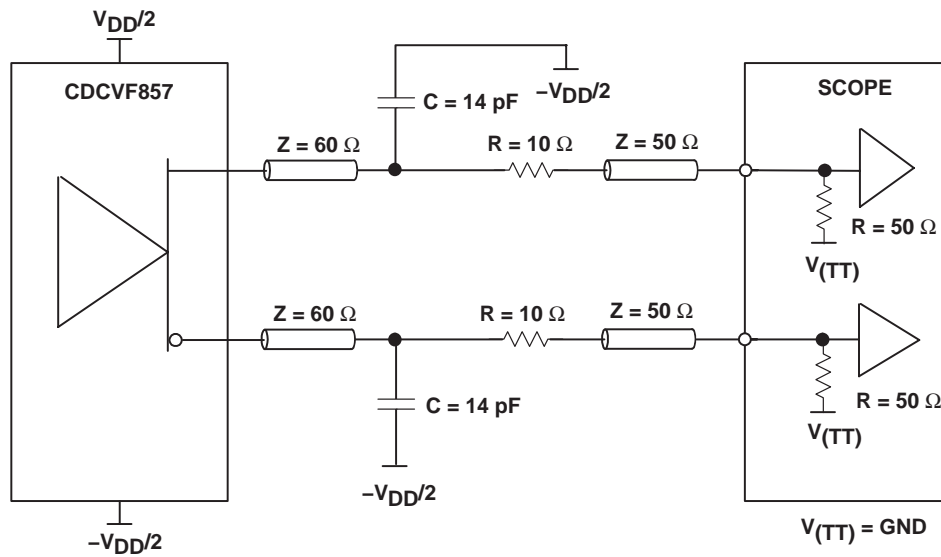
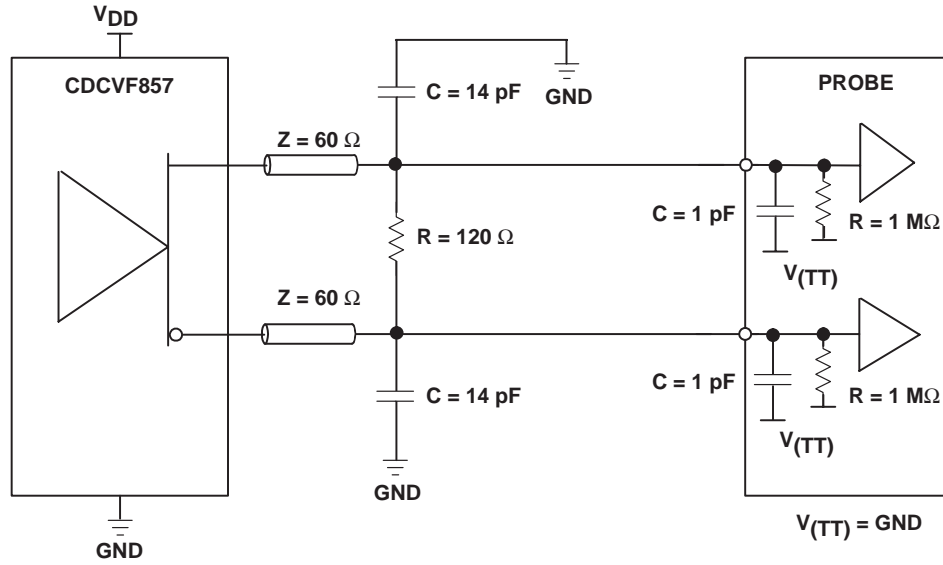
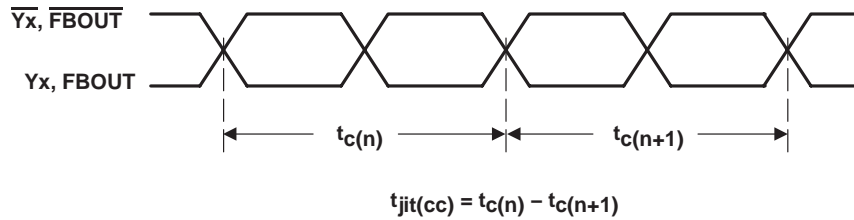


Figure 2. Output Load Test Circuit



**Figure 3. Output Load Test Circuit for Crossing Point**



**Figure 4. Cycle-to-Cycle Jitter**

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### PARAMETER MEASUREMENT INFORMATION

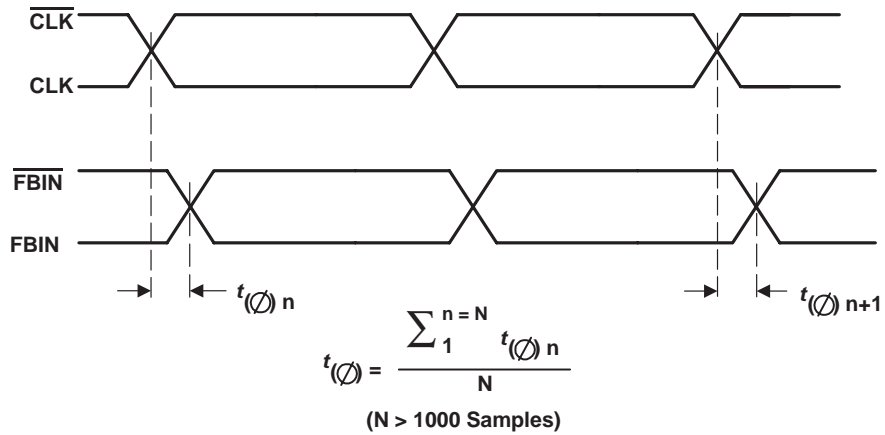


Figure 5. Phase Offset

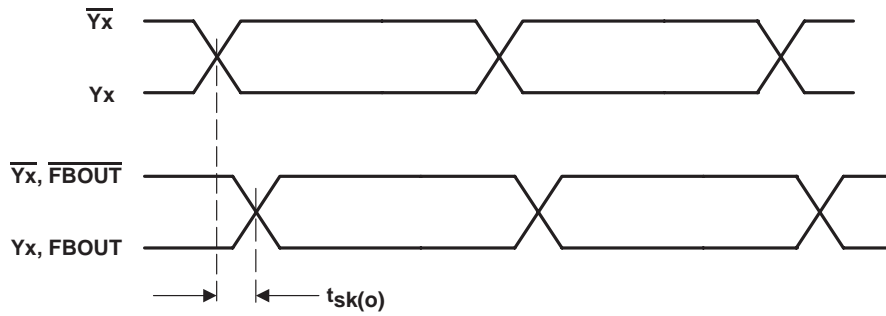


Figure 6. Output Skew

PARAMETER MEASUREMENT INFORMATION

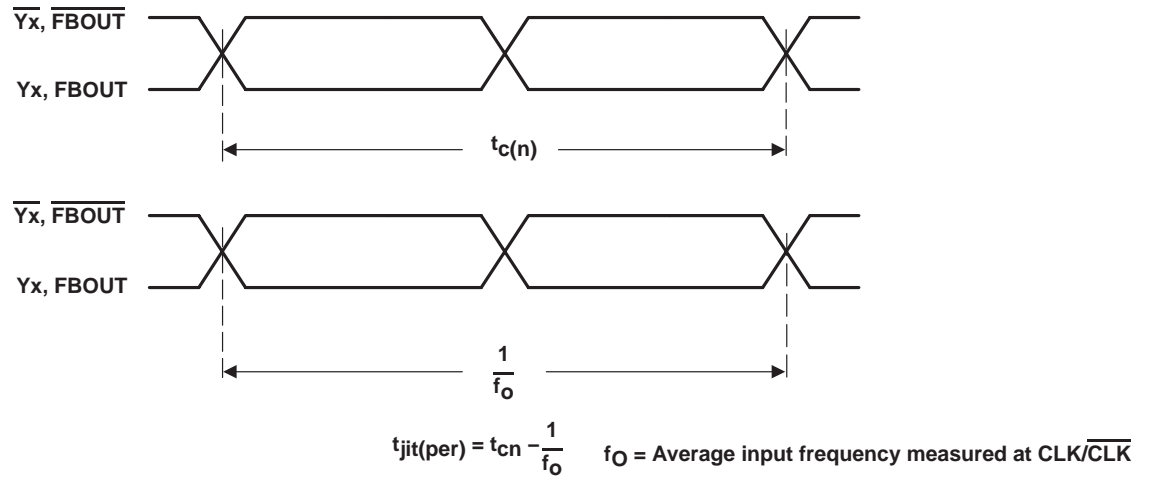


Figure 7. Period Jitter

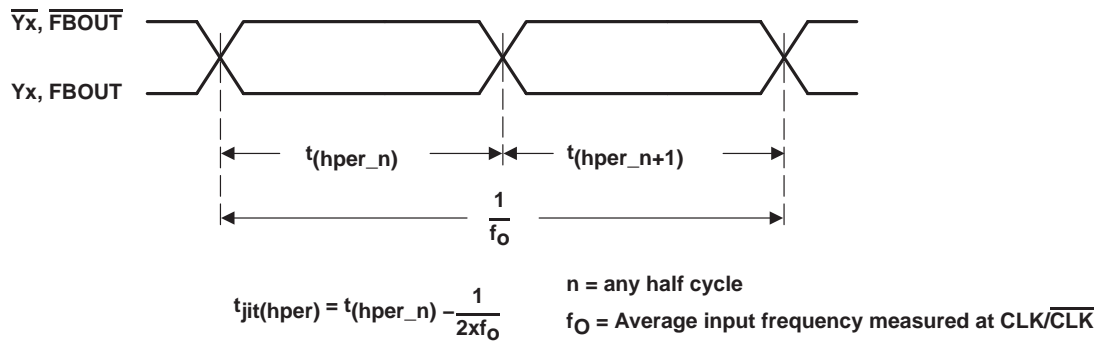


Figure 8. Half-Period Jitter

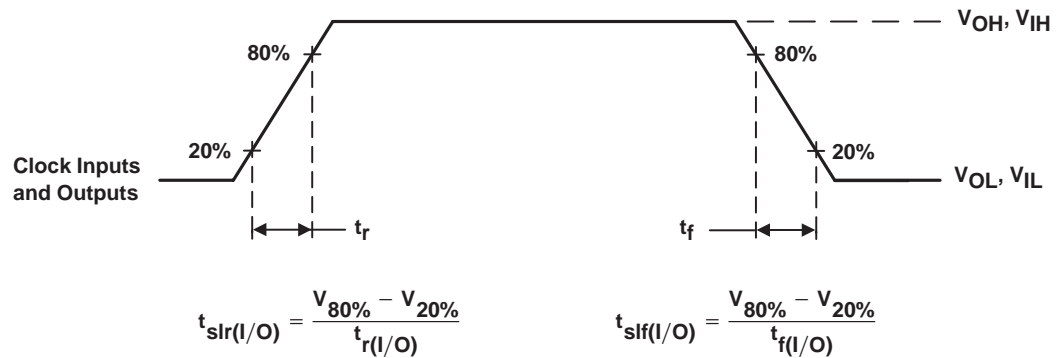
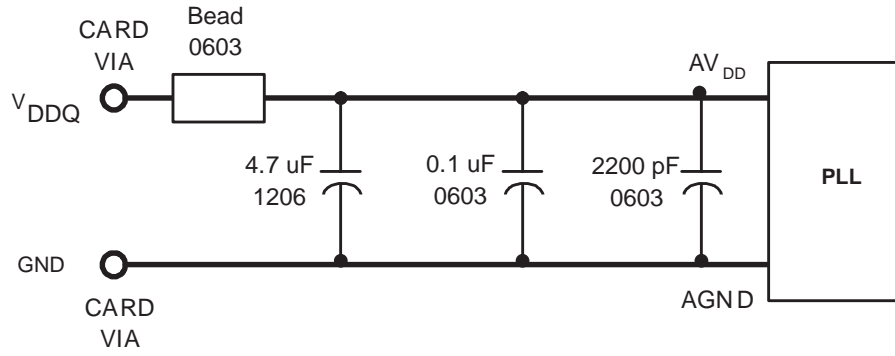


Figure 9. Input and Output Slew Rates

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See Notes 9, 10, and 11

**Figure 10. Recommended AV<sub>DD</sub> Filtering**

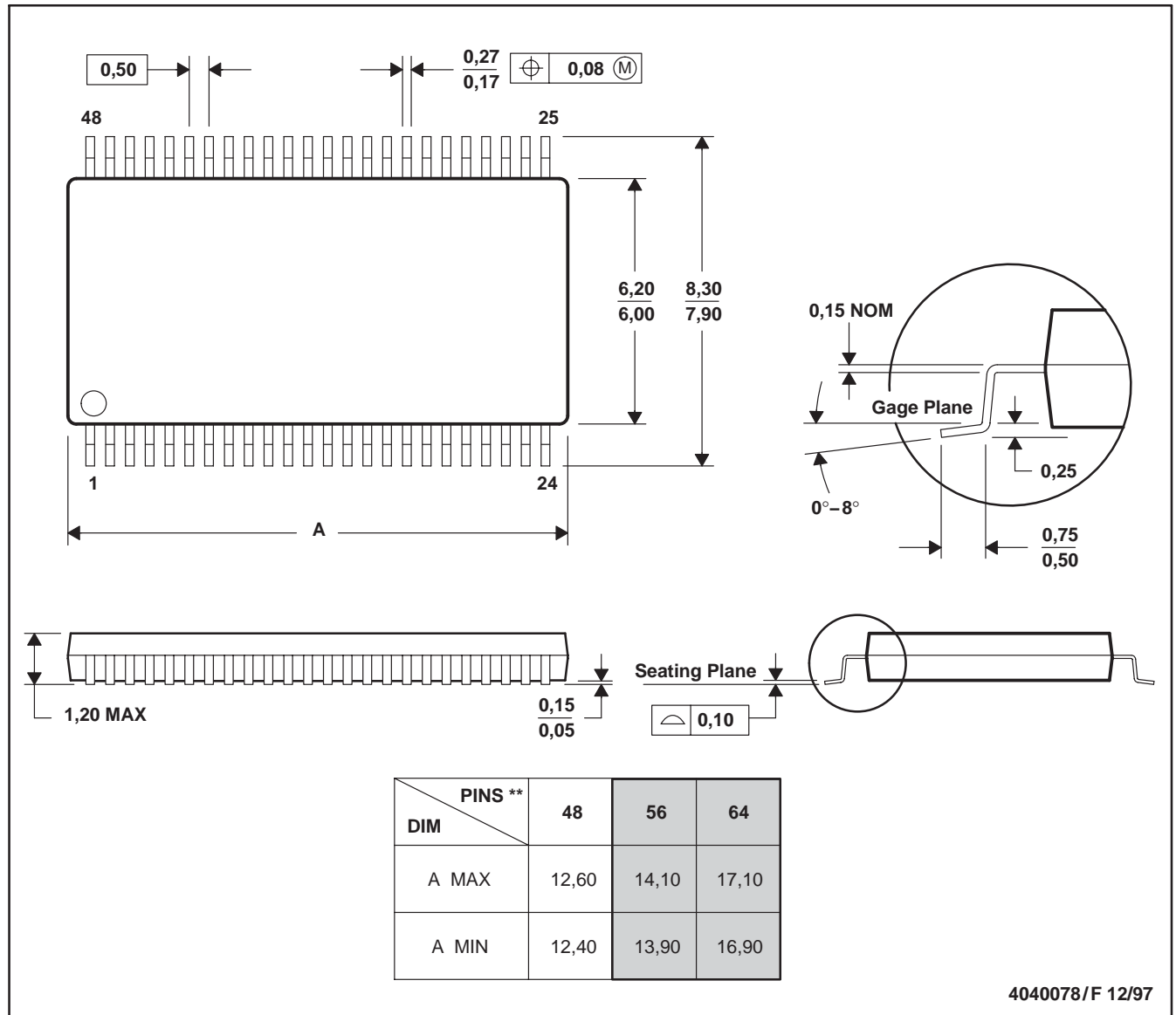
- NOTES:
- 9. Place the 2200-pF capacitor close to the PLL.
  - 10. Use a wide trace for the PLL analog power and ground. Connect PLL and capacitors to AGND trace and connect trace to one GND via (farthest from the PLL).
  - 11. Recommended bead: Fair-Rite P/N 2506036017Y0 or equivalent (0.8  $\Omega$  dc maximum, 600  $\Omega$  at 100 MHz).

**MECHANICAL DATA**

**DGG (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**



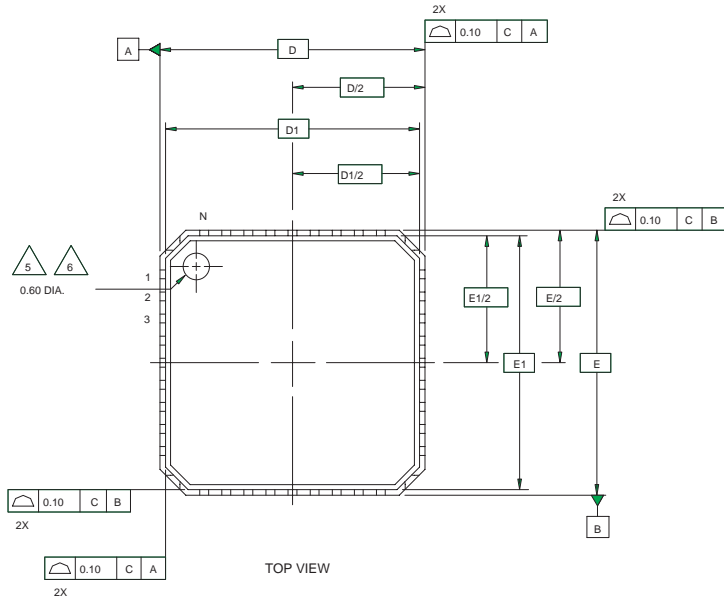
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

# CDCVF857 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

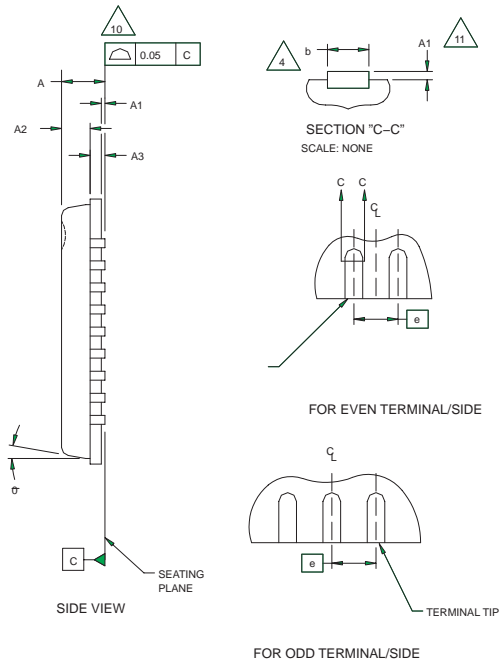
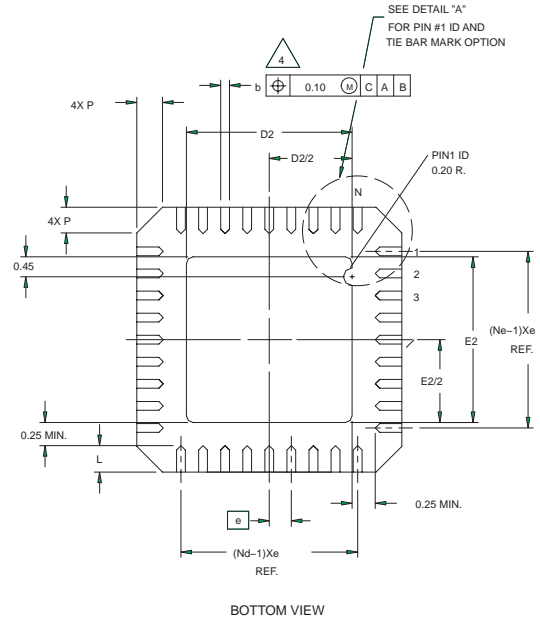
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## MECHANICAL DATA

### RTB (MLF2-N40)



### HIGH-DENSITY MATRIX LEADFRAME



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.85	0.90	
A1	0.00	0.01	0.05	D
A2	–	0.65	0.80	
A3	0.20 REF.			
D	6.00 BSC			
D1	5.75 BSC			
E	6.00 BSC			
E1	5.75 BSC			
ϕ			12	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	C

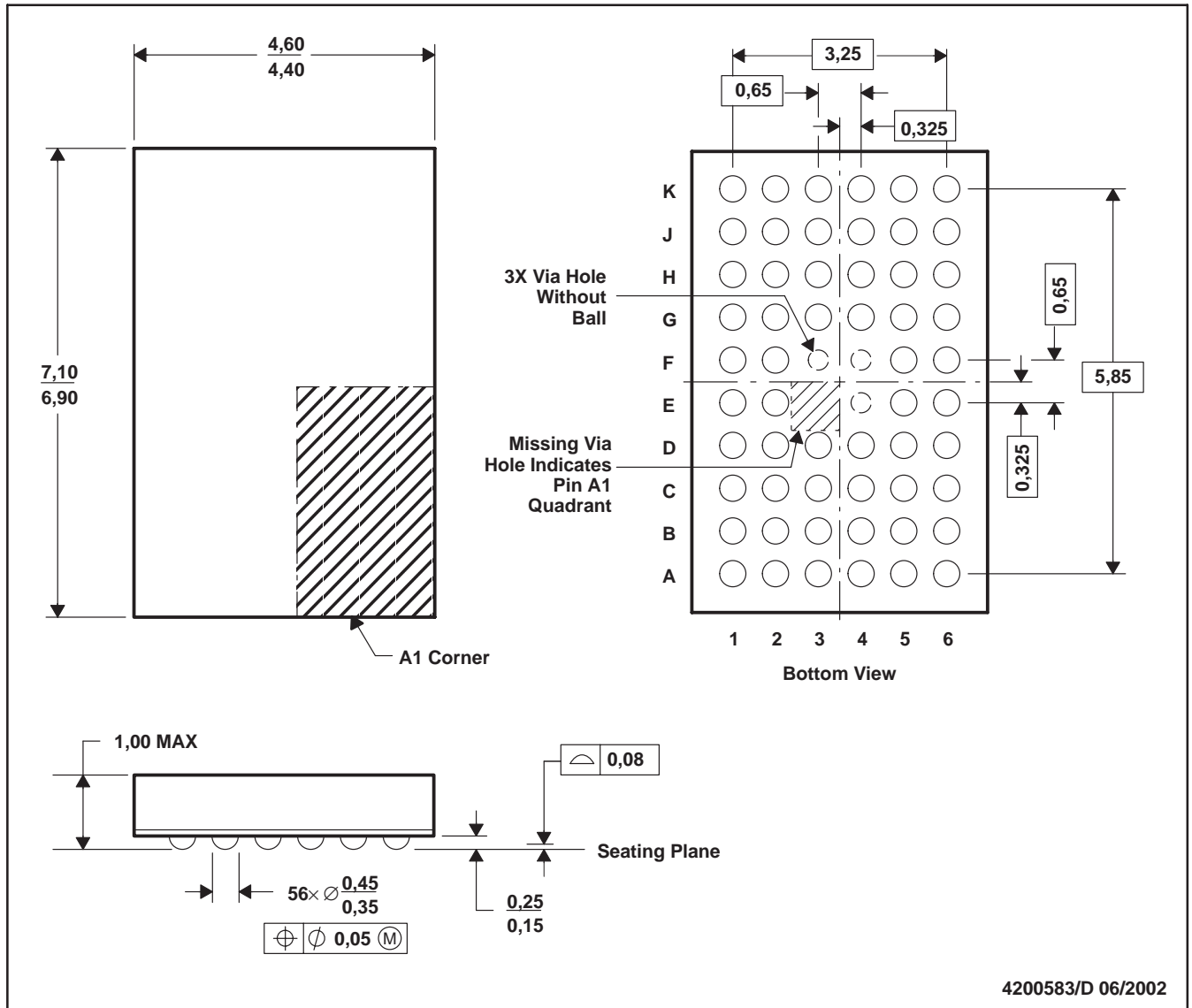
SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e	0.50 BSC			
N	40			A
Nd	10			A
Ne	10			A
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	B
Q	0.00	0.20	0.45	C
D2	2.75	2.90	3.05	
E2	2.75	2.90	3.05	

- NOTES:
- N is the number of terminals
  - Dimension b applies to the plated terminal and is measured
  - Q and R apply only for the straight tiebar shapes.
  - Applied only for terminals
  - 40-pin HP-VFQFP-N, 6.0 × 6.0 mm body size, 0.5-mm pitch, variation VJJD-2, E2 & D2 = 2.9 mm ±0.15 mm

MECHANICAL DATA

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - MicroStar Junior™ BGA configuration
  - Falls within JEDEC MO-225 variation BA.
  - This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CDCVF857DGG	ACTIVE	TSSOP	DGG	48	40	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CDCVF857DGGR	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CDCVF857GQLR	ACTIVE	VFBGA	GQL	56	1000	None	Call TI	Level-2A-220C-4 WKS
CDCVF857RTBR	ACTIVE	QFN	RTB	40	2500	None	CU SNPB	Level-3-235C-168 HR
CDCVF857RTBT	ACTIVE	QFN	RTB	40	250	None	CU SNPB	Level-3-235C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

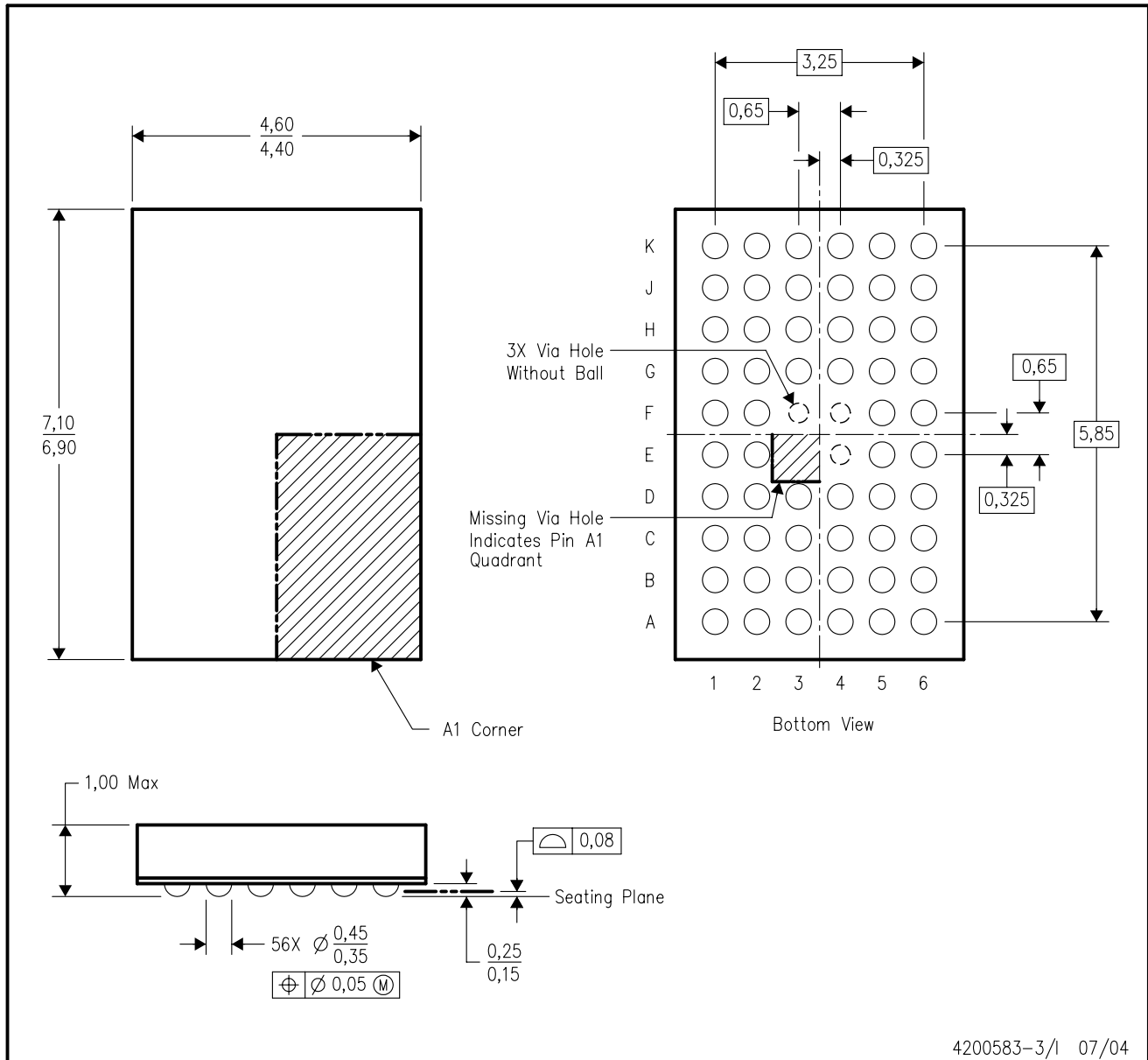
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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GQL (R-PBGA-N56)

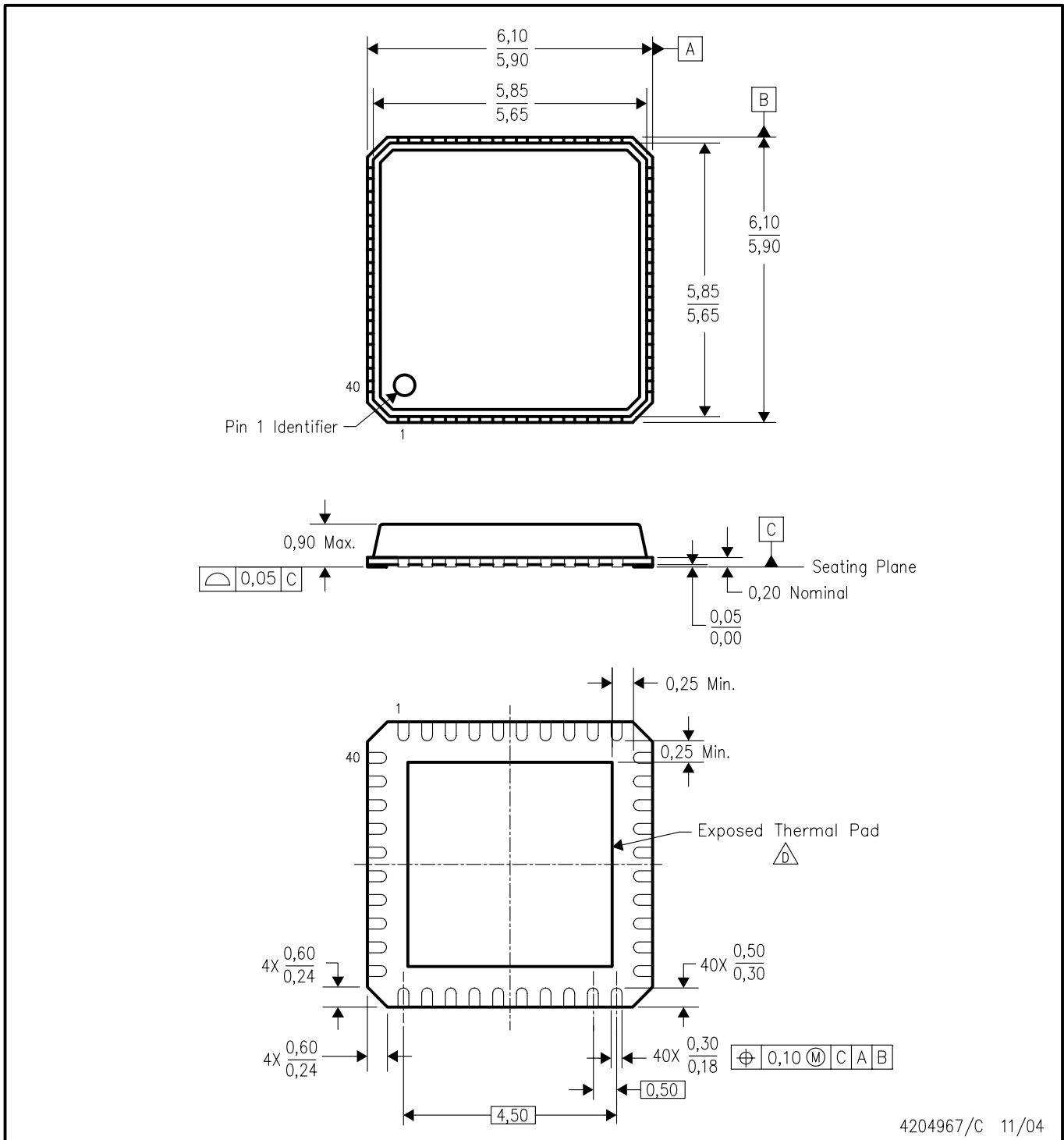
PLASTIC BALL GRID ARRAY




- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BA.
  - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

RTB (S-PQFP-N40)

PLASTIC QUAD FLATPACK



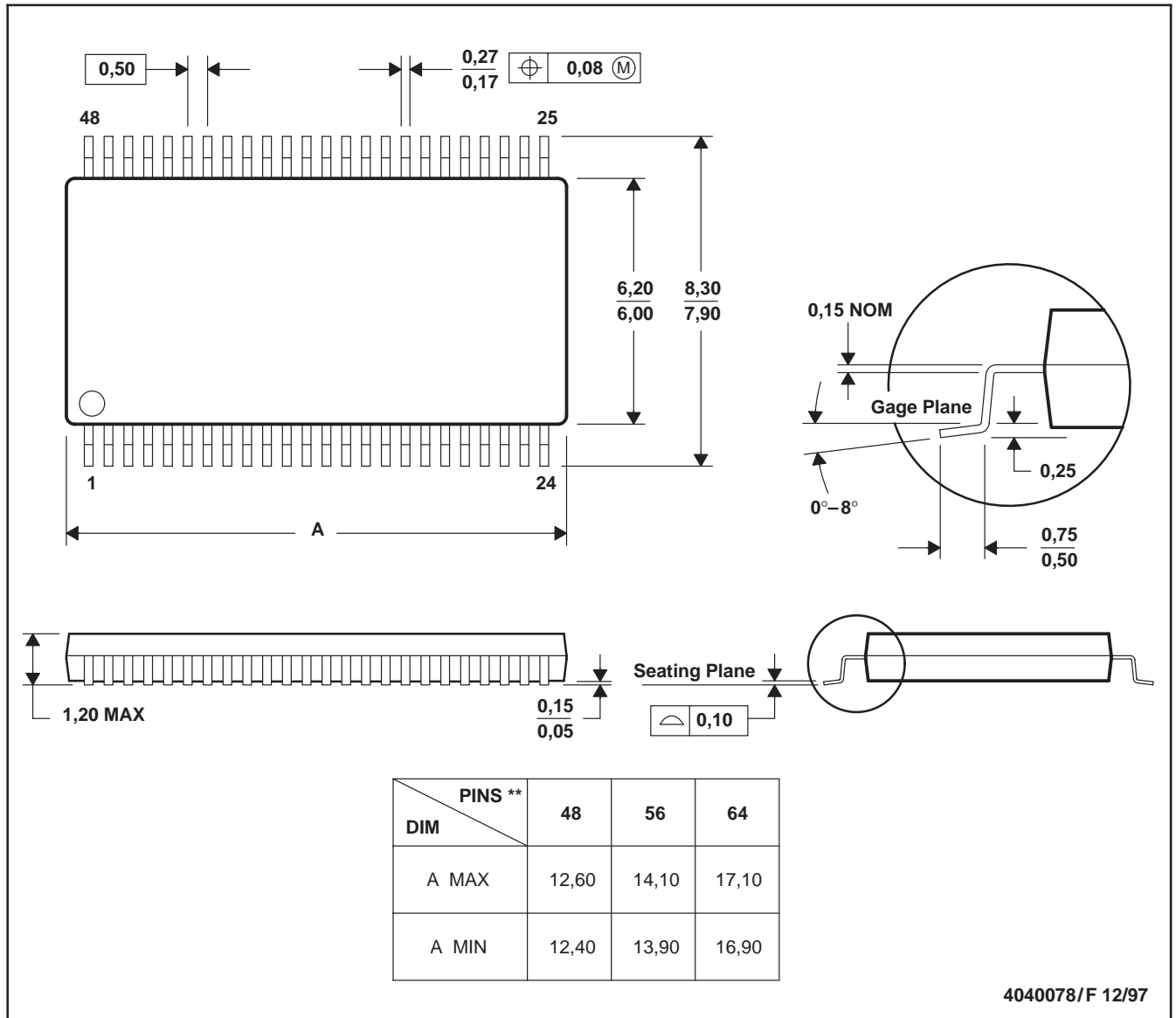
4204967/C 11/04

- NOTES: A. All linear dimensions are in millimeters.  
 Dimensioning and tolerancing per ASME Y14.5M-1994.  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.  
 B. This drawing is subject to change without notice.  
 C. QFN (Quad Flatpack No-Lead) Package configuration.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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