PRECISION, LOW POWER INSTRUMENTATION AMPLIFIERS

Check for Samples: INA128-HT, INA129-HT

FEATURES (1)

- **Low Offset Voltage**
- **Low Input Bias Current: 50 nA Typ**
- **High CMR: 95 dB Typ**
- **Inputs Protected to ±40 V**
- **Wide Supply Range: ±2.25 V to ±18 V**
- **Low Quiescent Current: 2 mA Typ**

APPLICATIONS

- **Bridge Amplifier**
- **Thermocouple Amplifier**
- **RTD Sensor Amplifier**
- **Medical Instrumentation**
- **Data Acquisition**

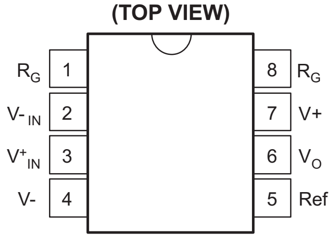
(1) Typical values for 210°C application

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

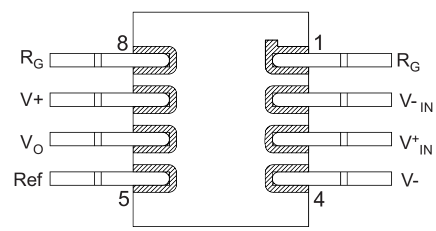
- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/210°C) Temperature Range (2)**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments' high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

(2) Custom temperature ranges available

D, JD OR HKJ PACKAGE (TOP VIEW)



HKQ PACKAGE (TOP VIEW)



HKQ as formed or HKJ mounted dead bug

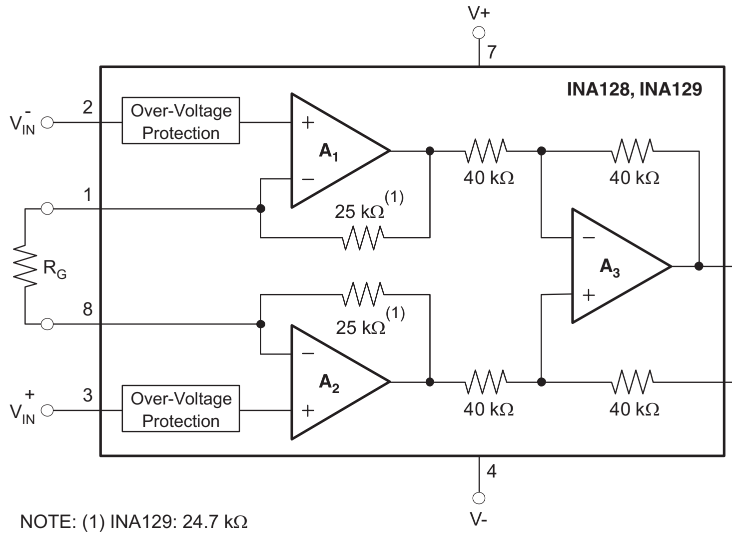
DESCRIPTION

The INA128 and INA129 are low power, general purpose instrumentation amplifiers offering excellent accuracy. The versatile three operational amplifier design and small size make them ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain.

A single external resistor sets any gain from 1 to 10,000. The INA128 provides an industry-standard gain equation; the INA129 gain equation is compatible with the AD620.

The INA128/INA129 is laser trimmed for very low offset voltage (50 μV) and high common-mode rejection (93 dB at G ≥ 100). It operates with power supplies as low as ±2.25 V, and quiescent current of 2 mA - typically. Internal input protection can withstand up to ±40 V without damage.

The INA129 is available in 8-pin ceramic DIP and 8-pin ceramic surface-mount packages, specified for the –55°C to 210°C temperature range. The INA128 is available in an 8-pin SO-8 surface-mount package, specified for the –55°C to 175°C temperature range.



INA128:

$$G = 1 + \frac{50\ k\Omega}{R_G}$$

INA129:

$$G = 1 + \frac{49.4\ k\Omega}{R_G}$$

ORDERING INFORMATION

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 210°C	HKJ	INA129SHKJ	INA129SHKJ
	HKQ	INA129SHKQ	INA129SHKQ
	KGD	INA129SKGD1	NA
	JD	INA129SJD	INA129SJD
–55°C to 175°C	D	INA128HD	128HD

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils	Silicon with backgrind	GND	Al-Si-Cu (0.5%)

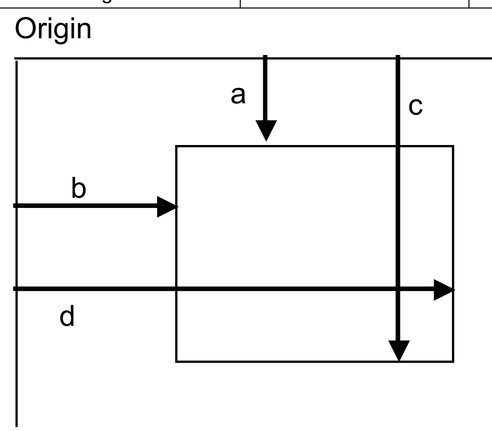
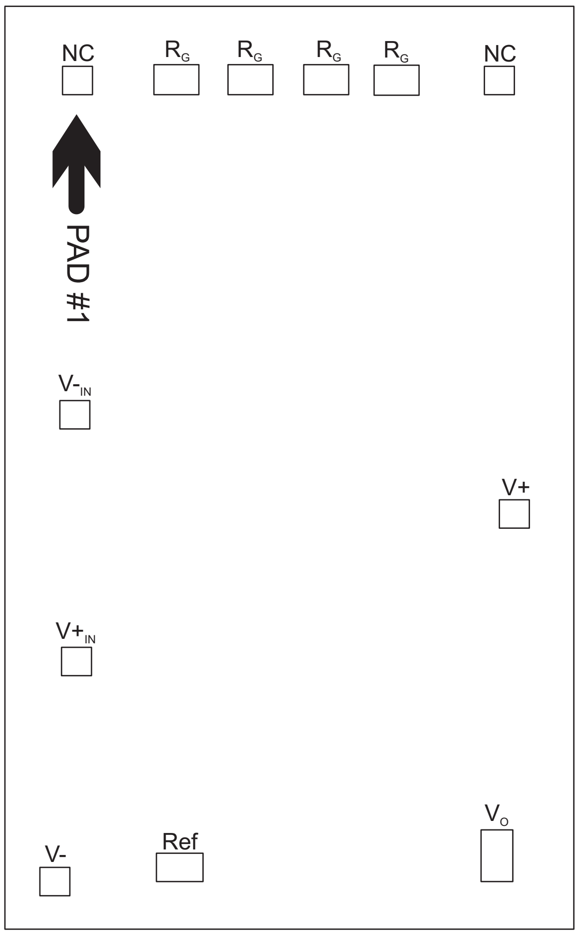


Table 1. Bond Pad Coordinates in Mils

DESCRIPTION	PAD NUMBER	a	b	c	d
NC	1	-57.4	-31.1	-53.3	-27
$V-_{IN}$	2	-9.85	-31.4	-5.75	-27.3
$V+_{IN}$	3	25.05	-31.4	29.15	-27.3
V-	4	56.2	-34.3	60.3	-30.2
Ref	5	53.75	-17.6	57.85	-11
V_O	6	50.35	27.8	56.95	31.9
V+	7	7.75	30.2	11.85	34.3
NC	8	-57.4	28.4	-53.3	32.5
R_G (1)	9	-57.4	13.4	-53.3	20
R_G (1)	10	-57.5	2.7	-53.4	9.3
R_G (1)	11	-57.5	-7.9	-53.4	-1.3
R_G (1)	12	-57.4	-18.6	-53.3	-12

(1) Pads 9 and 10 must both be bonded to a common point and correspond to package pin 8. Pads 11 and 12 must both be bonded to a common point and correspond to package pin 1.



ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_S	Supply voltage		±18	V
	Analog input voltage range		±40	V
	Output short-circuit (to ground)		Continuous	
T_A	Operating temperature	HKJ, HKQ, KGD and JD packages	–55 to 210	°C
		D package	–55 to 175	
T_{STG}	Storage temperature range	HKJ, HKQ, KGD and JD packages	–55 to 210	°C
		D package	–55 to 175	
	Lead temperature (soldering, 10s)		300	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

THERMAL CHARACTERISTICS FOR D PACKAGE

THERMAL METRIC[1]		INA128 D 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	110	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	57	
θ_{JB}	Junction-to-board thermal resistance[4]	54	
ψ_{JT}	Junction-to-top characterization parameter[5]	11	
ψ_{JB}	Junction-to-board characterization parameter[6]	53	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

THERMAL CHARACTERISTICS FOR JD PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance[1]	High-K board[2], no airflow		64.9		°C/W
		No airflow		83.4		
θ_{JB}	Junction-to-board thermal resistance	High-K board without underfill		27.9		°C/W
θ_{JC}	Junction-to-case thermal resistance			6.49		°C/W

(1) The intent of θ_{JA} specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.
(2) JED51-7, high effective thermal conductivity test board for leaded surface mount packages

THERMAL CHARACTERISTICS FOR HKJ OR HKQ PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance	to ceramic side of case			5.7	°C/W
		to top of case lid (metal side of case)			13.7	

ELECTRICAL CHARACTERISTICS FOR INA128

T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 175°C(1)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
OFFSET VOLTAGE, RTI								
Initial	T_A = 25°C		±25 ±100/G	±125 ±1000/G				µV
vs temperature	T_A = T_{MIN} to T_{MAX}		±0.2 ±5/G	±1 ±20/G			±3.5 ±80/G	µV/°C
vs power supply	V_S = ±2.25 V to ±18 V			±2 ±200/G			±5 ±500/G	µV/V
Long-term stability			±1 ±3/G			±1 ±3/G		µV/mo
Impedance, differential			10^{10} || 2			10^{10} || 2		Ω || pF
Common mode			10^{11}||9			10^{11}||9		Ω || pF
Common mode voltage range(2)	V_O = 0 V	(V+) − 2	(V+) − 1.4		(V+) − 2	(V+) − 1.4		V
		(V−) + 2	(V−) + 1.7		(V−) + 2	(V−) + 1.7		V
Safe input voltage				±40			±40	V
Common-mode rejection	V_{CM} = ±13 V, ΔR_S = 1 kΩ							
	G = 1	58	86		58	75		dB
	G = 10	78	106		78	85		
	G = 100	99	125		99	110		
	G = 1000	113	130		113	120		
CURRENT								
Bias current			±2	±10			±45	nA
vs temperature			±30			±550		pA/°C
Offset Current			±1	±10			±45	nA
vs temperature			±30			±550		pA/°C
NOISE								
Noise voltage, RTI	G = 1000, R_S = 0 Ω							
f = 10 Hz			10			10		nV/√Hz
f = 100 Hz			8			8		nV/√Hz
f = 1 kHz			8			8		nV/√Hz
f_B = 0.1 Hz to 10 Hz			0.2			0.8		μV_{PP}
Noise current								
f = 10 Hz			0.9					pA/√Hz
f = 1 kHz			0.3					pA/√Hz
f_B = 0.1 Hz to 10 Hz			30					pA_{PP}

(1) Minimum and maximum parameters are characterized for operation at T_A = 175°C, but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(2) Input common-mode range varies with output voltage — see typical curves.

ELECTRICAL CHARACTERISTICS FOR INA128 (continued)

T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 175°C(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
GAIN									
Gain equation				1 + (50 kΩ/R_G)			1 + (50 kΩ/R_G)		V/V
Range of gain			1		10000	1		10000	V/V
Gain error		G = 1		±0.01	±0.1		±0.1	±0.5	%
		G = 10		±0.02	±0.5		±0.5	±1	
		G = 100		±0.05	±0.7		±0.7	±1.5	
		G = 1000		±0.5	±2.5		±2	±4	
Gain vs temperature(3)		G = 1		±1	±10		±75		ppm/°C
50-kΩ resistance(3)(4)				±25	±100		±75		ppm/°C
Nonlinearity		V_O = ±13.6 V, G = 1		±0.0001	±0.001			±0.008	% of FSR
		G = 10		±0.0003	±0.002			±0.010	
		G = 100		±0.0005	±0.002			±0.010	
		G = 1000		±0.001	See (5)		±0.6	See (5)	
OUTPUT									
Voltage	Positive	R_L = 10kΩ	(V+) − 1.4	(V+) − 0.9		(V+) − 1.4	(V+) − 0.9		V
	Negative	R_L = 10kΩ	(V−) + 1.4	(V−) + 0.8		(V−) + 1.4	(V−) + 0.8		
Load capacitance stability				1000			1000		pF
Short-curcuit current				+6/−15			+6/−15		mA
FREQUENCY RESPONSE									
Bandwidth, −3 dB		G = 1		1300			1100		kHz
		G = 10		700			700		
		G = 100		200			190		
		G = 1000		20			17.5		
Slew rate		V_O = ±10 V, G = 10		4			4		V/µs
Settling time, 0.01%		G = 1		7			7		µs
		G = 10		7			7		
		G = 100		9			9		
		G = 1000		80			80		
Overload recovery		50% overdrive		4			4		µs
POWER SUPPLY									
Voltage range			±2.25	±15	±18	±2.25	±15	±18	V
Current, total		V_{IN} = 0 V		±0.7	±1			±1	mA
TEMPERATURE RANGE									
Specification			−55		125			175	°C
Operating			−55		125			175	°C

(3) Specified by wafer test.
(4) Temperature coefficient of the 50-kΩ term in the gain equation.
(5) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%.

ELECTRICAL CHARACTERISTICS FOR INA129

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C(1)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
OFFSET VOLTAGE, RTI								
Initial	T_A = 25°C		±25 ±100/G	±125 ±1000/G				µV
vs temperature	$T_A = T_{MIN}$ to T_{MAX}		±0.2 ±5/G	±1 ±20/G		±1 ±850/G		µV/°C
vs power supply	V_S = ±2.25 V to ±18 V		±0.2 ±20/G	±2 ±200/G		±20 ±1000/G		µV/V
Long-term stability			±1 ±3/G			±1 ±3/G		µV/mo
Impedance, differential			10^{10} || 2			10^{10} || 2		Ω || pF
Common mode			10^{11}||9			10^{11}||9		Ω || pF
Common mode voltage range(2)	V_O = 0 V	(V+) − 2	(V+) − 1.4		(V+) − 2	(V+) − 1.4		V
		(V−) + 2	(V−) + 1.7		(V−) + 2	(V−) + 1.7		V
Safe input voltage				±40			±40	V
Common-mode rejection	V_{CM} = ±13 V, ΔR_S = 1 kΩ							
	G = 1	58	86			53		dB
	G = 10	78	106			69		dB
	G = 100	99	125			89		dB
	G = 1000	113	130			95		dB
CURRENT								
Bias current			±2	±10		±50		nA
vs temperature			±30			±600		pA/°C
Offset Current			±1	±10		±50		nA
vs temperature			±30			±600		pA/°C
NOISE								
Noise voltage, RTI	G = 1000, R_S = 0 Ω							
f = 10 Hz			10			25		nV/√Hz
f = 100 Hz			8			20		nV/√Hz
f = 1 kHz			8			20		nV/√Hz
f_B = 0.1 Hz to 10 Hz			0.2			2		$µV_{PP}$
Noise current								
f = 10 Hz			0.9					pA/√Hz
f = 1 kHz			0.3					pA/√Hz
f_B = 0.1 Hz to 10 Hz			30					pA_{PP}

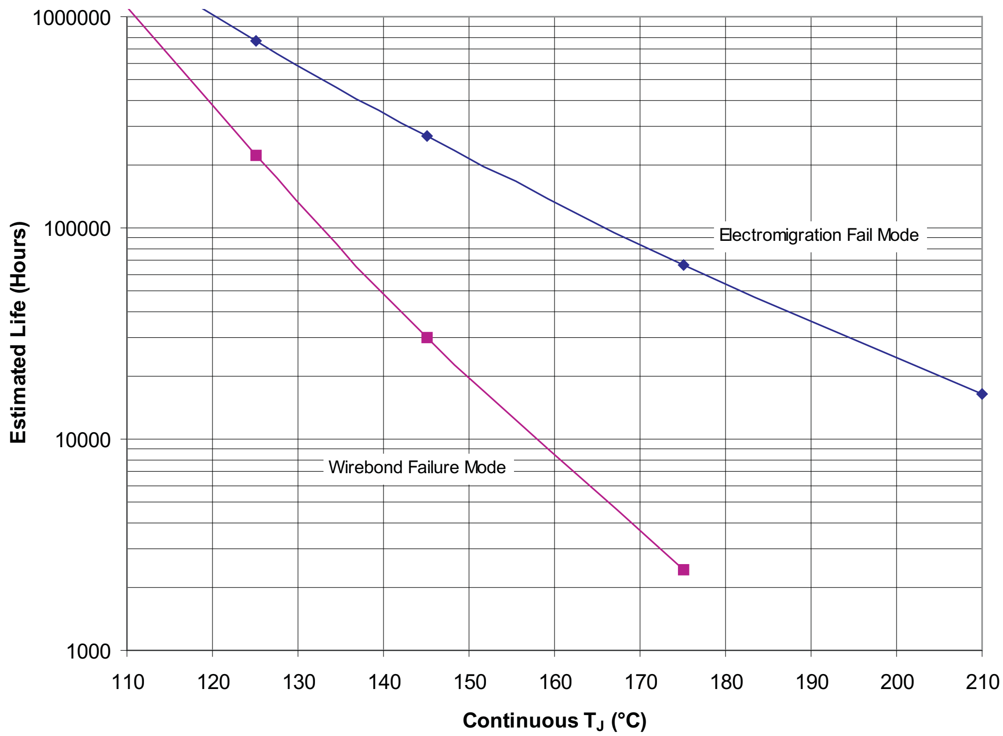
(1) Minimum and maximum parameters are characterized for operation at T_A = 210°C, but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(2) Input common-mode range varies with output voltage — see typical curves.

ELECTRICAL CHARACTERISTICS FOR INA129 (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C MIN	TYP	MAX	T_A = 210°C(1) MIN	TYP	MAX	UNIT
GAIN									
Gain equation				1 + (49.4 kΩ/R_G)			1 + (49.4 kΩ/R_G)		V/V
Range of gain			1		10000	1		10000	V/V
Gain error		G = 1		±0.01	±0.1		±1.1		%
		G = 10		±0.02	±0.5		±2.6		
		G = 100		±0.05	±0.7		±13.5		
		G = 1000		±0.5	±2.5		±65.5		
Gain vs temperature(3)		G = 1		±1	±10		±100		ppm/°C
49.4-kΩ resistance(3)(4)				±25	±100		±100		ppm/°C
Nonlinearity		V_O = ±13.6 V, G = 1		±0.0001	±0.001		±0.1		% of FSR
		G = 10		±0.0003	±0.002		±0.2		
		G = 100		±0.0005	±0.002		±0.7		
		G = 1000		±0.001	See (5)		±2.4	See (5)	
OUTPUT									
Voltage	Positive	R_L = 10kΩ	(V+) − 1.4	(V+) − 0.9		(V+) − 1.4	(V+) − 0.9		V
	Negative	R_L = 10kΩ	(V−) + 1.4	(V−) + 0.8		(V−) + 1.4	(V−) + 0.8		
Load capacitance stability				1000			1000		pF
Short-curcuit current				+6/−15			+12/−5		mA
FREQUENCY RESPONSE									
Bandwidth, −3 dB		G = 1		1300			850		kHz
		G = 10		700			400		
		G = 100		200			50		
		G = 1000		20			7.5		
Slew rate		V_O = ±10 V, G = 10		4			4		V/µs
Settling time, 0.01%		G = 1		7			10		µs
		G = 10		7			10		
		G = 100		9			30		
		G = 1000		80			150		
Overload recovery		50% overdrive		4			4		µs
POWER SUPPLY									
Voltage range			±2.25	±15	±18	±2.25	±15	±18	V
Current, total		V_{IN} = 0 V		±0.7	±1		±2		mA
TEMPERATURE RANGE									
Specification			−55		125			210	°C
Operating			−55		125			210	°C

(3) Specified by wafer test.
(4) Temperature coefficient of the 49.4-kΩ term in the gain equation.
(5) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%.



(1) See the data sheet for absolute maximum and minimum recommended operating conditions.

(2) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characterisitics.

(3) Wirebond lifetime is only applicable for D package.

Figure 1. INA128HD/INA129SKGD1 Operating Life Derating Chart

TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

GAIN vs FREQUENCY

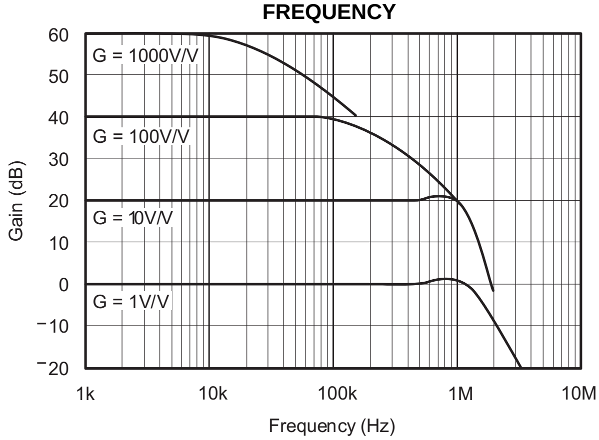


Figure 2.

COMMON-MODE REJECTION vs FREQUENCY

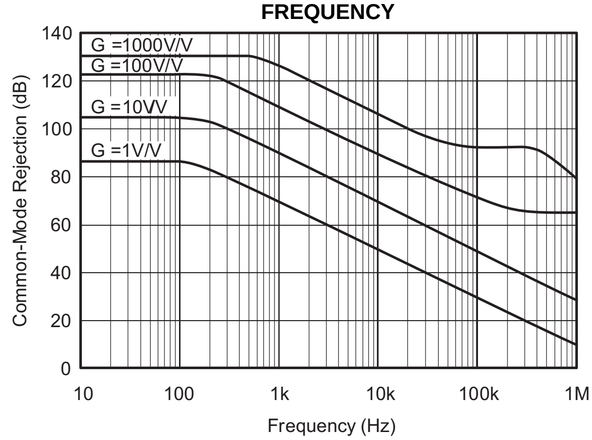


Figure 3.

POSITIVE POWER SUPPLY REJECTION vs FREQUENCY

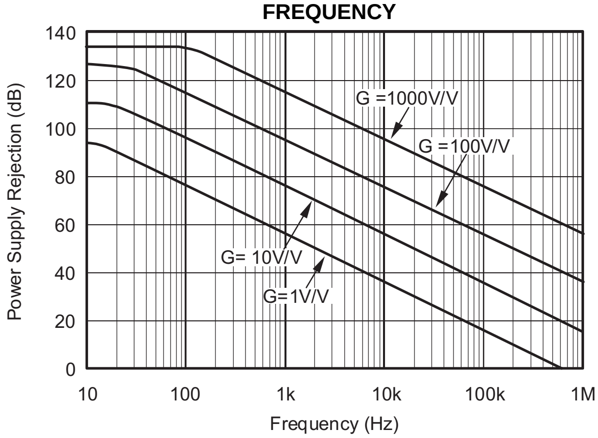


Figure 4.

NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY

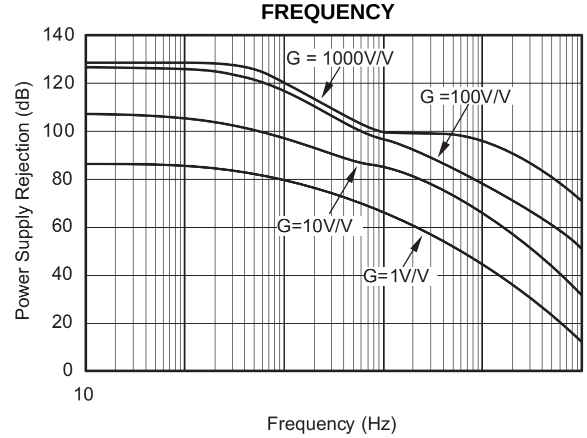


Figure 5.

INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE (V_S = ±15 V)

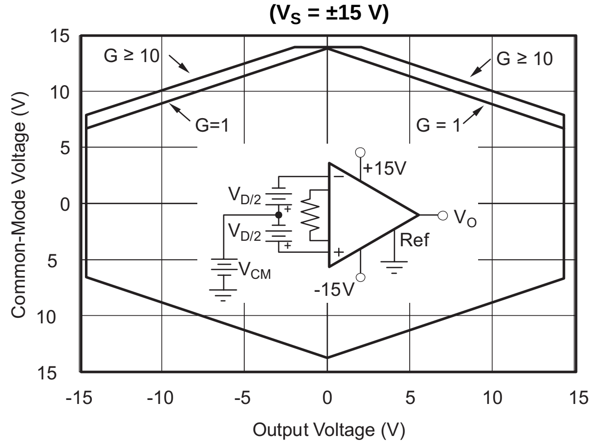


Figure 6.

INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE (V_S = ±5 V, ±2.5 V)

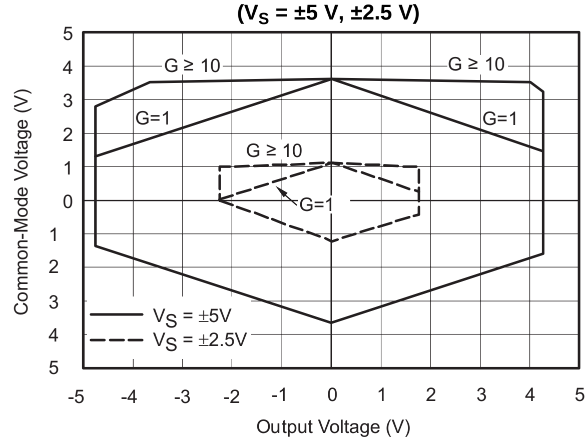


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

INPUT-REFERRED NOISE vs FREQUENCY

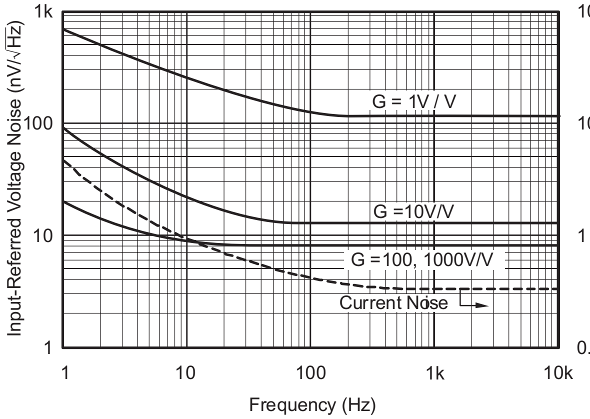


Figure 8.

SETTLING TIME vs GAIN

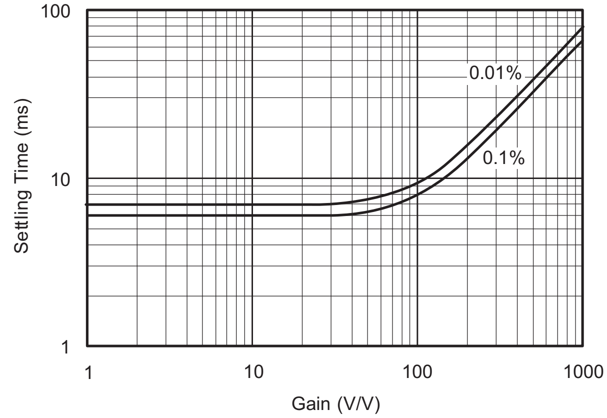


Figure 9.

QUIESCENT CURRENT AND SLEW RATE vs TEMPERATURE

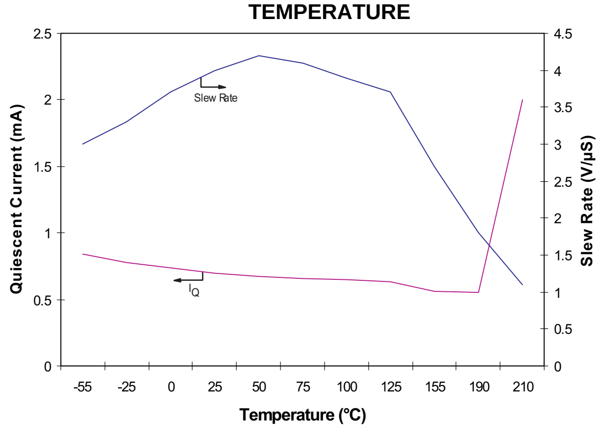


Figure 10.

INPUT OVER-VOLTAGE V/I CHARACTERISTICS

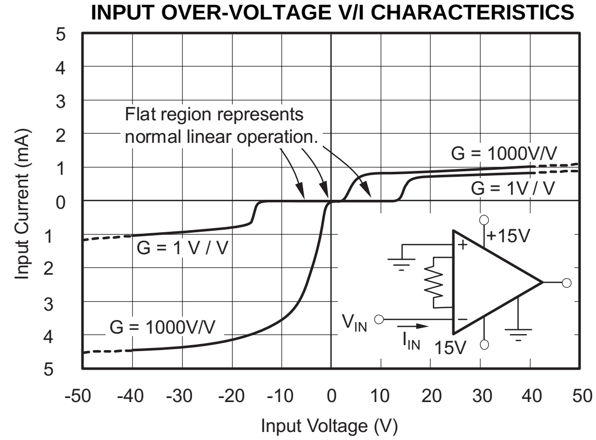


Figure 11.

INPUT OFFSET VOLTAGE WARM-UP

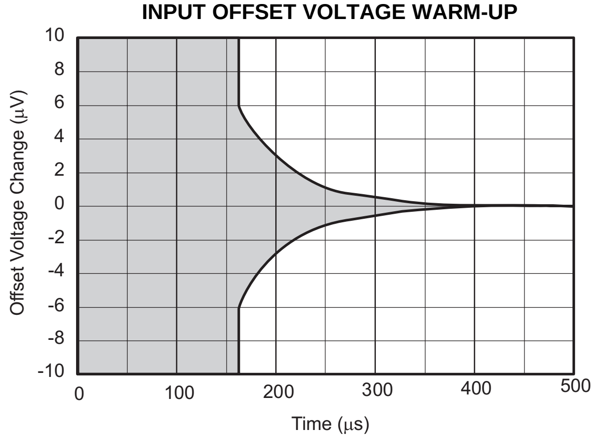


Figure 12.

INPUT BIAS CURRENT vs TEMPERATURE

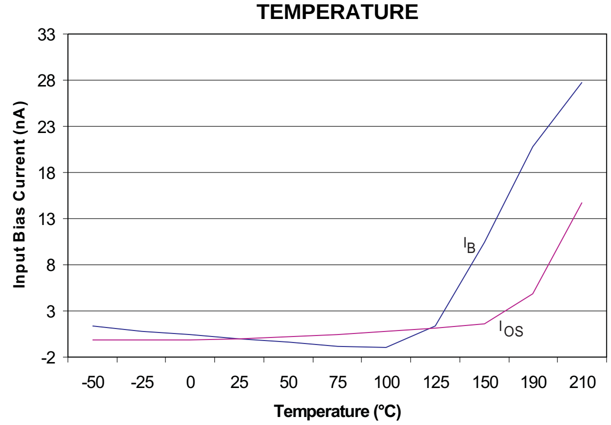


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

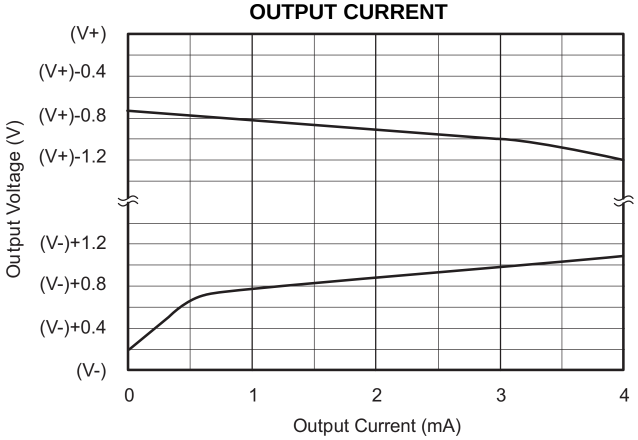


Figure 14.

OUTPUT VOLTAGE SWING vs POWER SUPPLY VOLTAGE

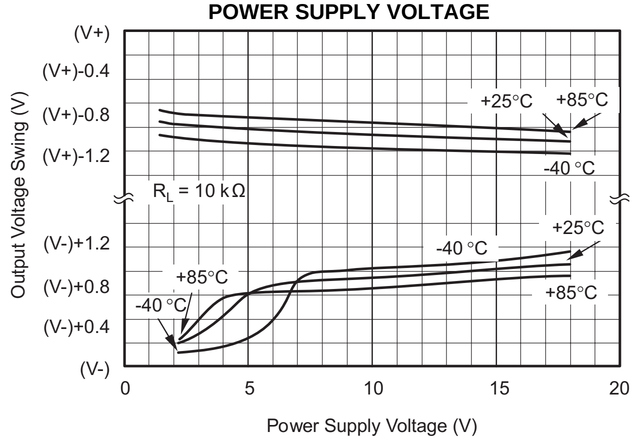


Figure 15.

SHORT-CIRCUIT OUTPUT CURRENT vs TEMPERATURE

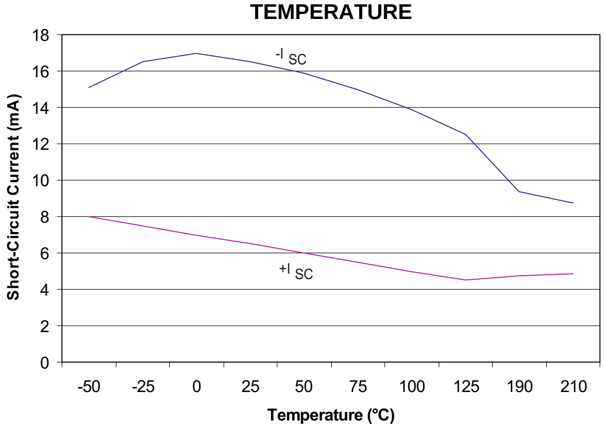


Figure 16.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

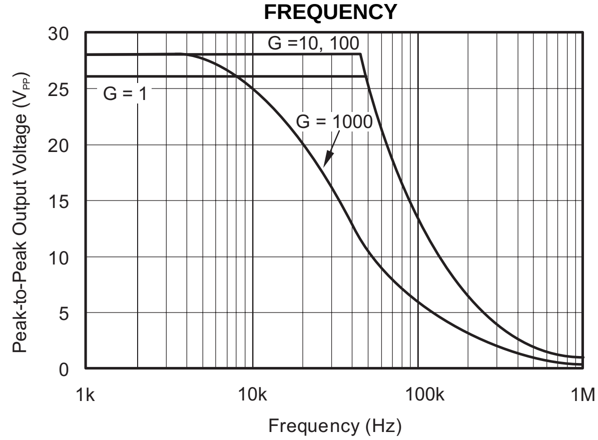


Figure 17.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

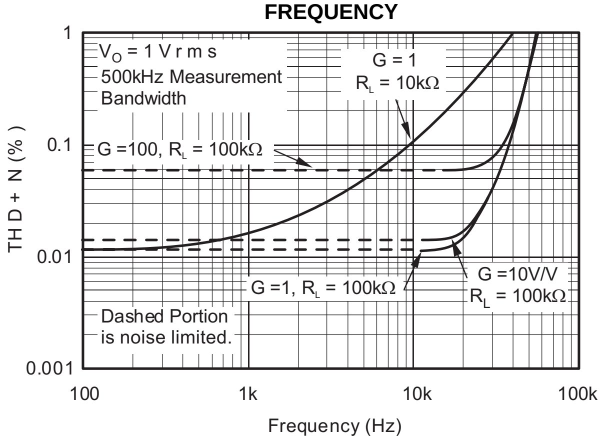


Figure 18.

SMALL SIGNAL (G = 1, 10)

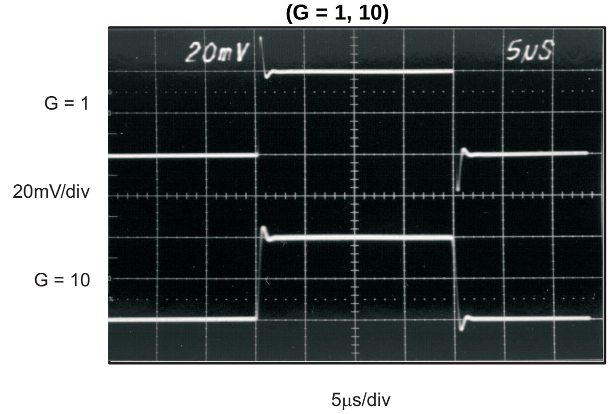


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

SMALL SIGNAL (G = 100, 1000)

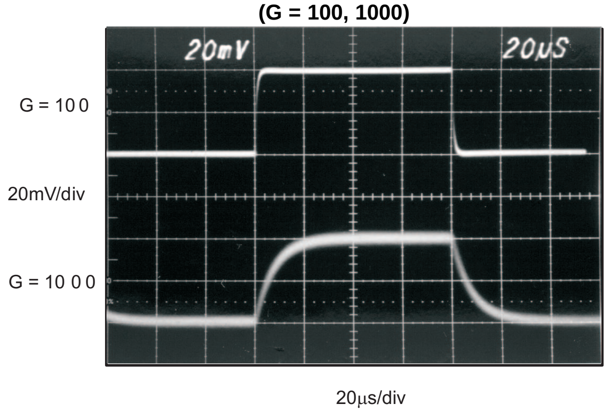


Figure 20.

LARGE SIGNAL (G = 1, 10)

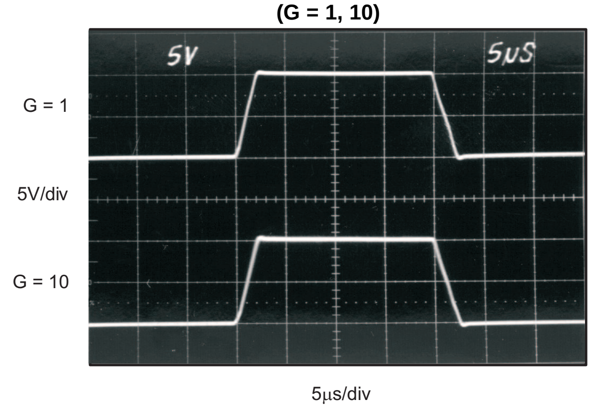


Figure 21.

LARGE SIGNAL (G = 100, 1000)

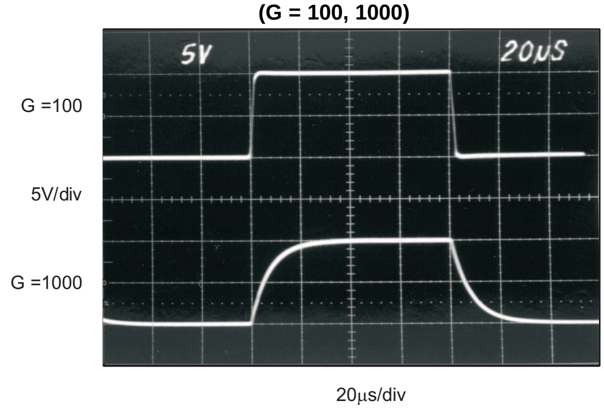


Figure 22.

VOLTAGE NOISE 0.1 Hz TO 10 Hz INPUT-REFERRED, G ≥ 100

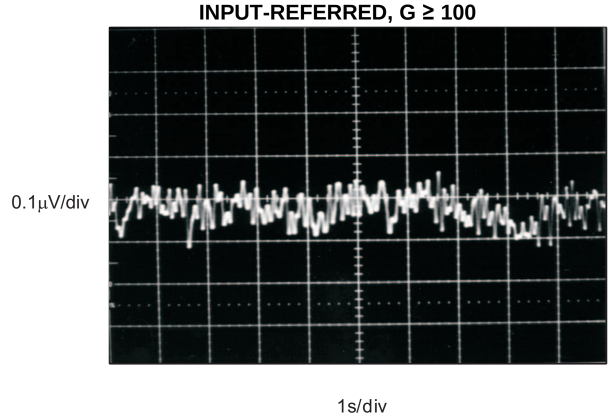


Figure 23.

APPLICATION INFORMATION

Figure 24 shows the basic connections required for operation of the INA128/INA129. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8 Ω in series with the Ref pin will cause a typical device to degrade.

Setting the Gain

Gain is set by connecting a single external resistor, R_G, between pins 1 and 8.

INA128:

$$G = 1 + \frac{50\ \text{k}\Omega}{R_G} \tag{1}$$

INA129:

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_G} \tag{2}$$

Commonly used gains and resistor values are shown in Figure 24.

The 50-kΩ term in Equation 1 (49.4-kΩ in Equation 2) comes from the sum of the two internal feedback resistors of A1 and A2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these internal resistors are included in the gain accuracy and drift specifications of the INA128/INA129.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from Equation 2. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

INA128: $G = 1 + \frac{50\ \text{k}\Omega}{R_G}$ INA129: $G = 1 + \frac{49.4\text{k}\Omega}{R_G}$

DESIRED GAIN (V/V)	INA128 R_G (Ω)	INA128 NEAREST 1% R_G (Ω)	INA129 R_G (Ω)	INA129 NEAREST 1% R_G (Ω)
1	NC	NC	NC	NC
2	50K	49.9K	49.4K	49.9K
5	12.5K	12.4K	12.35K	12.4K
10	5.556K	5.62K	5489	5.49K
20	2.632K	2.61K	2600	2.61K
50	1.02K	1.02K	1008	1K
100	505.1	511	499	499
200	251.3	249	248	249
500	100.2	100	99	100
1000	50.5	49.9	49.5	49.9
2000	25.01	24.9	24.7	24.9
5000	10	10	9.88	9.76
10000	5.001	4.99	4.94	4.87

NC: No Connection

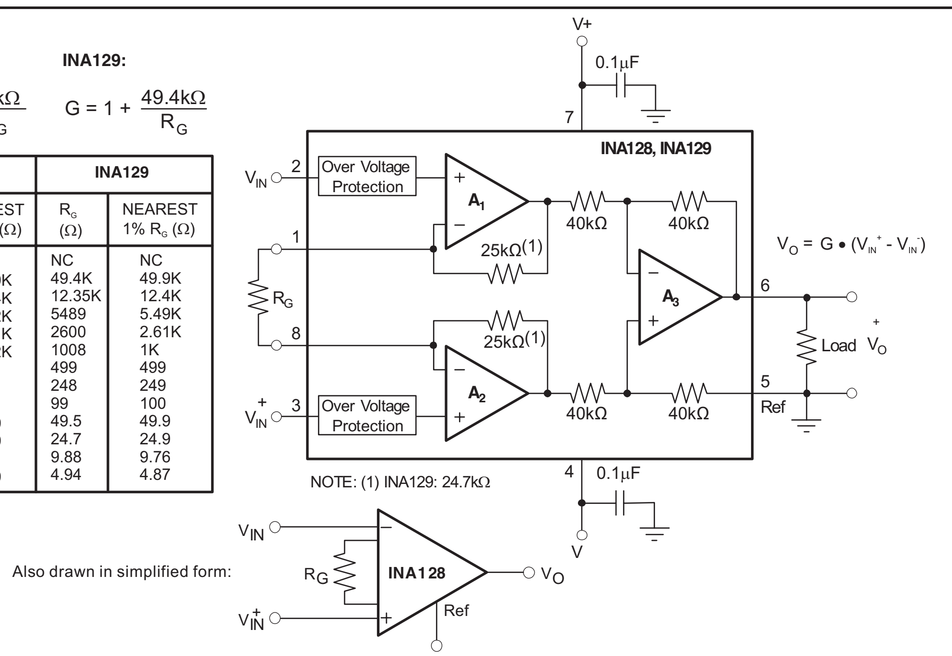


Figure 24. Basic Connections

Dynamic Performance

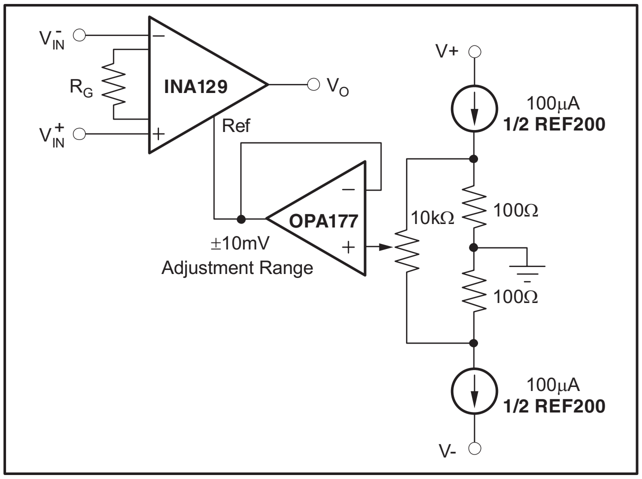
Figure 2 shows that, despite its low quiescent current, the INA128/INA129 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the input stage circuitry. Settling time also remains excellent at high gain.

Noise Performance

The INA128/INA129 provides very low noise in most applications. Low frequency noise is approximately 2 μVPP measured from 0.1 Hz to 10 Hz (G ≥ 100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

Offset Trimming

The INA128/INA129 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 25 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The operational amplifier buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.



(1) OPA177 and REF200 are not tested or characterized at 210°C.

Figure 25. Optional Trimming of Output Offset Voltage

Input Bias Current Return Path

The input impedance of the INA128/INA129 is extremely high (approximately 10^{10} Ω). However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±50 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 26 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range, and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 26). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

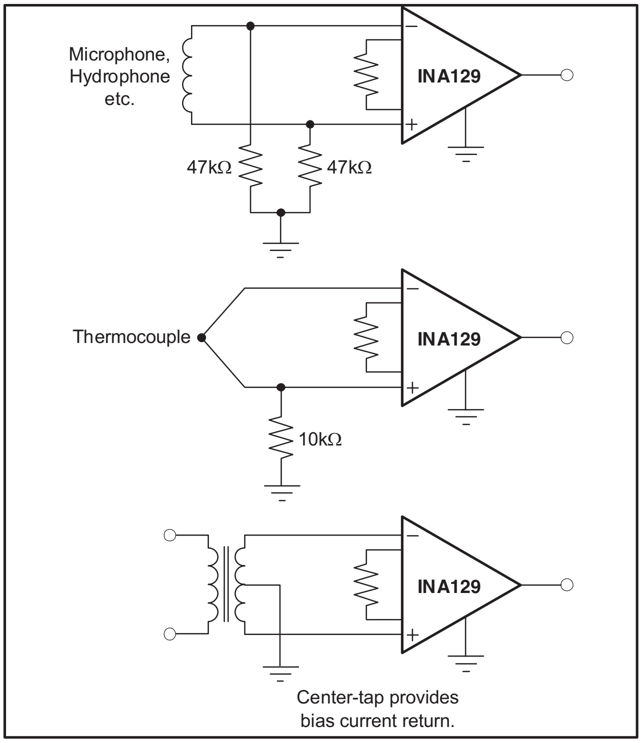


Figure 26. Providing an Input Common-Mode Current Path

Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA128/INA129 is from approximately 1.4 V below the positive supply voltage to 1.7 V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range will be limited by the output voltage swing of amplifiers A1 and A2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage (see Figure 6 and Figure 7).

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of A3 will be near 0 V even though both inputs are overloaded.

Low Voltage Operation

The INA128/INA129 can be operated on power supplies as low as ±2.25 V. Performance remains excellent with power supplies ranging from ±2.25 V to ±18 V. Most parameters vary only slightly throughout this supply voltage range.

Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Figure 6 and Figure 7 show the range of linear operation for ±15 V, ±5 V, and ±2.5 V supplies.

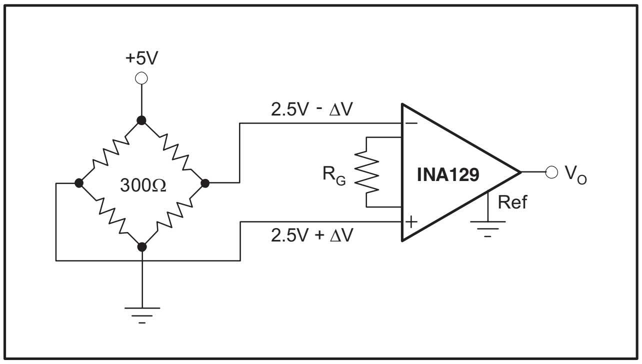
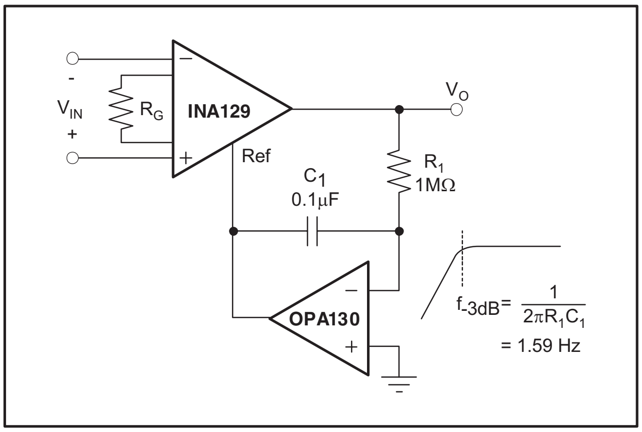
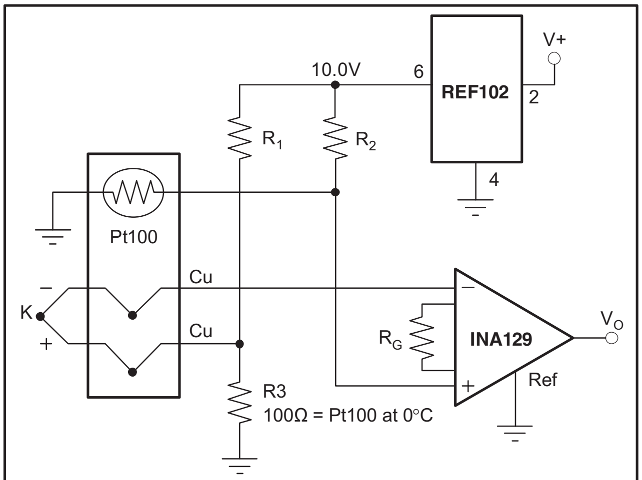


Figure 27. Bridge Amplifier



(1) OPA130 is not tested or characterized at 210°C.

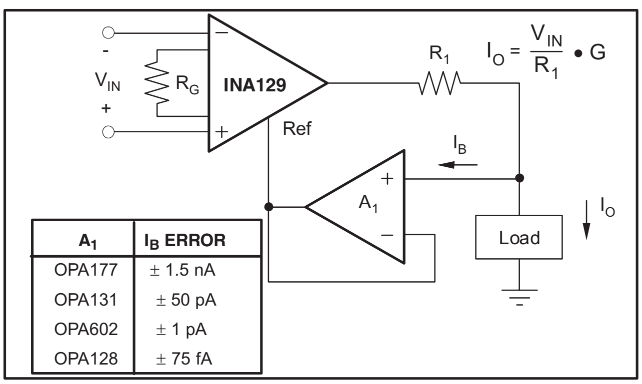
Figure 28. AC-Coupled Instrumentation Amplifier



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (μV/°C)	R_1, R_2
E	+Chromel -Constantan	58.5	66.5kΩ
J	+Iron -Constantan	50.2	76.8kΩ
K	+Chromel -Alumel	39.4	97.6kΩ
T	+Copper -Constantan	38	102kΩ

(1) REF102 is not tested or characterized at 210°C.

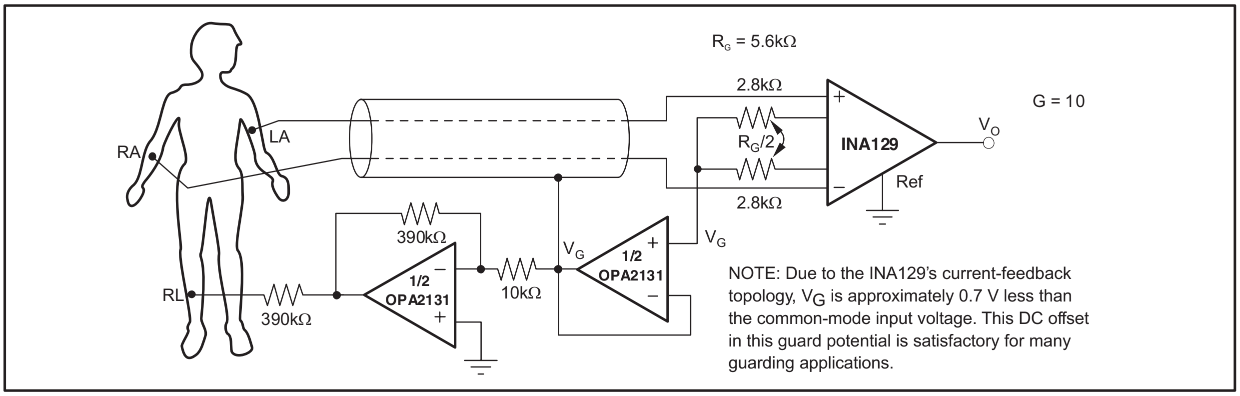
Figure 29. Thermocouple Amplifier With RTD Cold-Junction Compensation



A_1	I_B ERROR
OPA177	± 1.5 nA
OPA131	± 50 pA
OPA602	± 1 pA
OPA128	± 75 fA

(1) OPA177, OPA131, OPA602 and OPA128 are not tested or characterized at 210°C.

Figure 30. Differential Voltage to Current Converter



(1) OPA2131 is not tested or characterized at 210°C.

Figure 31. ECG Amplifier With Right-Leg Drive

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA128HD	ACTIVE	SOIC	D	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to +175	128HD	Samples
INA129SHKJ	ACTIVE	CFP	HKJ	8	1	TBD	Call TI	N / A for Pkg Type	-55 to 210	INA129S HKJ	Samples
INA129SHKQ	ACTIVE	CFP	HKQ	8	1	TBD	AU	N / A for Pkg Type	-55 to 210	INA129S HKQ	Samples
INA129SJD	ACTIVE	CDIP SB	JDJ	8	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 210	INA129SJD	Samples
INA129SKGD1	ACTIVE	XCEPT	KGD	0	180	TBD	Call TI	N / A for Pkg Type	-55 to 210		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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OTHER QUALIFIED VERSIONS OF INA128-HT, INA129-HT :

- Catalog: INA128, INA129

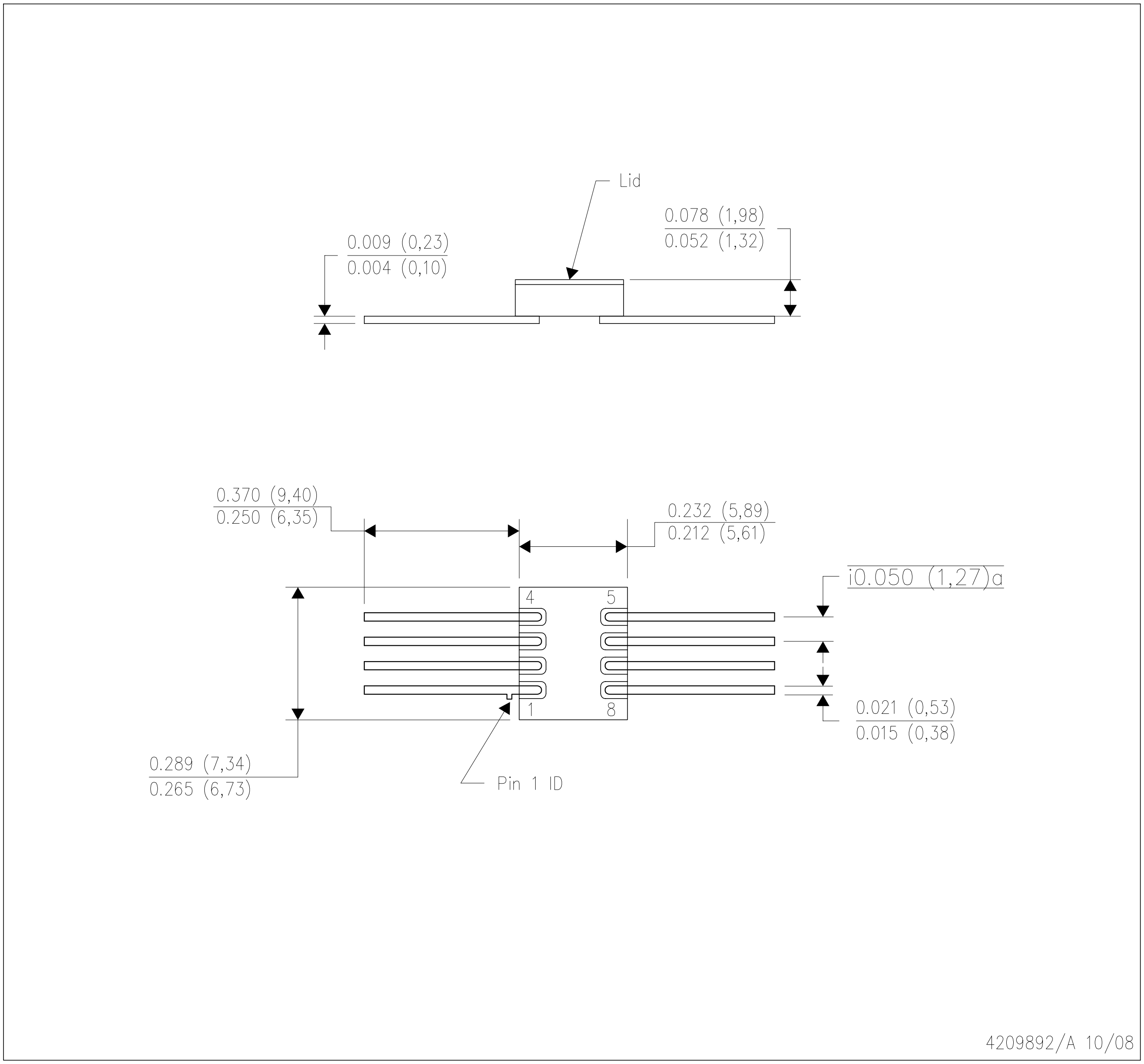
- Enhanced Product: INA129-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

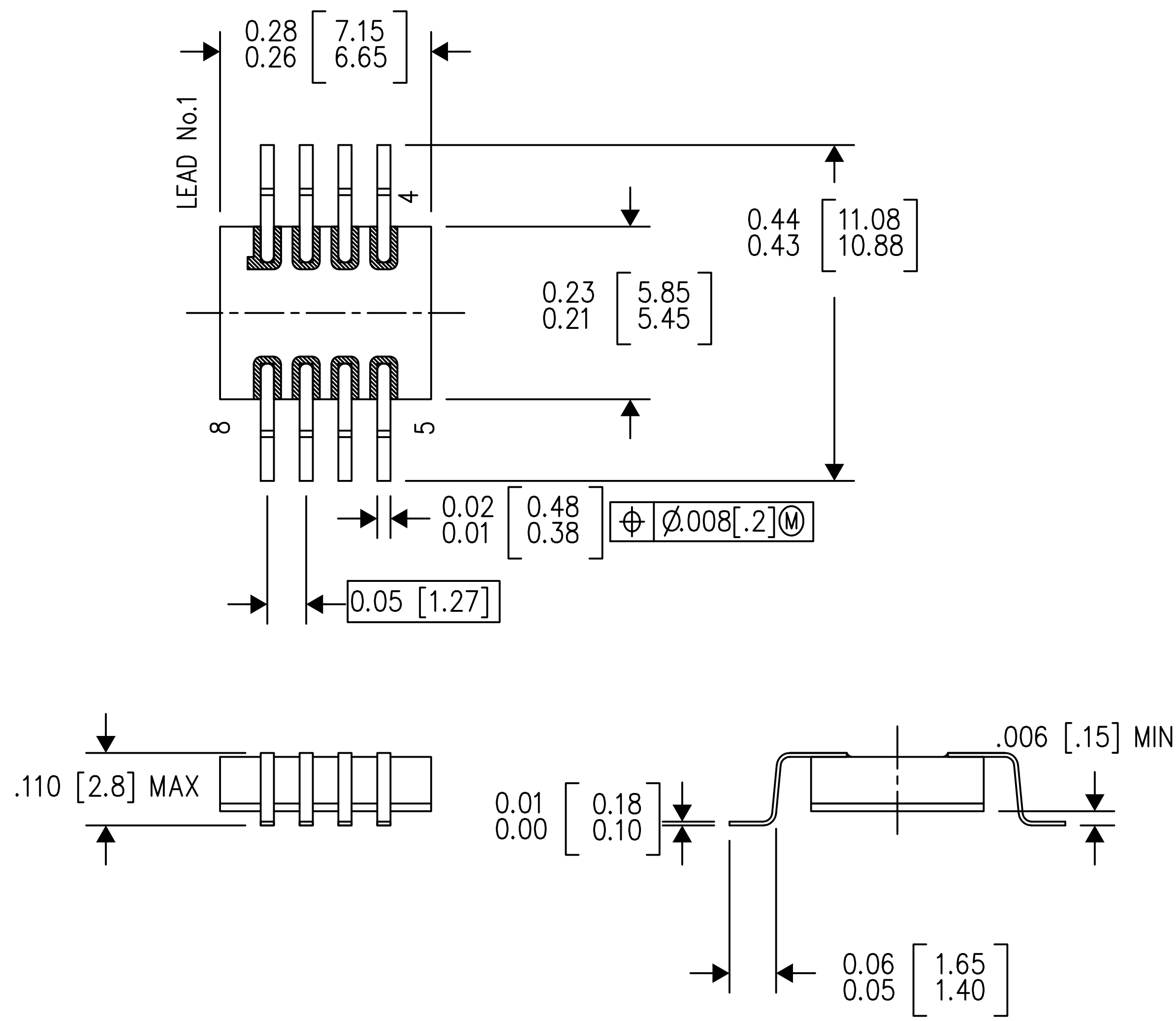
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

HKJ (R–CDFP–F8) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

HKQ (R–CDFP–G8) CERAMIC GULL WING



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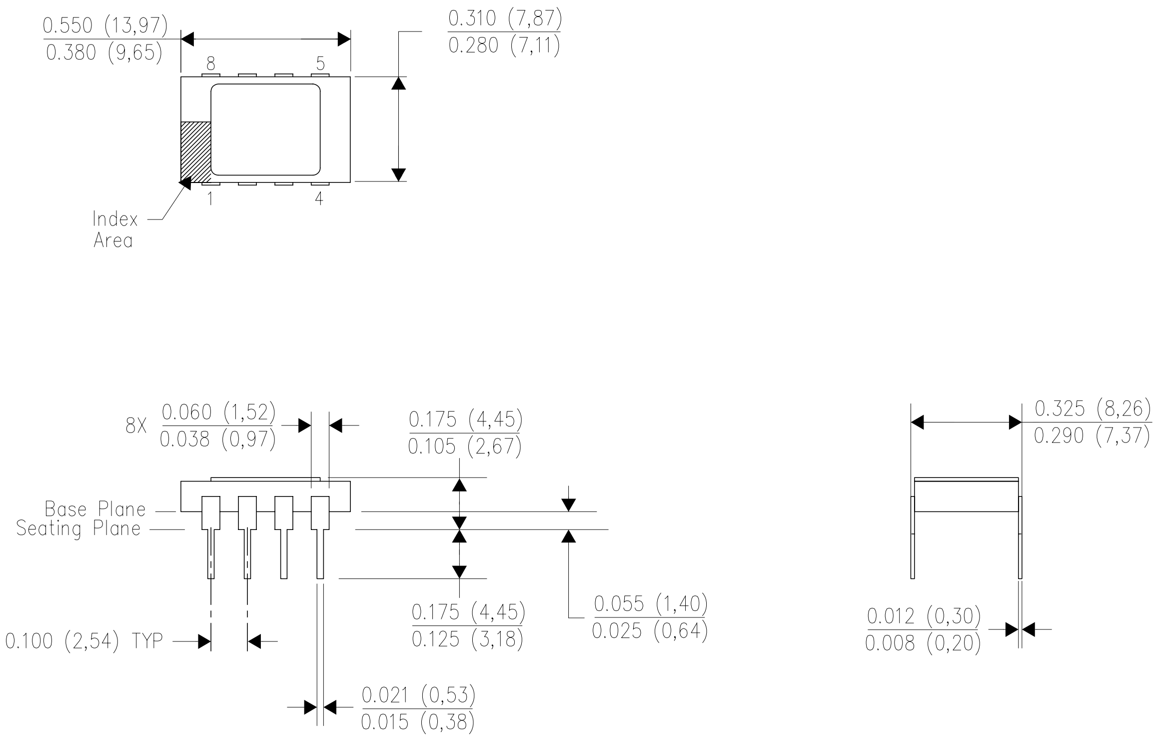
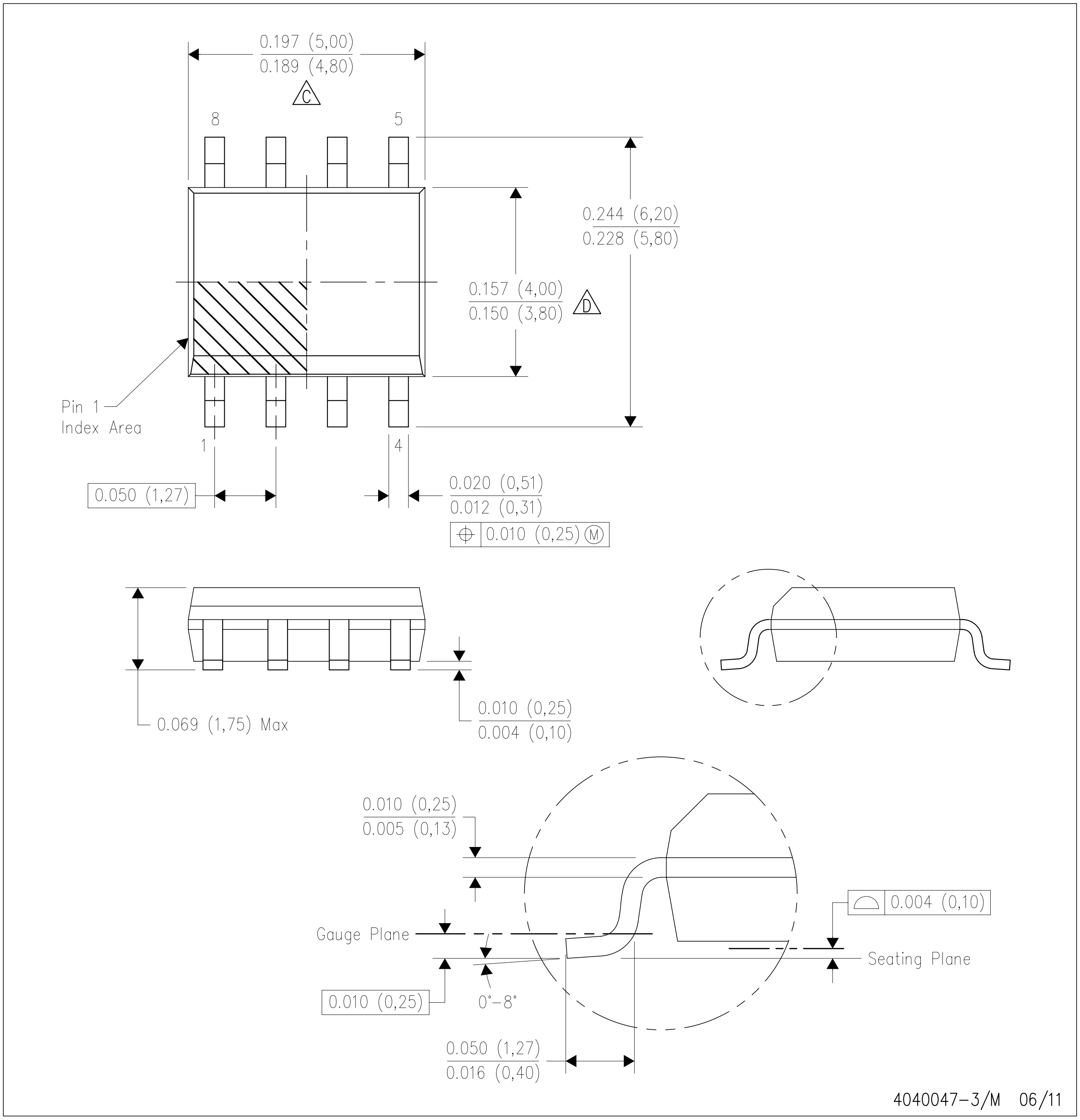
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals will be gold plated.
- E. Lid is not connected to any lead.

JDJ (R–CDIP–T8) CERAMIC DUAL IN–LINE PACKAGE



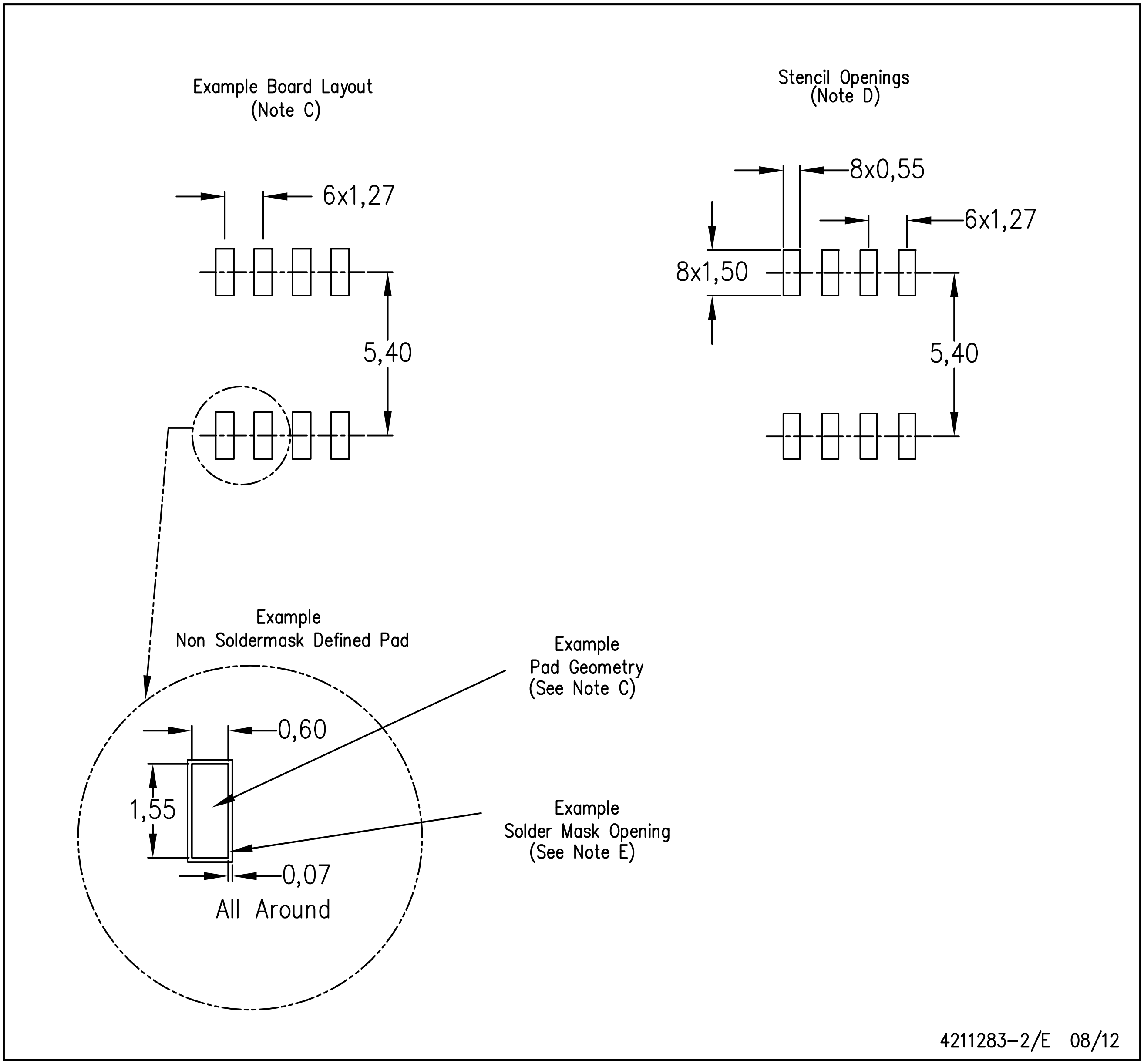
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.
G. Lid and heat sink are connected to GND leads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.