DUAL, ISOLATED, BIDIRECTIONAL DIGITAL COUPLER

FEATURES

- **Replaces High-Performance Optocouplers**
- **Data Rate: 80 M Baud, Typ**
- **Low Power Consumption: 25 mW Per Channel, Max**
- **Two Channels, Each Bidirectional, Programmable by User**
- **Partial Discharge Tested: 2400 Vrms**
- **Creepage Distance of 7,2 mm**
- **Low Cost Per Channel**
- **Available in SO Package**

APPLICATIONS

- **Digital Isolation for A/D, D/A Conversion**
- **Isolated RS-485 Interface**
- **Multiplexed Data Transmission**
- **Isolated Parallel to Serial Interface**
- **Test Equipment**
- **Microprocessor System Interface**
- **Isolated Line Receiver**
- **Ground Loop Elimination**

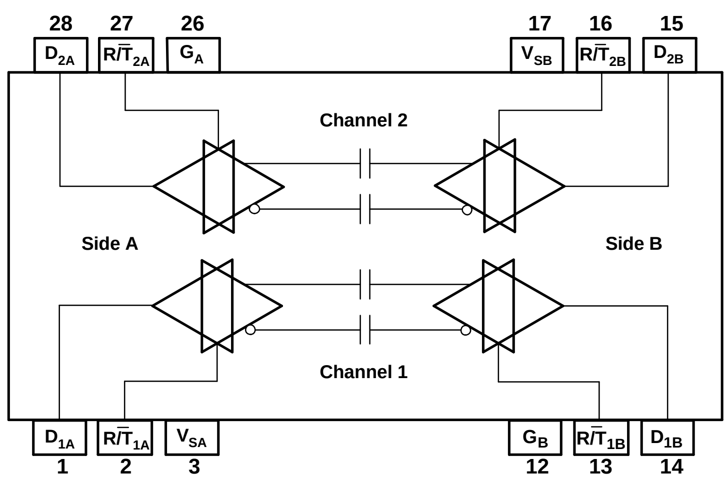
DESCRIPTION

The ISO150 is a 2-channel, galvanically-isolated data coupler capable of data rates of 80M Baud, typical. Each channel can be individually programmed to transmit data in either direction.

Data is transmitted across the isolation barrier by coupling complementary pulses through high voltage 0.4 pF capacitors. Receiver circuitry restores the pulses to standard logic levels. Differential signal transmission rejects isolation-mode voltage transients up to 1.6 kV/µs

The ISO150 avoids problems commonly associated with optocouplers. Optically isolated couplers require high current pulses and allowance must be made for LED aging. The ISO150's Bi-CMOS circuitry operates at 25 mW per channel.

The ISO150 is available in an SO-28 and is specified for operation from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ISO150AU	SO-28	DVB	–40°C to 85°C	ISO150AU	ISO150AU	Rails, 28
					ISO150AU/1K	Tape and Reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		UNIT
	Storage temperature	–40°C to 125°C
V_S	Supply voltage	–0.5 V to 6 V
V_I	Transmitter input voltage	–0.5 V to V_S + 0.5 V
V_O	Receiver output voltage	–0.5 V to V_S + 0.5 V
	$R/\overline{T}_x$ inputs	–0.5 V to V_S + 0.5 V
V_{ISO}	Isolation voltage dV/dt	500 kV/µs
D_x	Short to ground	Continuous
T_J	Junction temperature	175°C
	Lead temperature (soldering, 10s)	260°C

ELECTRICAL CHARACTERISTICS

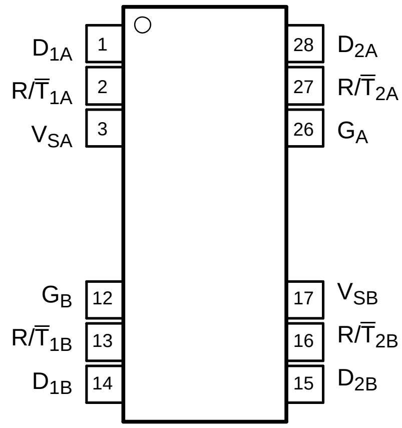
At T_A = 25°C and V_S = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ISO150AU MIN	ISO150AU TYP	ISO150AU MAX	UNIT
ISOLATION PARAMETERS						
Rated Voltage, Continuous		60 Hz	1500			Vrms
Partial Discharge, 100% Test(1)		1s, 5pC	2400			Vrms
Creepage distance (external)	SO-U Package			7.2		mm
Internal isolation distance				0.10		mm
Isolation voltage transient immunity(2)				1.6		kV/µs
Barrier impedance				$>10^{14}$ || 7		Ω || pF
Leakage current		240 Vrms, 50 Hz		0.6		µArms
DC PARAMETERS						
Logic output voltage	HIGH, V_{OH}	I_{OH} = 6 mA	V_S – 1		V_S	V
	LOW, V_{OL}	I_{OL} = 6 mA	0		0.4	V
Logic output short-circuit current		Source or sink		30		mA
Logic input voltage	HIGH(3)		2		V_S	V
	LOW(3)		0		0.8	V
Logic input capacitance				5		pF
Logic input current				<1		nA
Power-supply voltage range(3)			3	5	5.5	V
Power-supply current(4)	Transmit mode	DC		0.001	100	µA
	Transmit mode	50M Baud		14		mA
	Receive mode	DC		7.2	10	mA
	Receive mode	50M Baud		16		mA
AC PARAMETERS						
Data rate	Maximum(5)	C_L = 50 pF	50	80		M Baud
	Minimum		DC			M Baud
Propagation time(6)		C_L = 50 pF		27	40	ns
Propagation delay skew(7)		C_L = 50 pF		0.5	2	ns
Pulse width distortion(8)		C_L = 50 pF		1.5	6	ns
Output rise-and-fall time, 10% to 90%		C_L = 50 pF		9	14	ns
Mode switch time	Receive to Transmit			13		ns
	Transmit to receive(9)			75		ns
TEMPERATURE RANGE						
Operating range			–40		85	°C
Storage			–40		125	°C
Thermal resistance, θ_{JA}				75		°C/W

(1) All devices receive a 1s test. Failure criterion is ≥ 5 PULSES OF ≥5 Pc.
(2) The voltage rate-of-change across the isolation barrier that can be sustained without data errors.
(3) Logic inputs are HCT-type and thresholds are a function of power-supply voltage with approximately 0.4 V hysteresis – see text.
(4) Supply current measured with both transceivers set for the indicated mode. Supply current varies with data rate – see typical characteristics.
(5) Calculated from the maximum pulse width distortion (PWD), where Data Rate = 0.3/PWD.
(6) Propagation time measured from V_{IN} = 1.5 V to V_O = 2.5 V.
(7) The difference in propagation time of channel A and channel B in any combination of transmission directions.
(8) The difference between propagation time of a rising edge and a falling edge.
(9) When the device is powered up or direction is changed, the transceiver output is indeterminate (either high or low) and cannot be known until an input signal is applied. The output begins to track the input as soon as the input receives a change in logic state, either low to high or high to low.

PIN CONFIGURATION

Top View **SO**



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
D_{1A}	1	Data in or data out for transceiver 1A, $R/\overline{T}_{1A}$ held low makes D_{1A} and input pin.
$R/\overline{T}_{1A}$	2	Receive/transmit switch controlling transceiver 1A.
V_{SA}	3	+5V supply pin for side A, which powers transceivers 1A and 2A.
G_B	12	Ground pin for transceivers 1B and 2B.
$R/\overline{T}_{1B}$	13	Receive/transmit switch controlling transceiver 1B.
D_{1B}	14	Data in or data out for transceiver 1B. $R/\overline{T}_{1B}$ held LOW makes D_{1B} an input pin.
D_{2B}	15	Data in or data out for transceiver 2B. $R/\overline{T}_{2B}$ held LOW makes D_{2B} an input pin.
$R/\overline{T}_{2B}$	16	Receive/transmit switch controlling D_{2B}.
V_{SB}	17	+5V supply pin for side B, which powers transceivers 1B and 2B.
G_A	26	Ground pin for transceivers 1A and 2A.
$R/\overline{T}_{2A}$	27	Receive/transmit switch controlling transceiver 2A.
D_{2A}	28	Data in or data out for transceiver 2A, $R/\overline{T}_{21A}$ held low makes D_{2A} and input pin.

TYPICAL CHARACTERISTICS

At T_A = 25°C and V_S = 5 V, unless otherwise noted.

SUPPLY CURRENT PER CHANNEL vs SUPPLY VOLTAGE

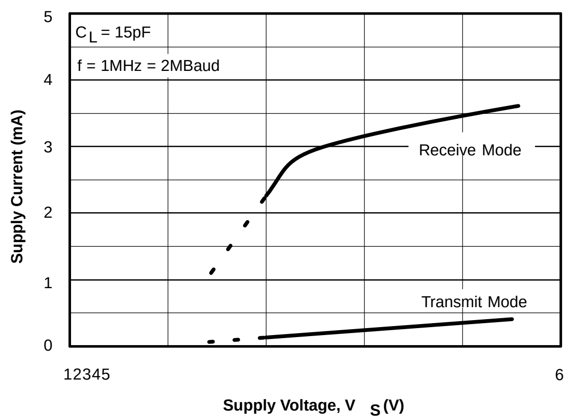


Figure 1.

POWER CONSUMPTION PER CHANNEL vs FREQUENCY

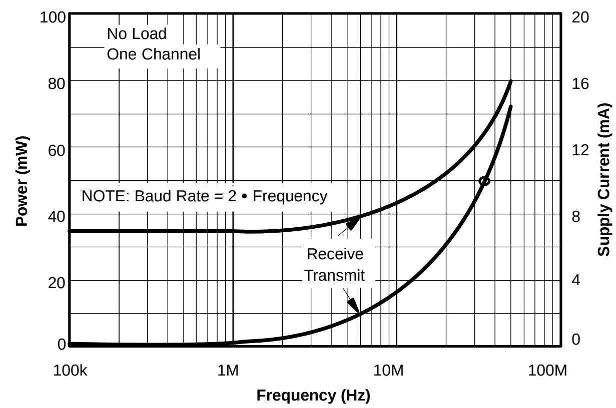


Figure 2.

SUPPLY CURRENT PER CHANNEL vs TEMPERATURE

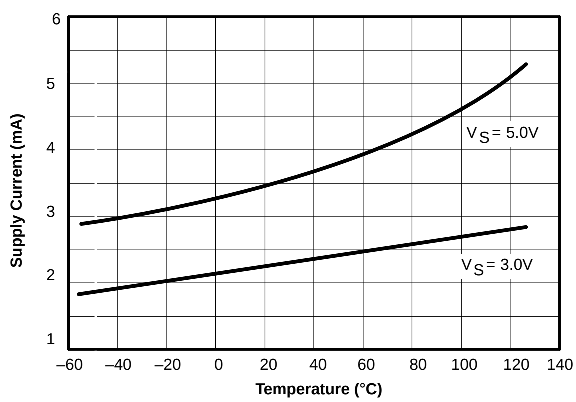


Figure 3.

TYPICAL RISE AND FALL TIMES vs CAPACITIVE LOAD vs SUPPLY VOLTAGE

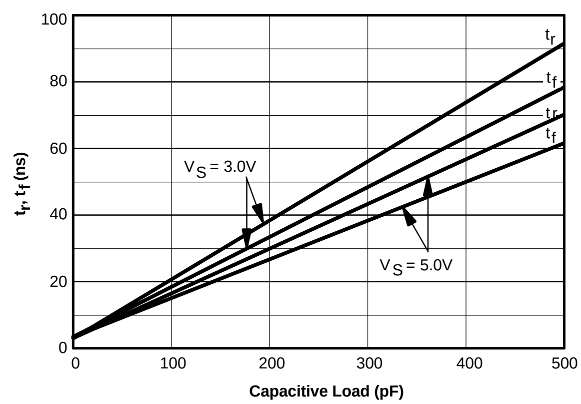


Figure 4.

NORMALIZED RISE-AND-FALL TIME vs TEMPERATURE

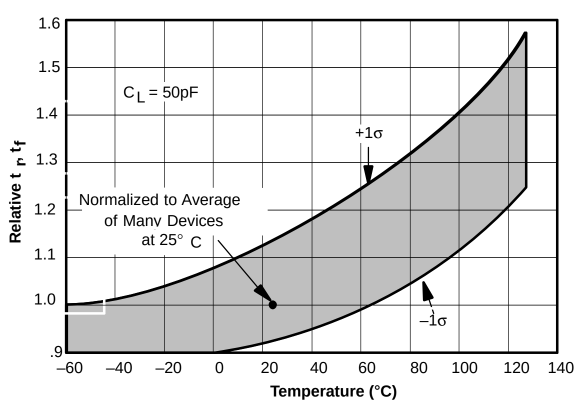


Figure 5.

PROPAGATION DELAY vs SUPPLY VOLTAGE

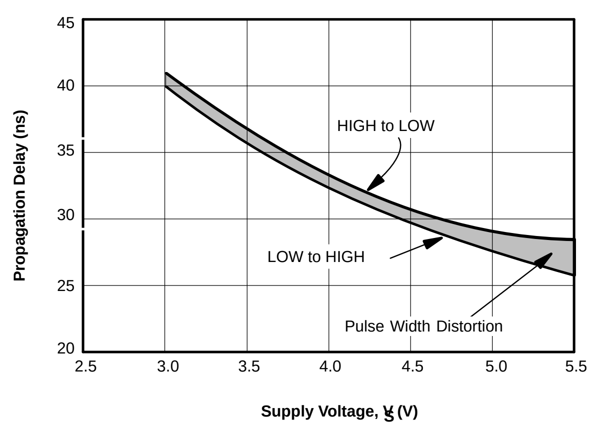


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C and V_S = 5 V, unless otherwise noted.

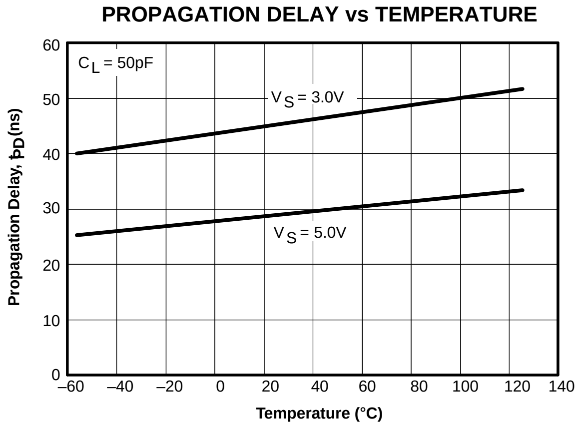


Figure 7.

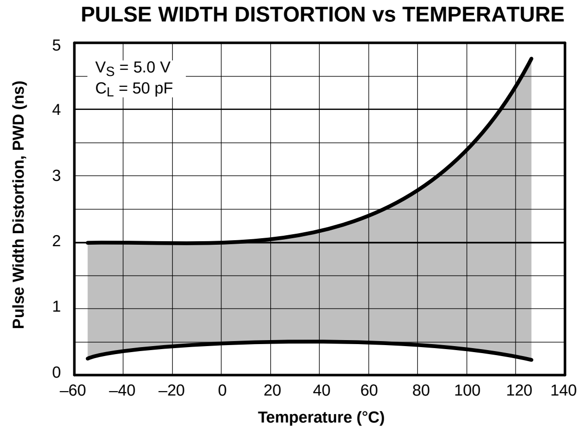


Figure 8.

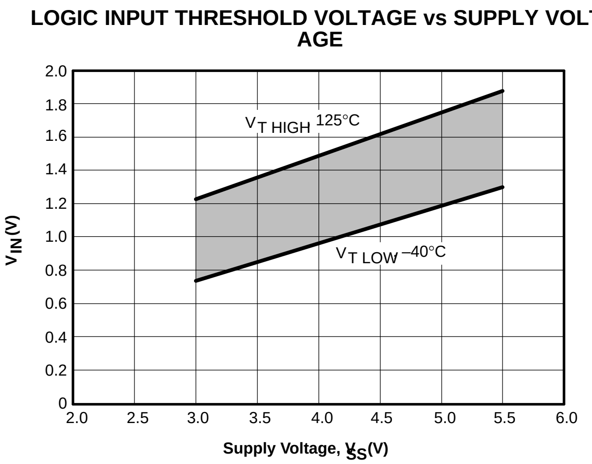


Figure 9.

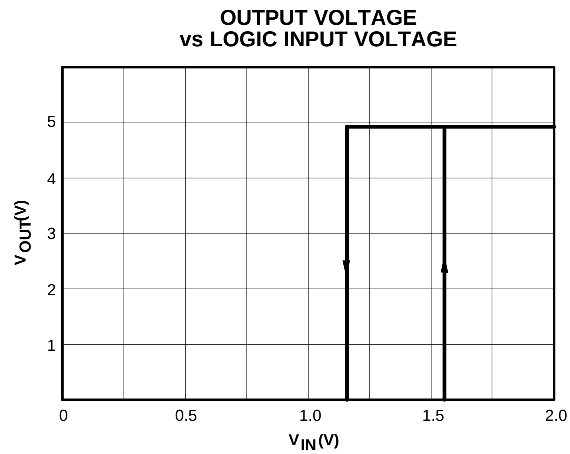


Figure 10.

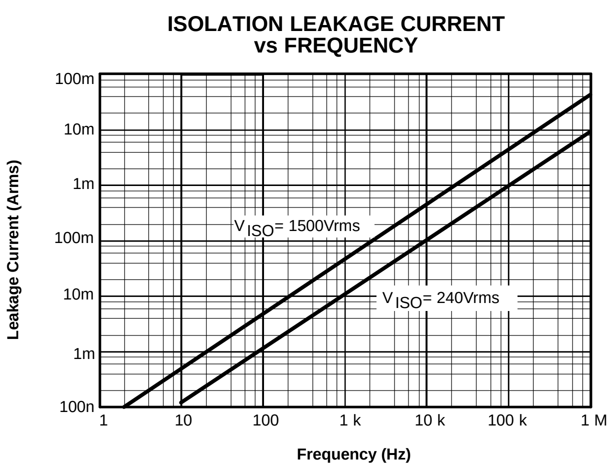


Figure 11.

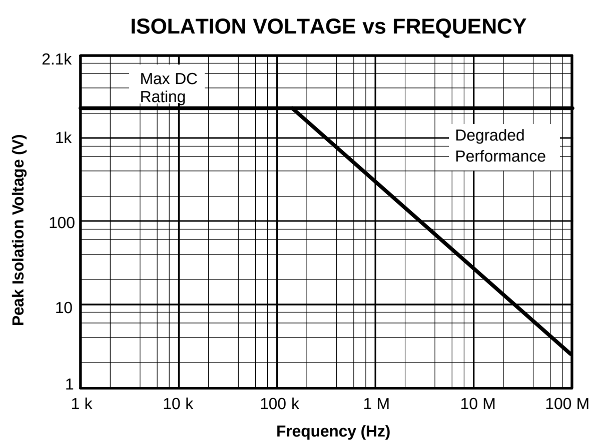


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C and V_S = 5 V, unless otherwise noted.

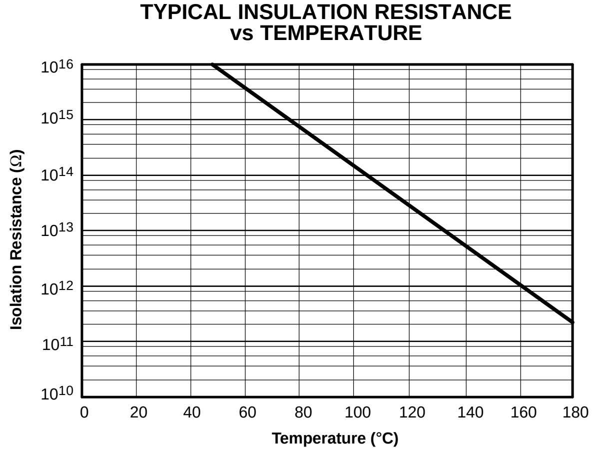


Figure 13.

ISOLATION BARRIER

Data is transmitted by coupling complementary logic pulses to the receiver through two 0.4 pF capacitors. These capacitors are built into the ISO150 package with Faraday shielding to guard against false triggering by external electrostatic fields.

The integrity of the isolation barrier of the ISO150 is verified by partial discharge testing: 2400 Vrms, 60 Hz, is applied across the barrier for one second while measuring any tiny discharge currents that might flow through the barrier. These current pulses are produced by localized ionization within the barrier; this is the most sensitive and reliable indicator of barrier integrity and longevity, and does not damage the barrier. A device fails the test if five or more current pulses of 5pC or greater are detected.

Conventional isolation barrier testing applies test voltage far in excess of the rated voltage to catastrophically break down a marginal device. A device that passes the test may be weakened, and lead to premature failure.

APPLICATION INFORMATION

Figure 14 shows the ISO150 connected for basic operation; Channel 1 is configured to transmit data from side B to A, whereas Channel 2 is set for transmission from side A to B. The R/T̄ pins for each of the four transceivers are shown connected to the required logic level for the transmission direction shown. The transmission direction can be controlled by logic signals applied to the R/T̄ pins. Channel 1 and 2 can be independently controlled for the desired transmission direction. See Figure 15 and Figure 16 for application examples using the ISO150.

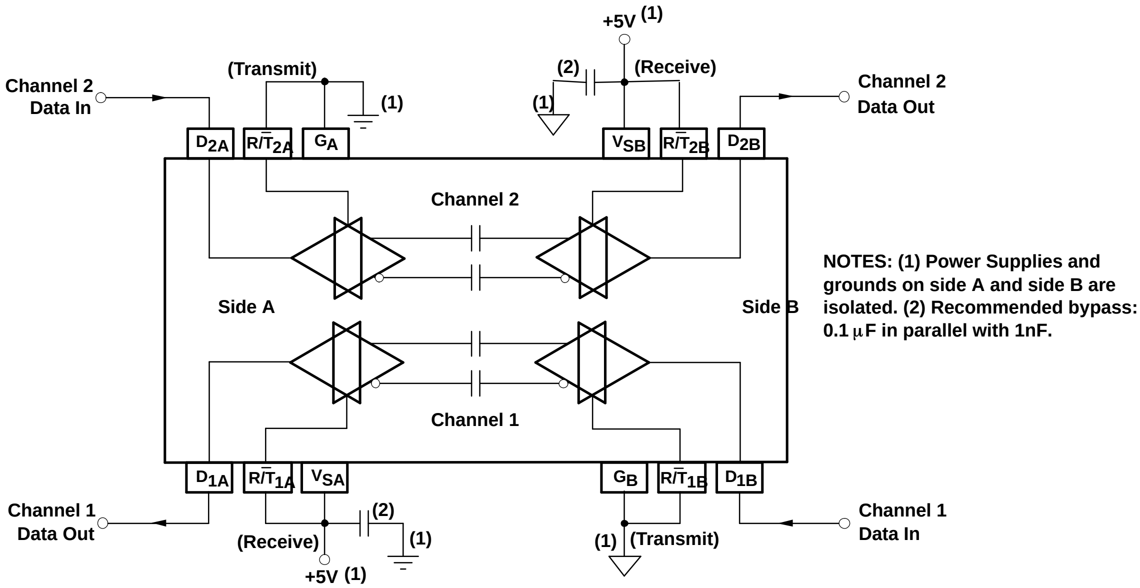


Figure 14. Basic Operation Diagram

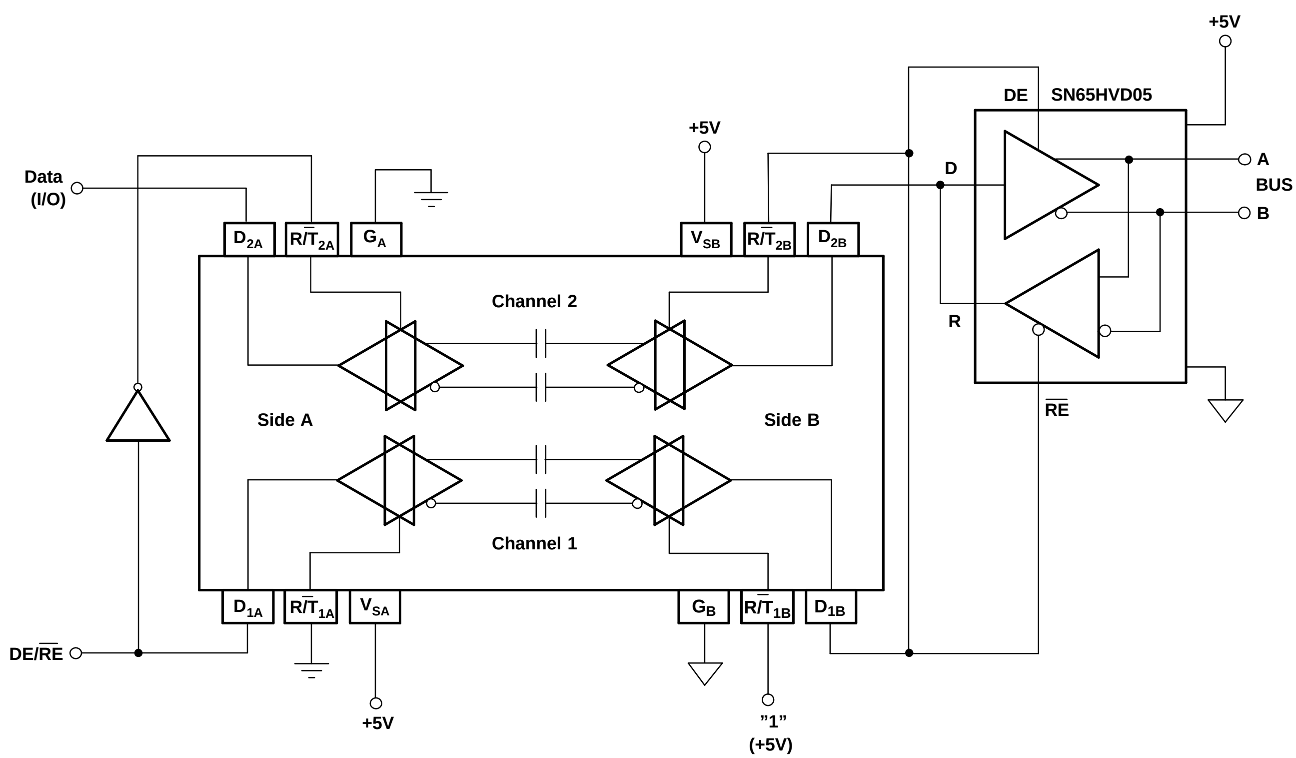


Figure 15. Isolated RS-485 Interface

LOGIC LEVELS

A single pin serves as a data input or output, depending on the mode selected. Logic inputs are CMOS with thresholds set for TTL compatibility. The logic threshold is approximately 1.3 V with 5 V supplies with approximately 400 mV of hysteresis. Input logic thresholds vary with the power-supply voltage. Drive the logic inputs with signals that swing the full logic voltage swing, note that the ISO150 will use somewhat greater quiescent current if logic inputs do not swing within 0.5 V of the power-supply rails.

In receive mode, the data output can drive 15 standard LS-TTL loads. It will also drive CMOS loads. The output drive circuits are CMOS.

POWER SUPPLY

Separate, isolated power supplies must be connected to side A and side B to provide galvanic isolation. Nominal rated supply voltage is 5 V. Operation extends from 3 V to 5.5 V. Power supplies should be bypassed close to the device pins on both sides of the isolation barrier.

The V_S pin for each side powers the transceivers for both channel 1 and 2. The specified supply current is the total of both transceivers on one side, both operating in the indicated mode. Supply current for one transceiver in transmit mode and one in receive mode can be estimated by averaging the specifications for transmit and receive operation. Supply current varies with the data transmission rate — see the typical characteristics.

POWER-UP STATE

When the device is powered up or direction is changed, the transceiver output is indeterminate (either high or low) and cannot be known until an input signal is applied. The output begins to track the input as soon as the input receives a change in logic state, either low to high or high to low.

SIGNAL LOSS

The ISO150's differential-mode signal transmission and careful receiver design make it highly immune to voltage across the isolation barrier (isolation-mode voltage). Rapidly changing isolation-mode voltage can cause data errors. As the rate of change of isolation voltage is increased, there is a very sudden increase in data errors. Approximately 50% of all ISO150s will begin to produce data errors with isolation-mode transients of 1.6kV/µs. This may occur as low as 500 V/µs in some devices. In comparison, a 1000 Vrms, 60 Hz isolation-mode voltage has a rate of change of approximately 0.5V/µs.

Still, some applications with large, noisy isolation-mode voltage can produce data errors by causing the receiver output to change states. After a data error, subsequent changes in input data will produce correct output data.

PROPAGATION DELAY AND SKEW

Logic transitions are delayed approximately 27ns through the ISO150. Some applications are sensitive to data skew—the difference in propagation delay between channel 1 and channel 2. Skew is less than 2ns between channel 1 and channel 2. Applications using more than one ISO150 must allow for somewhat greater skew from device to device. As all devices are tested for delay times of 20ns min to 40ns max, 20ns is the largest device-to-device data skew.

MODE CHANGES

The transmission direction of a channel can be changed *on the fly* by reversing the logic levels at the channel's R/$\overline{T}$ pin. Note that when channel direction is changed, the output state of the channel is indeterminate (either high or low) and cannot be known until an input signal is applied. The output begins to track the input as soon as the input receives a change in logic state, either low to high or high to low.

STANDBY MODE

Quiescent current of each transceiver circuit is very low in transmit mode when input data is not changing (1nA typical). To conserve power when data transmission is not required, program both side A and B transceivers for transmit mode. Input data applied to either transceiver is ignored by the other side. High-speed data applied to either transceiver will increase quiescent current.

CIRCUIT LAYOUT

The high speed of the ISO150 and its isolation barrier require careful circuit layout. Use good high speed logic layout techniques for the input and output data lines. Power supplies should be bypassed close to the device pins on both sides of the isolation barrier. Use low inductance connections. Ground planes are recommended.

Maintain spacing between side 1 and side 2 circuitry equal or greater than the spacing between the missing pins of the ISO150 (approximately 7mm).

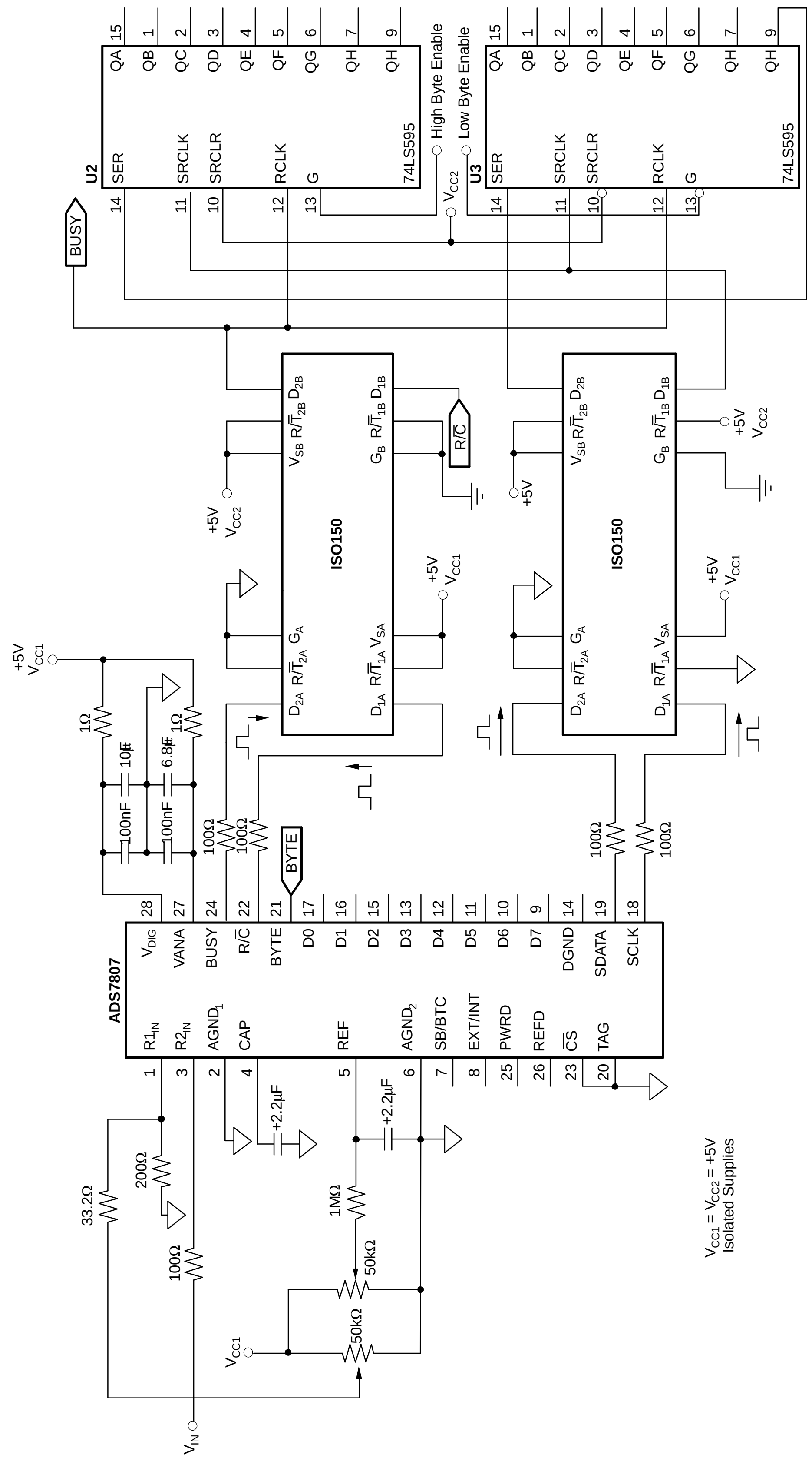


Figure 16. The ISO150 and the ADS7807 are Used to Reduce Circuit Noise in a Mixed-Signal Application

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
ISO150AP	OBSOLETE	PDIP	NVG	12		None	Call TI	Call TI
ISO150AU	ACTIVE	SOP	DVB	12	28	None	CU SNPB	Level-3-240C-168 HR
ISO150AU/1K	ACTIVE	SOP	DVB	12	1000	None	CU SNPB	Level-3-240C-168 HR
ISO150AUG4	PREVIEW	SOP	DVB	12	28	None	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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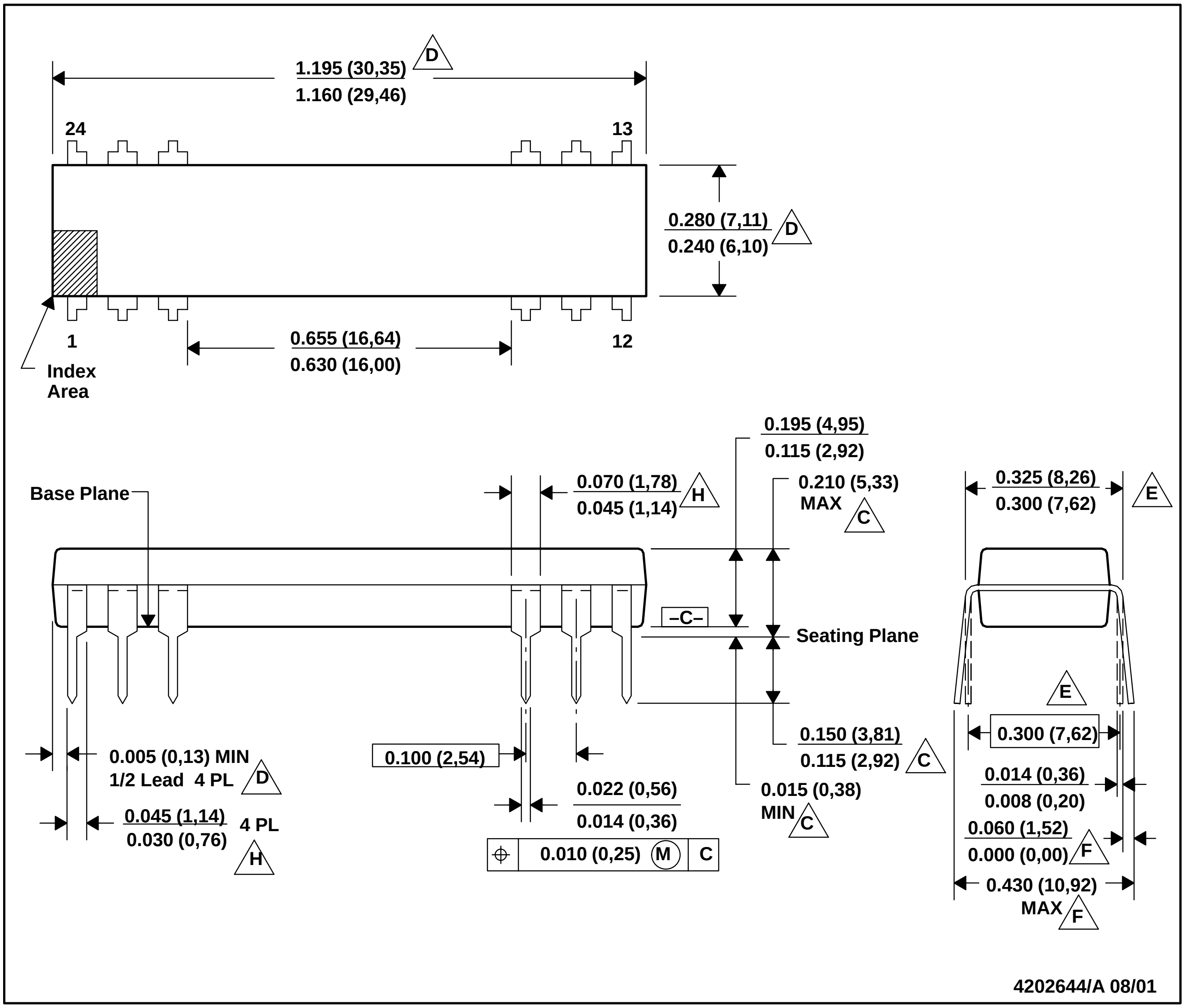
NVG (R-PDIP-T12/24) **PLASTIC DUAL-IN-LINE**



NOTES:

A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Dimensions are measured with the package seated in JEDEC seating plane gauge GS-3.

D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).

E. Dimensions measured with the leads constrained to be perpendicular to Datum C.

F. Dimensions are measured at the lead tips with the leads unconstrained.

G. Pointed or rounded lead tips are preferred to ease insertion.

H. Maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).

I. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.

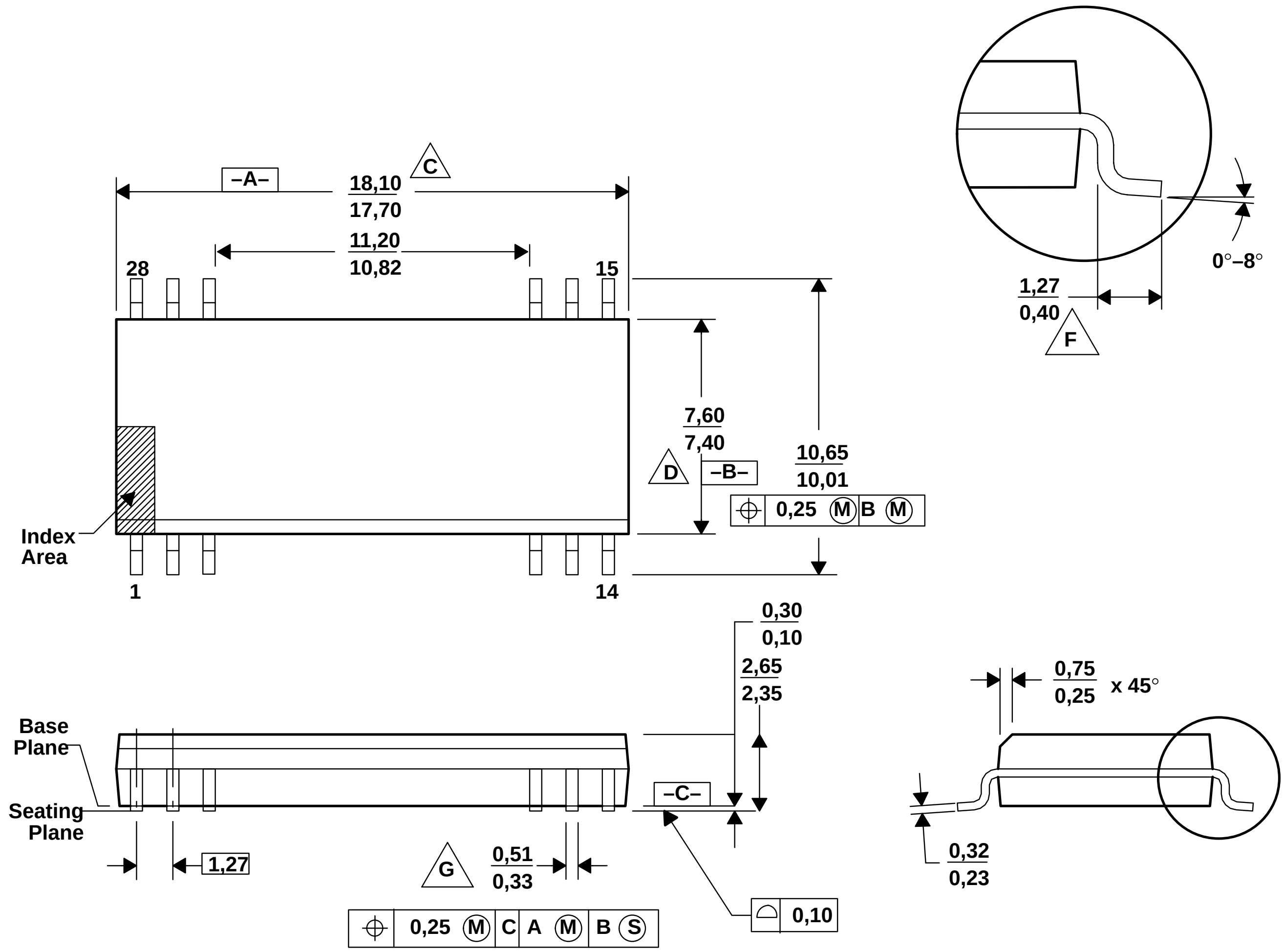
J. A visual index feature must be located within the cross–hatched area.

K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

L. Controlling dimension in inches.

M. Falls within JEDEC-MS-001-BE with exception of lead count.

DVB(R-PDSO-G12/28) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0,15 mm per side.
D. Body width dimension does not include inter-lead flash or portrusions. Inter-lead flash and protrusions shall not exceed 0,25 mm per side.
E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
F. Lead dimension is the length of terminal for soldering to a substrate.
G. Lead width, as measured 0,36 mm or greater above the seating plane, shall not exceed a maximum value of 0,61 mm.
H. Lead-to-lead coplanarity shall be less than 0,10 mm from seating plane.
I. Falls within JEDEC MS-013-AE with the exception of the number of leads.

IMPORTANT NOTICE

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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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