LM3686 Step-Down DC-DC Converter with Integrated Post Linear Regulators System and Low-Noise Linear Regulator

Check for Samples: LM3686

FEATURES

DC-DC REGULATOR

- **V_{OUT_DCDC} = 1.2V to 2.5V (in 100 mV Steps - Factory Programmed)**
- **600 mA Maximum Load Capability (LILO = OFF)**
- **3 MHz PWM Fixed Switching Frequency (Typ.)**
- **Automatic PFM/PWM Mode Switching**
- **Internal Synchronous Rectification for High Efficiency**
- **Internal Soft Start**

DUAL RAIL LINEAR REGULATOR: LILO

- **Load Transients < 50 mV Peak Typ.**
- **Line Transients < 1 mV Peak Typ.**
- **V_{OUT_LILO} = 0.7V to 2.0V (in 50 mV Steps - Factory Programmed)**
- **70 µA Typical I_Q From V_{IN_LILO}**
- **350 mA Maximum Load Capability (Large FET)**

LINEAR REGULATOR: LDO

- **Load Transients < 80 mV Peak Typ.**
- **Line Transients < 1 mV Peak Typ.**
- **V_{OUT_LDO} = 1.5V to 3.3V (in 100 mV Steps - Factory Programmed)**
- **50 µA Typical I_Q**
- **300 mA Maximum Load Capability**

COMBINED GLOBAL FEATURES

- **$V_{BATT} \geq V_{OUT\_LILO}$ + 1.5V or 2.7V, Whichever is Higher**
- **900 mA Maximum Combined Load Capability**
- **Operates From a Single Li-Ion Cell or 3 Cell NiMH/NiCd Batteries**
- **Only Six Tiny Surface-mount External Components Required (One Inductor, Five Ceramic Capacitors)**
- **12–bump DSBGA**
- **100 µA Iq From V_{BATT}**
- **15.66 mm^2 Total Solution Size**

APPLICATIONS

- **Moblie TV**
- **Hand-Held Radios**
- **Personal Digital Assistants**
- **Palm-top PCs**
- **Portable Instruments**
- **Battery-Powered Devices**
- **Portable Personal Clients**

DESCRIPTION

The LM3686 is a step-down DC-DC converter with one integrated very low dropout linear regulator and a low noise linear regulator optimized for powering ultra-low voltage circuits from a single Li-Ion cell or 3 cell NiMH/NiCd batteries. It provides three outputs with combined load current up to 900 mA over an input voltage range from 2.7V to 5.5V.

The device offers superior features and performance for many applications. Automatic intelligent switching between PWM low-noise and PFM low-current mode offers improved system control. During full-power operation, a fixed-frequency 3 MHz (typ.), PWM mode drives loads from ~70 mA to 600 mA max. Hysteretic PFM mode extends the battery life through reduction of the quiescent current to 28 µA (typ.) at light load and system standby. Internal synchronous rectification provides high efficiency.

Three enable pins allow the separate operation of either the DC-DC, post-regulation linear regulator or the linear regulator alone. If the DC-DC is not enabled during startup of the post-regulation linear regulator, a parallel small pass transistor supplies the linear regulator from V_{BATT} with maximal 50 mA. In the combined operation where both enables are raised together, the small pass transistor is deactivated and the big pass transistor provides 350 mA output current. In shutdown mode (Enable pins pulled low), the device turns off and reduces battery consumption to 2.5 µA (typ.).

DESCRIPTION (CONTINUED)

The LM3686 is available in a 12-bump DSBGA package. A high-switching frequency of 3 MHz (typ.) allows the use of a few tiny surface-mount components. Only six external surface-mount components, an inductor and five ceramic capacitors, are required to establish a 15.66 mm^2 total solution size.

Typical Application Circuit

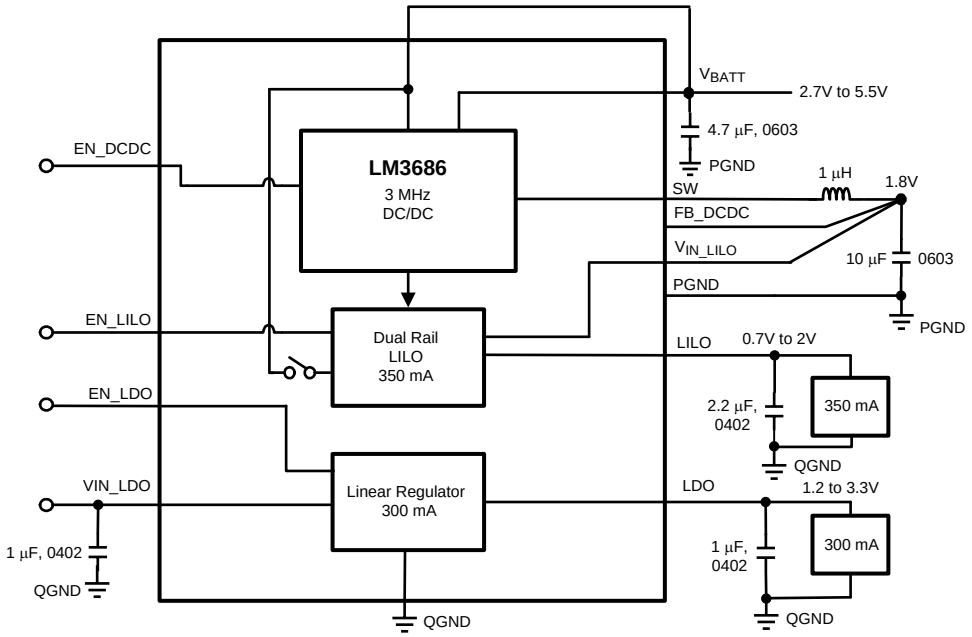


Figure 1. Typical Application

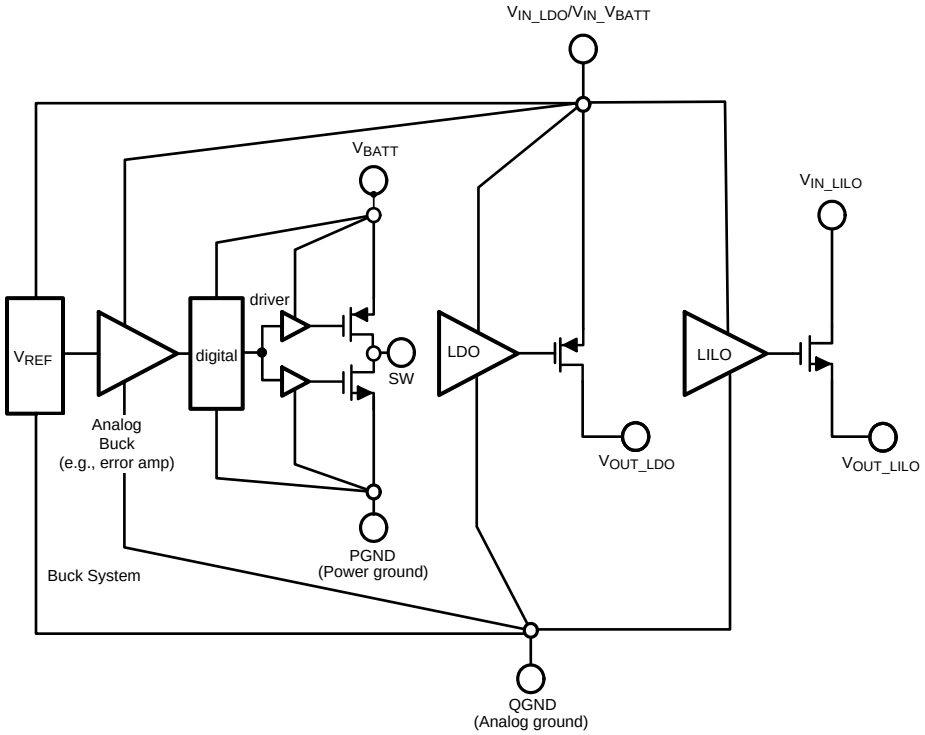


Figure 2. Functional Diagram (Always Connenct VIN_LDO to VBATT)

Connection Diagram

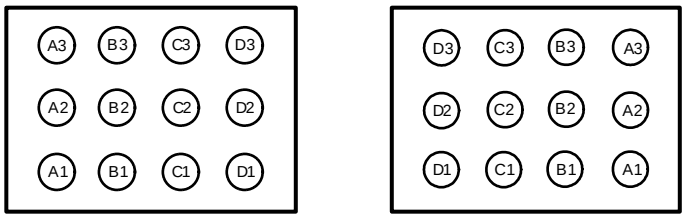


Figure 3. 12-pin DSBGA Package
See Package Number YZR0012

ORDERING INFORMATION

PART NUMBER	VOLTAGE OPTIONS
LM3686TL/TLX-AADW	1.8V_Bk
	1.2V_LILO
	2.8V_LDO
LM3686TLE/TLX-AAED	1.2V_Bk
	1.8V_LILO
	2.8V_LDO
LM3686TLE/TLXX-AAEF	1.8V_Bk
	1.2V_LILO
	3.0V_LDO

PIN DESCRIPTIONS

Pin Number	Symbol	Name and Function
A1	PGND	Power Ground pin
A2	SW	Switching node connection to the internal PFET switch and NFET synchronous rectifier.
A3	FB_DCDC	Feedback analog input for the DC-DC converter. Connect to the output filter capacitor.
B1	V_{BATT}	Power supply input for switcher. Connect to the input filter capacitor.
B2	EN_LILO	Enable input for the linear regulator. The linear regulator is in shutdown mode if voltage at this pin is < 0.4V and enabled if > 1.1V. Do not leave this pin floating.
B3	EN_DCDC	Enable input for the DC-DC converter. The DC-DC converter is in shutdown mode if voltage at this pin is < 0.4V and enabled if > 1.1V. Do not leave this pin floating.
C1	V_{IN_LDO}	Input power to LDO. (Must tie to V_{BATT} at all times)
C2	EN_LDO	Enable input for the linear regulator. The linear regulator is in shutdown mode if voltage at this pin is < 0.4V and enabled if > 1.1V. Do not leave this pin floating.
C3	QGND	Quiet GND pin for LDO and reference circuit.
D1	V_{OUT_LDO}	Voltage output of the linear regulator.
D2	V_{OUT_LILO}	Voltage output of the low input linear regulator
D3	V_{IN_LILO}	Input power to LILO (V_{IN_LILO} connects to output of DCDC or standalone).

Enable Combinations

EN_DCDC	EN_LILO	EN_LDO	Function
0	0	0	No Outputs
0	0	1	Linear Regulator enabled only (EN_LDO), supply from V_{IN_LDO}, I_{OUT_MAX} = 300 mA
0	1	0	Linear Regulator enabled only LILO supplies from V_{IN_LDO}, I_{OUT_MAX} = 50 mA, V_{IN_LDO} > = V_{OUT_LILO}
1	0	0	DC-DC converter enabled only
1	1	0	Linear Regulator & DCDC enabled 1) V_{IN_LILO} < V_{OUT_LILO} + 150 mV (typ.), the small NMOS device is active (I_{MAX} = 50 mA) and supplied by V_{IN_LDO}. 2) If V_{IN_LILO} > V_{OUT_LILO} + 250 mV (typ.), the large NMOS device is active (I_{MAX} = 350 mA) and supplied by V_{IN_LILO}. Maxium current of DC-DC when EN_LILO = High is 250 mA(1)(2)
1	1	1	DC-DC converter and linear regulator active. Linear regulator starts after DC-DC converter.

(1) The LILO is turned on via a small NMOS device supplied by V_{IN_LDO} . The maximum current is 50 mA when this small NMOS is ON. If higher current > 50 mA is desired the following condition must be done: EN_DC = HIGH .

(2) When the switcher is enabled, a transition occurs from the small NMOS to a larger NMOS. The transition occurs when V_{IN_LILO} > V_{OUT_LILO} + 250 mV. If V_{IN_LILO} < V_{OUT_LILO} + 150 mV, the LILO switches back to small NMOS (Switcher EN = low).

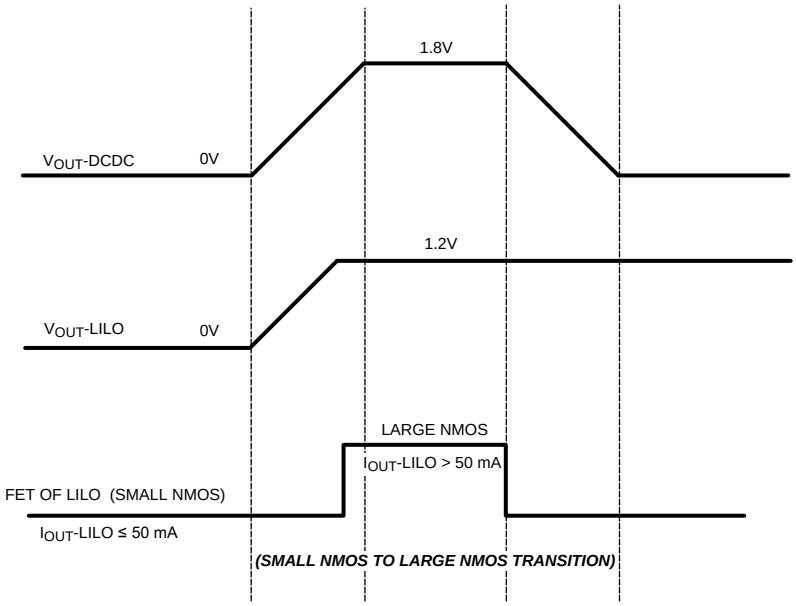


Figure 4. Mode Transition

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

V_{BATT} pin to GND and QGND	-0.2V to 6.0V
Enable pins, Feedback pins, SW pin	(GND-0.2V) to (V_{BATT}+0.2V) with 6.0V max
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature Range	-65°C to + 150°C
Continuous Power Dissipation[4]	Internally Limited
Maximum Lead Temperature (Soldering)	See[5]

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specfied. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).
(5) For detailed soldering specifications and information, see the TI AN-1112 Application Report (SNVA009).

Operating Ratings

Input Voltage Range V_{BATT} (DC-DC & LDO)	2.7V to 5.5V
Junction Temperature (T_J) Range	-40°C to + 125°C
Ambient Temperature (T_A) Range(1)	-40°C to + 85°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA})(1)	
DSBGA 12	120°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special attention must be paid to thermal dissipation issues in board design.

Electrical Characteristics
Linear Regulator — LILO (EN_DCDC = EN_LILO = ON - Large NMOS)(1)(2)(3)(4)

Limits in standard typeface are for T_A = 25°C. Limits appearing in **boldface** type apply over the full operating ambient temperature range: -40°C ≤ T_A= T_J ≤ +85°C. Unless otherwise noted, specifications apply to the closed loop typical application circuits (linear regulator) with $\mathbf{V_{IN\_LDO} = V_{BATT}}$ = 3.6V(5) , $V_{IN\_LILO} = V_{OUT\_DCDC(NOM)}$, $V_{EN\ (All)} = V_{BATT}$, C_{IN_DC} = 4.7 µF, C_{OUT_LILO} = 2.2 µF, C_{IN_LDO} = 1.0 µF , C_{OUT_LDO} = 1.0 µF ,$C_{OUT\_DC} = C_{IN\_LILO}$ = 10 µF

Symbol	Parameter	Condition	Limits			Units
			Min	Typ	Max	
ΔV_{OUT_LILO} / V_{OUT_LILO}	Output Voltage Accuracy, V_{OUT_LILO}	I_{OUT_LILO} = 1 mA to 350 mA $V_{IN\_LILO} = V_{OUT\_DCDC}$ V_{BATT} = 3.6V	**1.176**	1.2	**1.224**	V
ΔV_{OUT_LILO} / ΔmA	Load Regulation(6)	I_{OUT_LILO} = 1 mA & 350 mA $V_{IN\_LILO} = V_{OUT\_DCDC}$ V_{BATT} = 3.6V		4	**12**	µV/mA
V_{DROP}	Dropout Voltage(7)	$V_{BATT} = V_{OUT\_LILO}$ + 1.5V (V_{IN_LILO} disconnected from V_{OUT_DCDC}), I_{OUT} = 350 mA		50	**80**	mV
$I_{Q\_VIN\_LILO}$	Quiescent Current	$V_{BATT} = V_{IN\_LILO}$ = 3.6V		70	**90**	µA
I_{SC_LILO}	Short Circuit Current Limit	V_{OUT} = GND (V_{OUT_LILO} = 0)	**400**			mA

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical (typ.) numbers represent the most likely norm. Unless otherwise specified, conditions for typ. specifications are: V_{BATT} = 3.6V and T_A = 25°C.
(3) The parameters in the electrical characteristic table are tested at V_{BATT} = 3.6V unless otherwise specified. For performance over the input voltage range refer to datasheet curves.
(4) The input voltage range recommended for ideal applications performance for the specified output voltages is given below:V_{BATT} = 2.7V to 5.5V for 1.0V ≤ V_{OUT_DCDC} < 1.8VV_{BATT} = (V_{OUT_DCDC} + 1V) to 5.5V for 1.8V ≤ V_{OUT_DCDC} < 3.6V
(5) VIN_LDO must be ON at all time for biasing internal reference circuits
(6) To calculate the output voltage from the load regulation specified, use the following equation: ΔV_{OUT} = Load Regulation (%/mA) x Nominal V_{OUT} (V) x ΔI_{OUT} (mA).
(7) Dropout voltage is defined as the input to output voltage differential at which the output voltage falls to 100 mV below the nominal output voltage.

Electrical Characteristics
Linear Regulator — LILO (EN_DCDC = EN_LILO = ON - Large NMOS)(1)(2)(3)(4) (continued)

Limits in standard typeface are for T_A = 25°C. Limits appearing in **boldface** type apply over the full operating ambient temperature range: -40°C ≤ T_A= T_J ≤ +85°C. Unless otherwise noted, specifications apply to the closed loop typical application circuits (linear regulator) with $\mathbf{V_{IN\_LDO} = V_{BATT}}$ = 3.6V(5) , V_{IN_LILO} = $V_{OUT\_DCDC(NOM)}$, $V_{EN\ (All)}$ = V_{BATT}, C_{IN_DC} = 4.7 µF, C_{OUT_LILO} = 2.2 µF, C_{IN_LDO} = 1.0 µF , C_{OUT_LDO} = 1.0 µF ,C_{OUT_DC} = C_{IN_LILO} = 10 µF

Symbol	Parameter	Condition	Limits			Units
			Min	Typ	Max	
LILO (EN_DCDC = OFF, EN_LILO = ON - SMALL NMOS)						
ΔV_{OUT_LILO} / V_{OUT_LILO}	Output Voltage Accuracy, V_{OUT_LILO}	I_{OUT} = 1 mA to 50 mA	**1.176**		**1.224**	V
ΔV_{OUT_LILO} / ΔV_{BATT}	Line Regulation (Small NMOS)(8)	V_{IN_LILO} = (V_{OUT_LILO} + 0.3V) to 5.5V		0.4	**1.5**	mV/V
I_{SC_LILO}	Short circuit current	V_{OUT_LILO} = GND	**70**			mA
$T_{STARTUP}$	Start up time	EN to 0.95V_{OUT}		70		µS
System Characteristic(9)						
PSRR	Power Supply Rejection Ratio(10)	Signal to V_{BATT} = 3.6V, V_{IN_LILO} = 1.8V I_{OUT} = 200 mA, f = 100 Hz		68		dB
		Signal to V_{IN_LILO} = 1.8V I_{OUT} = 200 mA, f = 1kHz		60		
e_{N_LILO}	Output Noise voltage(10)	BW = 10 Hz to 100 kHz, V_{IN_LILO} = 1.8V, I_{OUT} = 200 mA, V_{IN_LDO} = 3.6V		166		μV_{RMS}
ΔV_{OUT_LILO}	Dynamic load transient response	Pulsed load 1 mA - 350 mA di/dt = 350 mA/1µS		+/- 30(11)		mV
ΔV_{IN_LILO}	Dynamic line transient response on V_{BATT}	V_{BATT} = 3.1V to 3.7V V_{IN_LILO} = V_{OUT_DCDC} tr, tf = 10 µS, I_{OUT} = 200 mA		+/-15(11)		mV

(8) To calculate the output voltage from the line regulation specified, use the following equation: ΔV_{OUT} = Line Regulation (%/V) x Nominal V_{OUT} (V) x ΔV_{IN} (V).
(9) Specified by design. Not production tested.
(10) The noise performance target is applied to PWM mode operation and this does not apply when DCDC converter is operating in PFM mode.
(11) For line and load transient specifications, the + symbol represents an overshoot in the output voltage and the – symbol represents an undershoot in the output voltage. The first value signifies overshoot or undershoot at the rising edge and the second value signifies the overshoot or undershoot at the falling edge.

Electrical Characteristics
Linear Regulator — LDO(1)(2)(3)(4)

Symbol	Parameter	Conditions	Typical Limit			Units
			Min	Typ	Max	
V_{IN_LDO}	LDO input voltage range		2.7		5.5	V
$\Delta V_{OUT\_LDO}/V_{OUT\_LDO}$	Output voltage accuracy, V_{OUT_LDO}	V_{IN} = 3.6V I_{OUT_LDO} = 1 mA & 300 mA	**2.744**	2.8	**2.856**	V
			2.94	3.0	3.06	
$\Delta V_{OUT\_LDO}/\Delta mA$	Load regulation(5)	I_{OUT_LDO} = 1 mA & 300 mA		8		µV/mA

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical (typ.) numbers represent the most likely norm. Unless otherwise specified, conditions for typ. specifications are: V_{BATT} = 3.6V and T_A = 25°C.
(3) The parameters in the electrical characteristic table are tested at V_{BATT} = 3.6V unless otherwise specified. For performance over the input voltage range refer to datasheet curves.
(4) The input voltage range recommended for ideal applications performance for the specified output voltages is given below:V_{BATT} = 2.7V to 5.5V for 1.0V ≤ V_{OUT_DCDC} < 1.8VV$_{BATT}$ = (V_{OUT_DCDC} + 1V) to 5.5V for 1.8V ≤ V_{OUT_DCDC} < 3.6V
(5) To calculate the output voltage from the load regulation specified, use the following equation: ΔV_{OUT} = Load Regulation (%/mA) x Nominal V_{OUT} (V) x ΔI_{OUT} (mA).

Electrical Characteristics
Linear Regulator — LDO[1][2][3][4] (continued)

Symbol	Parameter	Conditions	Typical Limit			Units
			Min	Typ	Max	
$\Delta V_{IN\_LDO}/\Delta V_{BATT}$	Line regulation[6]	V_{IN_LDO} = ($V_{OUT\_LDO(NOM)}$ + 0.3V) to 5.5V		0.2		mV/V
V_{DROP}	Dropout voltage[7]	I_{OUT} = 300 mA		120	**200**	mV
I_Q	Quiescent current	V_{en} = 0.95V, I_{OUT} = 0 mA		50	**80**	µA
I_{SC-LDO}	Short circuit current limit	V_{OUT} = GND	**350**			mA
System Characteristic[8]						
PSRR	Power supply rejection ratio	EN_DC = EN_LILO = GND f = 1 kHz, I_{OUT} = 200 mA		85		dB
		f = 10 kHz, I_{OUT} = 200 mA Signal to V_{IN_LDO} = 3.6V		70		
e_{N_LDO}	Output noise voltage[9]	BW = 10 Hz to 100 kHz, V_{IN_LDO} = 3.6V I_{OUT} = 200 mA		6.7		μV_{RMS}
ΔV_{IN_LDO}	Dynamic line transient response	V_{IN_LDO} = 3.8V to 4.4V tr, tf = 30 µs I_{OUT} = 1 mA		+/-2[10]		mV
ΔV_{OUT_LDO}	Dynamic load transient response	Pulsed load 1 mA & 300 mA tr, tf = 10 µs		+/-30[10]		mV

(6) To calculate the output voltage from the line regulation specified, use the following equation: ΔV_{OUT} = Line Regulation (%/V) x Nominal V_{OUT} (V) x ΔV_{IN} (V).
(7) Dropout voltage is defined as the input to output voltage differential at which the output voltage falls to 100 mV below the nominal output voltage.
(8) Specified by design. Not production tested.
(9) The noise performance target is applied to PWM mode operation and this does not apply when DCDC converter is operating in PFM mode.
(10) For line and load transient specifications, the + symbol represents an overshoot in the output voltage and the – symbol represents an undershoot in the output voltage. The first value signifies overshoot or undershoot at the rising edge and the second value signifies the overshoot or undershoot at the falling edge.

Electrical Characteristics
DC-DC Converter[1][2][3][4]

Symbol	Parameter	Conditions	Limit			Units
			Min	Typ	Max	
V_{FB_DCDC}	Feedback Voltage Accuracy	PWM Mode[5]	**1.746**	1.8	**1.836**	V
V_{REF}	Internal reference voltage			0.5		V
$R_{DSON(P)}$	Pin-Pin Resistance for PFET	V_{BATT} = 3.6V I_{SW} = 100 mA		350	450	mΩ
$R_{DSON(N)}$	Pin-Pin Resistance for NFET	V_{BATT} = 3.6V I_{SW} = 100 mA		150	250	mΩ
I_{Q_AUTO}	Quiescent current for auto mode	No load, device is not switching, FB = HIGH		28	**40**	µA
I_{LIM}	Switch peak current limit	Open loop	**1.035**	1.220	**1.375**	A
F_{OSC}	Internal Oscillator Frequency	PWM Mode	**2.4**	3	**3.4**	MHz

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical (typ.) numbers represent the most likely norm. Unless otherwise specified, conditions for typ. specifications are: V_{BATT} = 3.6V and T_A = 25°C.
(3) The parameters in the electrical characteristic table are tested at V_{BATT} = 3.6V unless otherwise specified. For performance over the input voltage range refer to datasheet curves.
(4) The input voltage range recommended for ideal applications performance for the specified output voltages is given below:V_{BATT} = 2.7V to 5.5V for 1.0V ≤ V_{OUT_DCDC} < 1.8VV_{BATT} = (V_{OUT_DCDC} + 1V) to 5.5V for 1.8V ≤ V_{OUT_DCDC} < 3.6V
(5) Electrical Characteristic table reflects open loop data (FB = 0V and current drawn from SW pin ramped up until cycle by cycle current limit is activated). Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

Electrical Characteristics
Global Parameters (DCDC, LILO, & LDO)[1][2][3][4]

Symbol	Parameter	Conditions	Typical Limit			Units
			Min	Typ	Max	
I_{Q_VBATT}	Quiescent current into V_{BATT}	Full power mode I_{OUT_DCDC} = I_{OUT_LILO} = I_{OUT_LDO} = 0 mA, DC-DC is not switching (FB_DCDC forced higher than V_{OUT_DCDC}) V_{en} = 1.1V,		100	**130**	µA
I_{Q_GLOBAL}	Shutdown current into V_{BATT}	V_{EN_DCDC} = V_{EN_LILO} = V_{EN_LDO} = 0V		2.5	**4**	µA
Enable Pins (EN_DCDC, EN_LILO, EN_LDO)						
I_{EN}	Enable pin input current	All EN = 0V		.01	**1**	µA
V_{IH}	Logic high input		**1.1**			V
V_{IL}	Logic low input				**0.40**	V

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical (typ.) numbers represent the most likely norm. Unless otherwise specified, conditions for typ. specifications are: V_{BATT} = 3.6V and T_A = 25°C.
(3) The parameters in the electrical characteristic table are tested at V_{BATT} = 3.6V unless otherwise specified. For performance over the input voltage range refer to datasheet curves.
(4) The input voltage range recommended for ideal applications performance for the specified output voltages is given below:V_{BATT} = 2.7V to 5.5V for 1.0V ≤ V_{OUT_DCDC} < 1.8VV_{BATT} = (V_{OUT_DCDC} + 1V) to 5.5V for 1.8V ≤ V_{OUT_DCDC} < 3.6V

Typical Performance Characteristics

Unless otherwise specified, typical application (post regulation), V_{BATT} = 3.6V, T_A = 25°C, enable pins tied to V_{BATT}, V_{OUT_DCDC} = 1.8V, V_{OUT_LILO} = 1.2V, V_{OUT_LDO} = 2.8V

V_{OUT_DCDC} vs. I_{OUT_DCDC}

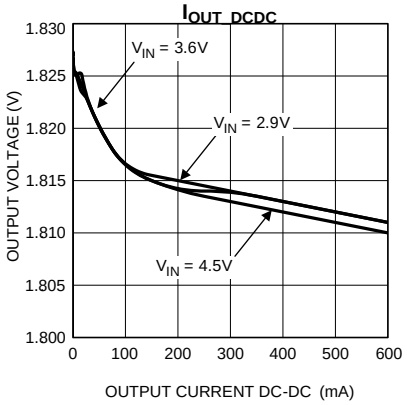


Figure 5.

V_{OUT_LILO} vs. I_{OUT_LILO}

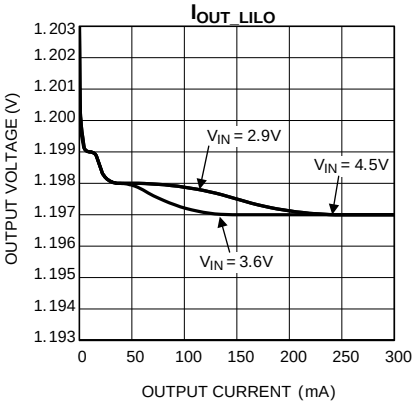


Figure 6.

Efficiency DC-DC vs. Output Current LILO and LDO disabled

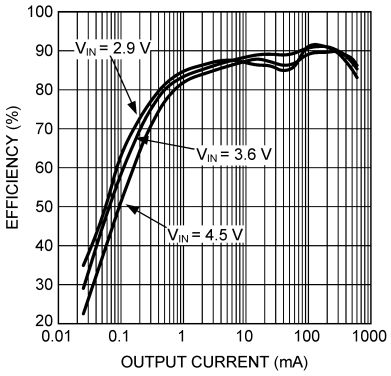


Figure 7.

PSRR vs. Frequency (LILO - VIN_LILO = 3.6V)

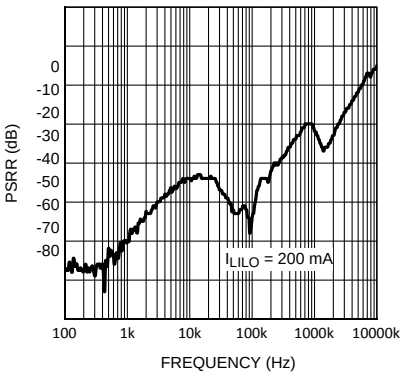


Figure 8.

PSRR vs. Frequency (LDO - VIN_LDO = 3.6V)

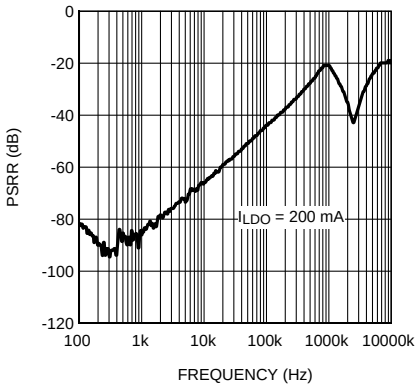


Figure .

Noise vs. Frequency (LDO - VIN_LDO = 3.6V)

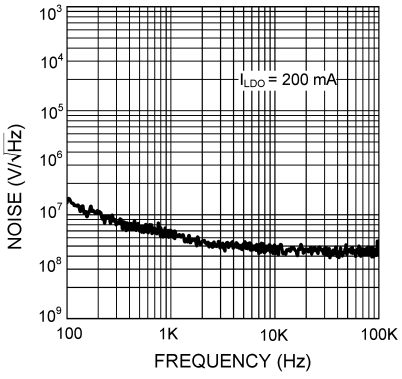


Figure 9.

Typical Performance Characteristics (continued)

Unless otherwise specified, typical application (post regulation), V_{BATT} = 3.6V, T_A = 25°C, enable pins tied to V_{BATT}, V_{OUT_DCDC} = 1.8V, V_{OUT_LILO} = 1.2V, V_{OUT_LDO} = 2.8V

Switching Frequency vs. Temperature

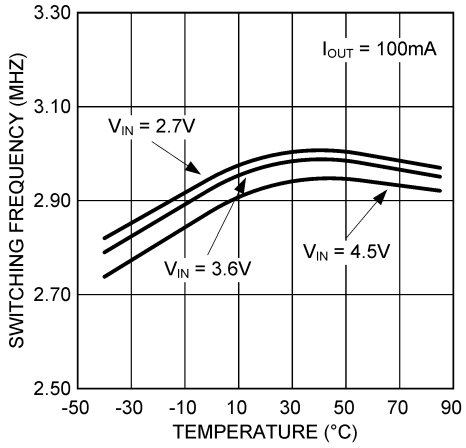


Figure 10.

Current Limit vs. Temperature (Open Loop)

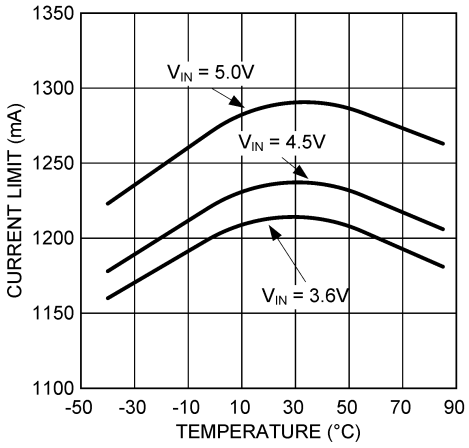


Figure 11.

R_{DSON} vs. Temperature

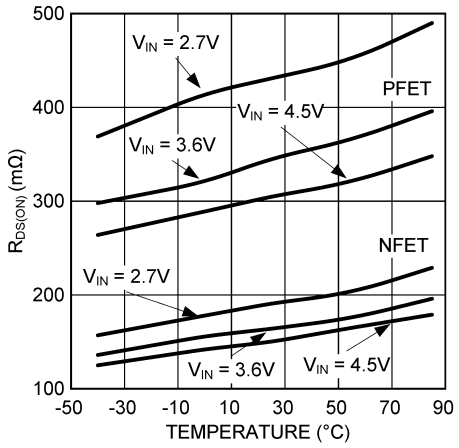


Figure 12.

Startup (all three enables tied together)

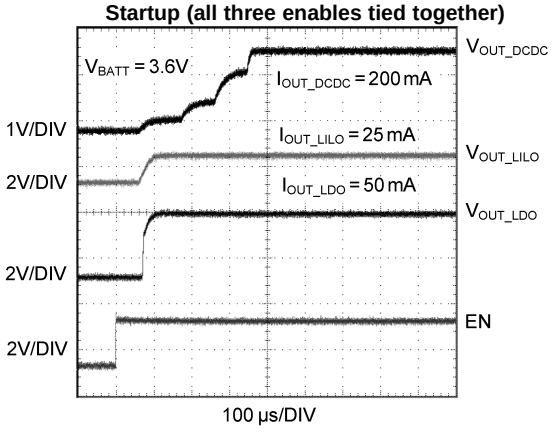


Figure 13.

V_{BATT} Line Transient Response

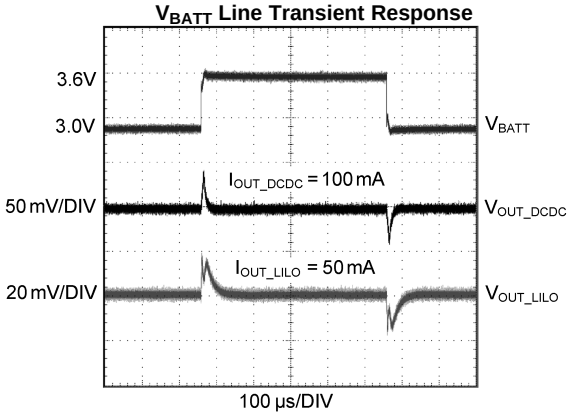


Figure 14.

Line Transient Response

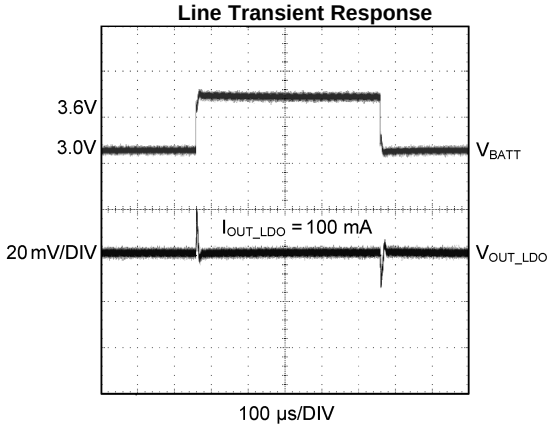


Figure 15.

Typical Performance Characteristics (continued)

Unless otherwise specified, typical application (post regulation), V_{BATT} = 3.6V, T_A = 25°C, enable pins tied to V_{BATT}, V_{OUT_DCDC} = 1.8V, V_{OUT_LILO} = 1.2V, V_{OUT_LDO} = 2.8V

Load Transient Response DC-DC (PWM Mode: 100mA to 350mA)

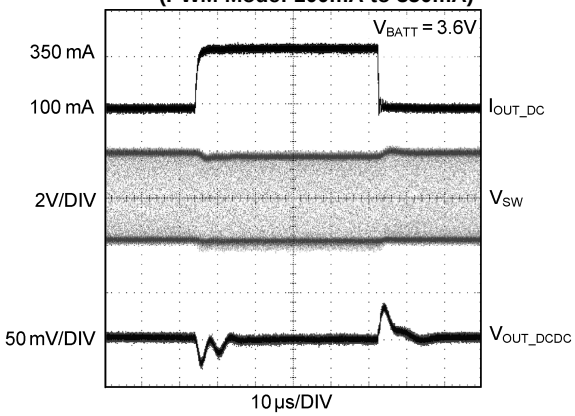


Figure 16.

Load Transient Response DC-DC (PFM Mode: 1mA to 150mA)

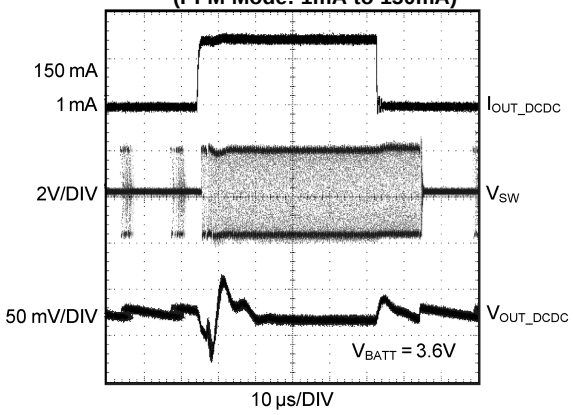


Figure 17.

Load Transient Response LILO 50mA to 250mA

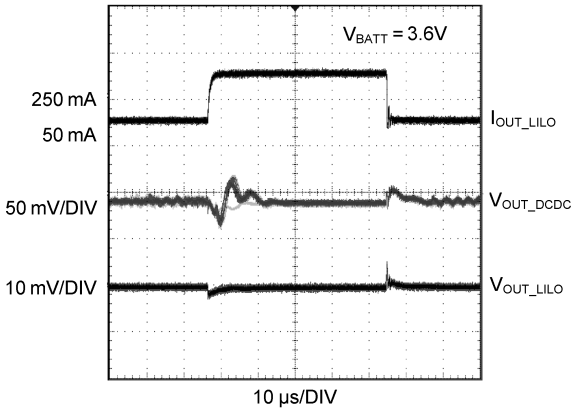


Figure 18.

Load Transient Response LDO 100mA to 250mA

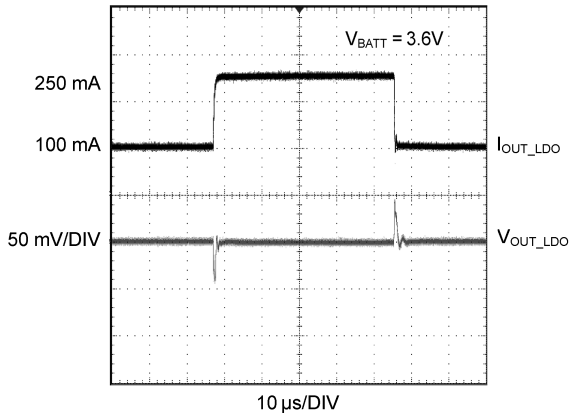


Figure 19.

Operation Description

DEVICE INFORMATION

The LM3686 incorporates a high efficiency synchronous switching step-down DC-DC converter, a very low dropout linear regulator (LILO), and ultra low noise linear regulator.

The DC-DC converter delivers a constant voltage from a single Li- Ion battery and input voltage rails from 2.7V to 5.5V to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, it has the ability to deliver up to 600 mA load current (when not powering the LILO) depending on the input voltage, output voltage, ambient temperature and the inductor chosen.

The linear regulator delivers a constant voltage biased from V_{IN_LILO} power input typically the output voltage of the DC-DC converter is used (post regulation) with a maximum load current of 350 mA.

The other linear regulator delivers a constant voltage biased from V_{IN_LDO} power input - with a maximum load current of 300 mA.

Three enable pins allow the independent control of the three outputs. Shutdown mode turns off the device, offering the lowest current consumption ($I_{SHUTDOWN}$ = 2.5 µA typ).

Besides the shutdown feature, for the DC-DC converter there are two more modes of operation depending on the current required:

- PWM (Pulse Width Modulation), and

- PFM (Pulse Frequency Modulation).

The device operates in PWM mode at load current of approximately 80 mA or higher. Lighter load current cause the device to automatically switch into PFM for reduced current consumption (I_{Q_VBATT} = 28 µA typ) and a longer battery life.

Additional features include soft-start, startup mode of the linear regulator, under-voltage protection, current overload protection, and over-temperature protection.

An internal reference generates a 1.8V biasing an internal resistive divider to create a reference voltage range from 0.7V to 1.8V (in 50 mV steps) for the LILO and the 0.5V reference used for the DC-DC converter. The ultra low noise linear regulator also has internal reference that generates a 1.8V biasing for a internal resistor divider. Thus, creating a reference voltage ranging from 1.5V to 3.3V

The Under-voltage lockout feature enables the device to startup once V_{BATT} has reached 2.65V typically and turns the device off if V_{BATT} drops below 2.41V typically.

Post Regulation Note:

In the case that the DC-DC converter is switched off while the Linear Regulator is still enabled, the LILO can still support up to 50 mA. The linear regulator LILO is turned on via a small NMOS device supplied by V_{IN_LDO} . The maximum current is 50 mA when this small NMOS is ON. If higher current > 50 mA is desired the following condition must be done:

1) EN_DC = HIGH

When the condition is met, the LILO transitions to the large NMOS and can support up to 350 mA.

DC-DC CONVERTER OPERATION

During the first part of each switching cycle, the control block in the LM3686 turns on the internal PFET switch. This allows current to flow from the input V_{BATT} through the switch pin SW and the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of (V_{BATT} - V_{OUT_DCDC}) / L, by storing energy in the magnetic field.

During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of (- V_{OUT_DCDC} / L).

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM Operation

During PWM (Pulse Width Modulation) operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependency, feed forward inversely proportional to the input voltage is introduced.

While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the duty-cycle-comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

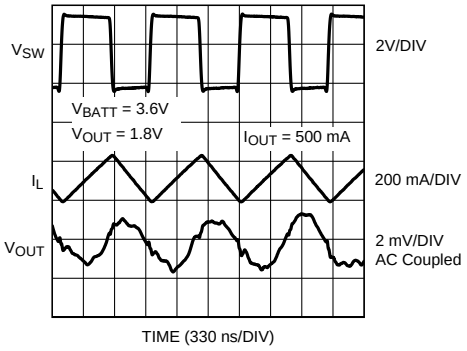


Figure 20. Typical PWM Operation

Internal Synchronous Rectification

While in PWM mode, the DC-DC converter uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Current Limiting

A current limit feature allows the LM3686 to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 1220mA (typ). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold. This allows the inductor current more time to decay, thereby preventing runaway.

PFM Operation

At very light load, the DC-DC converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency. The part automatically transitions into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

A. The NFET current reaches zero.

B. The peak PMOS switch current drops below the I_{MODE} level, (typically $I_{MODE} < 75\ mA + V_{BATT} / 55\Omega$).

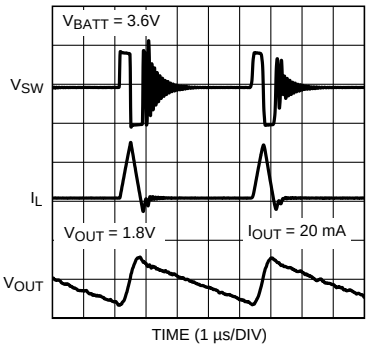


Figure 21. Typical PFM Operation

During PFM operation, the DC-DC converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between ~0.2% and ~1.8% above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is: I_{PFM} = 112 mA + V_{BATT} / 20Ω.

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see Figure 22), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is 28µA (typ), which allows the part to achieve high efficiency under extremely light load conditions.

If the load current should increase during PFM mode (see Figure 22) causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode.

When V_{BATT} = 2.7V the part transitions from PWM to PFM mode at ~35 mA output current and from PFM to PWM mode at ~95 mA , when V_{BATT}= 3.6V, PWM to PFM transition happens at ~42 mA and PFM to PWM transition happens at ~115 mA, when V_{BATT} = 4.5V, PWM to PFM transition happens at ~60 mA and PFM to PWM transition happens at ~135 mA.

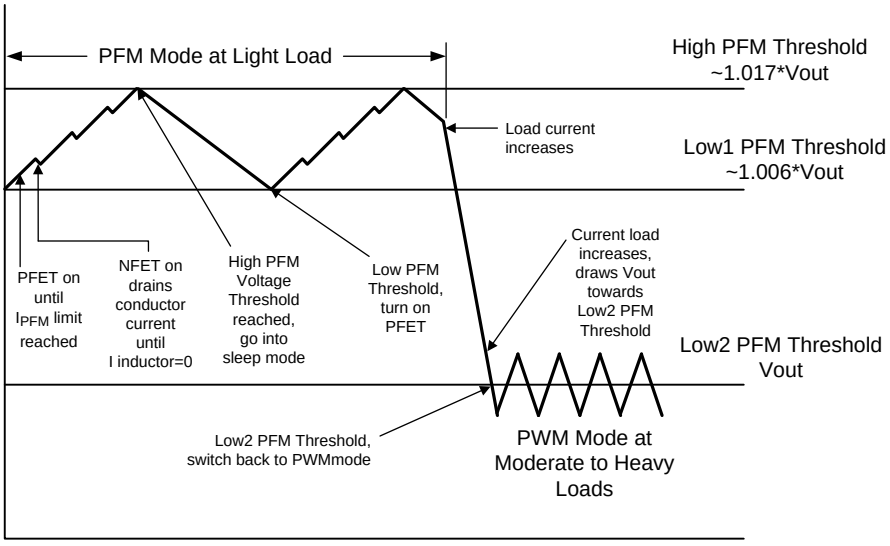


Figure 22. Operation in PFM Mode and Transfer to PWM Mode

Soft Start

The DC-DC converter has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN_DCDC goes from logic low to logic high after V_{BATT} reaches 2.7V. Soft start is implemented by increasing switch current limit in steps of 200 mA, 400 mA, 600 mA and 1220 mA (typical switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up. Typical start-up times with a 10 µF output capacitor and 200 mA load is 350 µs and with 1 mA load is 200 µs.

LINEAR REGULATOR OPERATION (LILO)

In the typical post regulation application the power input voltage V_{IN_LILO} for the linear regulator is generated by the DC-DC converter. Using a buck converter to reduce the battery voltage to a lower input voltage for the linear regulator translates to higher efficiency and lower power dissipation.

It's also possible to operate the linear regulator independent of the DC-DC converter output voltage either from V_{IN_LDO}/V_{BATT} or from a different source (V_{IN_LILO}) - (I_{OUT_LILO} = 50 mA max in independent mode).

An input capacitor of 1 µF at V_{IN_LILO} is needed to be added if no other filter or bypass capacitor is present in the V_{IN_LILO} path.

Startup Mode

If $V_{IN\_LILO} > V_{OUT\_LILO(NOM)}$ + 250 mV the main regulator is active, offering a rated output current of 350 mA and supplied by V_{IN_LILO}. (Large NMOS)

If $V_{IN\_LILO} < V_{OUT\_LILO(NOM)}$ + 150 mV the startup LILO is active, providing a reduced rated output current of 50 mA typical, supplied by V_{BATT}. (Small NMOS)

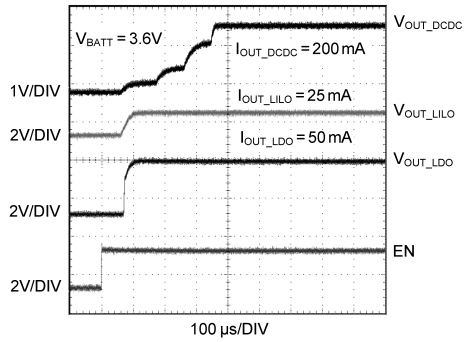


Figure 23. Startup Sequence, $V_{EN\_DCDC} = V_{EN\_LILO} = V_{EN\_LDO} = V_{BATT}$

Current Limiting (LDO and LILO)

The LM3686 incorporates also a current limit for the LDO and LILO to protect itself and external components during overload conditions at their outputs. In the event of a peak over-current condition at V_{OUT_LDO} or V_{OUT_LILO} the output current through the NFET pass device will be limited.

APPLICATION INFORMATION

Application Selection

It is strongly recommended to select the required components of LM3686 as described within the datasheet. If other components are selected, the device will not perform up to standard and electrical characteristics cannot be ensured.

Inductor Selection

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. **The minimum value of inductance to ensure good performance is 0.7 µH at I_{LIM} (typ) dc current over the ambient temperature range.** Shielded inductors radiate less noise and should be preferred. There are two methods to choose the inductor saturation current rating.

METHOD 1

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as:

$$I_{SAT} > I_{OUT\_DCDC\_MAX} + I_{RIPPLE} \quad (1)$$

where

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{where } I_{RIPPLE} = \left(\frac{V_{BATT} - V_{OUT}}{2 \times L}\right) \times \left(\frac{V_{OUT}}{V_{BATT}}\right) \times \left(\frac{1}{f}\right)$$

- I_{RIPPLE}: average to peak inductor current
- $I_{OUT\_DCDCMAX}$: maximum load current (600 mA)
- V_{BATT}: maximum input voltage in application
- L: minimum inductor value including worst case tolerances (30% drop can be considered for method 1)
- f: minimum switching frequency (2.55 MHz) (2)

METHOD 2

A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit of 1375 mA.

A 1.0 µH inductor with a saturation current rating of at least 1375 mA is recommended for most applications. The inductor's resistance should be less than 0.3Ω for good efficiency. Table 1 lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded- bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost bobbin models is unacceptable.

Table 1. Suggested Inductors and their Suppliers

Model	Vendor	Dimensions LxWxH (mm)	DCR (max)
BRL2518T1R0M	TAIYO YUDEN	2.5 X 1.8 X 1.2	80
MDT2520CR1R0M	TOKO	2.5 X 2.0 X 1.0	80
KSLI252010AG1R0	HITACHI METALS	2.5 X 2.0 X 1.0	75

External Capacitors

As common with most regulators, the LM3686 requires external capacitors to ensure stable operation. The LM3686 is specifically designed for portable applications requiring minimum board space and the smallest size components. These capacitors must be correctly selected for good performance.

Input Capacitor Selection

$C_{IN\_DC\text{-}DC}$

A ceramic input capacitor of 4.7 µF, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the V_{BATT} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The minimum input capacitance to ensure good performance is 2.2 µF at 3V dc bias; 1.5 µF at 5V dc bias including tolerances and over ambient temperature range. The input filter capacitor supplies current to the PFET switch of the LM3686 DC-DC converter in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} \times \sqrt{\frac{V_{OUT}}{V_{BATT}} \times \left(1 - \frac{V_{OUT}}{V_{BATT}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{BATT} - V_{OUT}) \times V_{OUT}}{L \times f \times I_{OUTMAX} \times V_{BATT}}$$

The worst case is when $V_{BATT} = 2 \times V_{OUT}$ (3)

C_{IN_LILO}

If the LILO is used as post regulation no additional capacitor is needed at V_{IN_LILO} as the output filter capacitor of the DC-DC converter is close by and therefore sufficient.

In case of independent mode use, a 1.0 µF ceramic capacitor is recommended at V_{IN_LILO} if no other filter capacitor is present in the V_{IN_LILO} supply path. This capacitor must be located a distance of not more than 1 cm from the V_{IN_LILO} input pin and returned to QGND.

C_{IN_LDO}

An input capacitor is required for stability. It is recommended to use a 1 µF ceramic capacitor and connected between the V_{IN_LDO} and QGND.

Output Capacitor

C_{OUT_DCDC}

A ceramic output capacitor of 10 µF, 6.3V is sufficient for most applications. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process.

The minimum output capacitance to ensure good performance is 5.75 µF at 1.8V DC bias including tolerances and over ambient temperature range. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and by the R_{ESR} and can be calculated as:

Voltage peak-to-peak ripple due to capacitance can be expressed as follow:

$$V_{PP\text{-}C} = \frac{I_{RIPPLE}}{4 \times f \times C} \quad (4)$$

Voltage peak-to-peak ripple due to ESR can be expressed as follow:

$$V_{PP\text{-}ESR} = (2 * I_{RIPPLE}) * R_{ESR} \quad (5)$$

Because these two components are out of phase, the rms (root mean squared) value can be used to get an approximate value of peak-to-peak ripple. The peak-to-peak ripple voltage, rms value can be expressed as follow:

$$V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^{2} + V_{PP\text{-}ESR}^{2}} \quad (6)$$

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}). The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

C_{OUT_LILO}

The linear regulator is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types X7R, Z5U, or Y5V) in the 2.2 µF range (up to 10 µF) and with an ESR between 3 mΩ to 300 mΩ is suitable as C_{OUT_LIN} in the LM3686 application circuit.

This capacitor must be located a distance of not more than 1cm from the V_{OUT_LILO} pin and returned to a clean analogue ground. It is also possible to use tantalum or film capacitors at the device output, V_{OUT_LILO} but these are not as attractive for reasons of size and cost (see Table 2).

C_{OUT_LDO}

A ceramic capacitor in the 1 uF to 2.2 uF range, and with ESR between 5 mΩ to 500 mΩ, is suitable for the linear regulator. This output capacitor should be connected no more than 1 cm from V_{OUT_LDO} and QGND

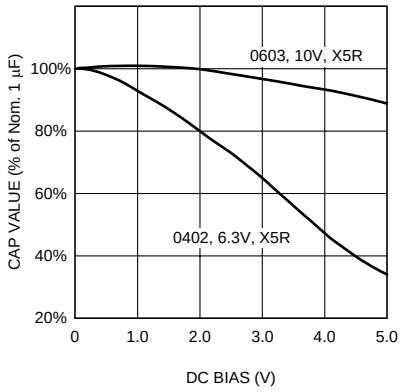


Figure 24. Graph Showing a Typical Variation In Capacitance vs. DC Bias

Table 2. Suggested Capacitors and their Suppliers

Capacitance / µF	Model	Voltage Rating	Vendor	Type	Case Size / Inch (mm)
10.0	C1608X5R0J106K	6.3V	TDK	Ceramic, X5R	0603 (1608)
4.7	C1608X5R0J475	6.3V	TDK	Ceramic, X5R	0603 (1608)
2.2	C1608X5R0J225M	6.3V	TDK	Ceramic, X5R	0603 (1608)
1.0	C1005JB0J105KT	6.3V	TDK	Ceramic, X5R	0402 (1005)

DSBGA Package Assembly And Use

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in the TI AN-1112 Application Report (SNVA009). Refer to the section "Surface Mount Technology (SMD) Assembly Considerations". For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the soldermask and pad overlap, from holding the device off the

surface of the board and interfering with mounting. See TI AN-1112 Application Report (SNVA009) for specific instructions how to do this. The 12-bump package used for LM3686 has 300 micron solder balls and requires 275 micron pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should not exceed 183 micron, for a section approximately 183 micron long or longer, as a thermal relief. Then each trace should neck up or down to its optimal width. The important criteria is symmetry. This ensures the solder bumps on the LM3686 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A1, A2, C1 and B3, because PGND, SGND, V_{BATT} and V_{IN_LIN} are typically connected to large copper planes, inadequate thermal relief can result in late or inadequate re-flow of these bumps. The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with frontside shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light, in the red and infrared range, shining on the package's exposed die edges.

Board Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Good layout for the LM3686 can be implemented by following a few simple design rules below.

1. Place the LM3686, inductor and filter capacitor close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{BATT} and PGND pin. Place the output capacitor of the linear regulator close to the output pin.
2. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor through the LM3686 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the LM3686 by the inductor to the output filter capacitor and then back through ground forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. Connect the ground pins of the LM3686 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3686 by giving it a low impedance ground connection. Route SGND to the ground-plane by a separate trace.
4. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
5. Route noise sensitive traces, such as the voltage feedback path (FB_DCDC), away from noisy traces between the power components. The voltage feedback trace must remain close to the LM3686 circuit and should be direct but should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed.
6. Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry. Interference with noise sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal plane; power to it is post-regulated to reduce conducted noise, a good field of application for the on-chip low-dropout linear regulator.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3686TLE-AADW/NOPB	ACTIVE	DSBGA	YZR	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SUEB	Samples
LM3686TLE-AAED/NOPB	ACTIVE	DSBGA	YZR	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SXTB	Samples
LM3686TLE-AAEF/NOPB	ACTIVE	DSBGA	YZR	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SXZB	Samples
LM3686TLX-AADW/NOPB	ACTIVE	DSBGA	YZR	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SUEB	Samples
LM3686TLX-AAED/NOPB	ACTIVE	DSBGA	YZR	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SXTB	Samples
LM3686TLX-AAEF/NOPB	ACTIVE	DSBGA	YZR	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SXZB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

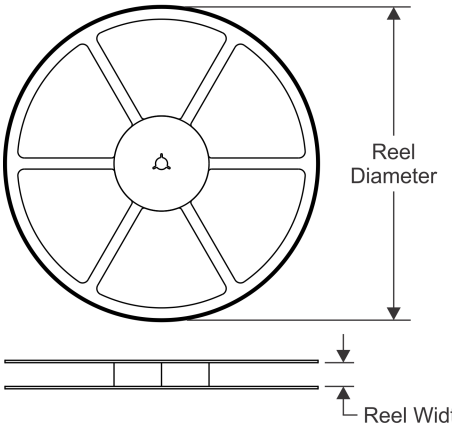
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

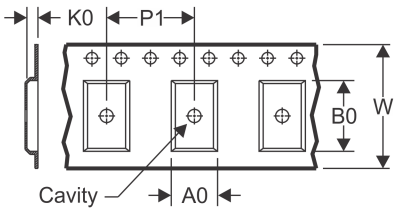
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

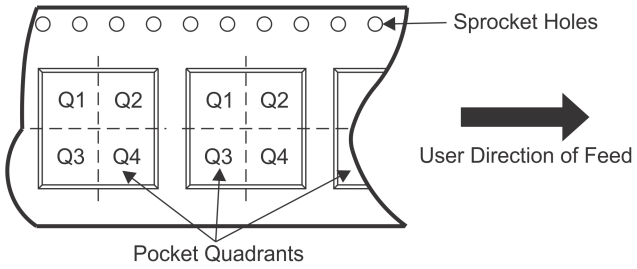


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

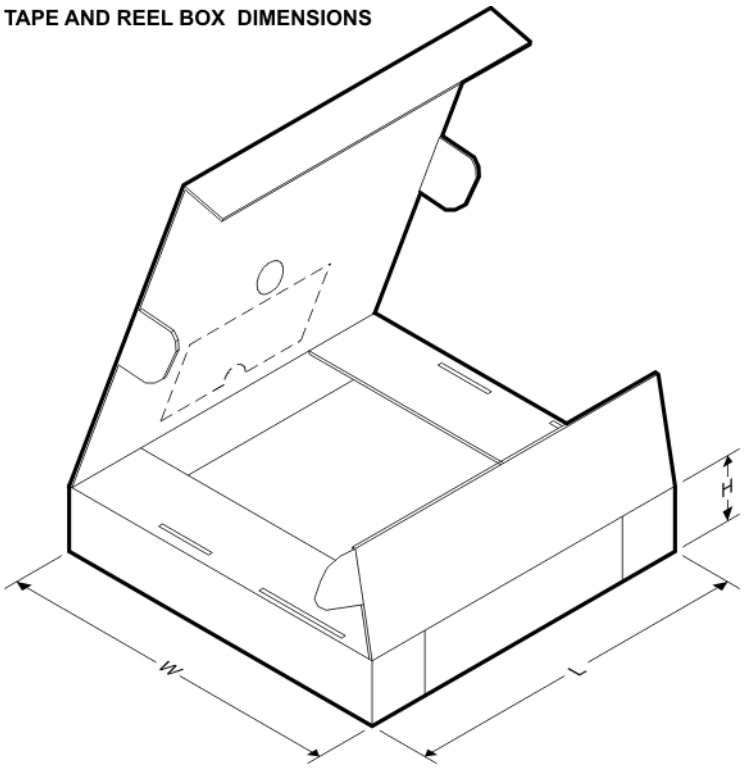
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3686TLE-AADW/NOPB	DSBGA	YZR	12	250	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LM3686TLE-AAED/NOPB	DSBGA	YZR	12	250	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LM3686TLE-AAEF/NOPB	DSBGA	YZR	12	250	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LM3686TLX-AADW/NOPB	DSBGA	YZR	12	3000	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LM3686TLX-AAED/NOPB	DSBGA	YZR	12	3000	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LM3686TLX-AAEF/NOPB	DSBGA	YZR	12	3000	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1

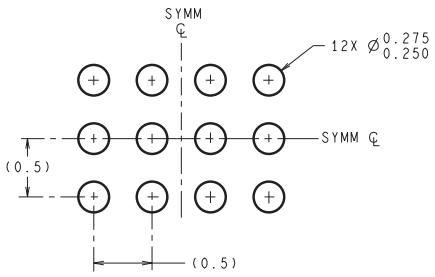
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

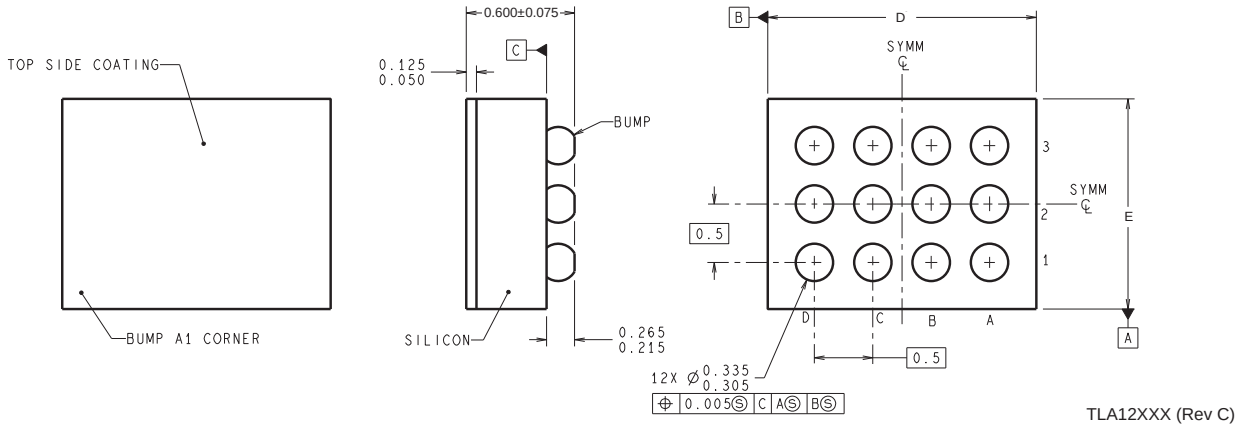
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3686TLE-AADW/NOPB	DSBGA	YZR	12	250	210.0	185.0	35.0
LM3686TLE-AAED/NOPB	DSBGA	YZR	12	250	210.0	185.0	35.0
LM3686TLE-AAEF/NOPB	DSBGA	YZR	12	250	210.0	185.0	35.0
LM3686TLX-AADW/NOPB	DSBGA	YZR	12	3000	210.0	185.0	35.0
LM3686TLX-AAED/NOPB	DSBGA	YZR	12	3000	210.0	185.0	35.0
LM3686TLX-AAEF/NOPB	DSBGA	YZR	12	3000	210.0	185.0	35.0

YZR0012



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



TLA12XXX (Rev C)

D: Max = 2.465 mm, Min =2.405 mm

E: Max = 1.717 mm, Min =1.656 mm

4215049/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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