High-Efficiency Three-String White LED Driver

Check for Samples: LM3697

FEATURES

- **Drives Three Parallel High-Voltage LED Strings for Display and Keypad Lighting**
- **High-Voltage Strings Capable of up to 40V Output Voltage and up to 90% Efficiency**
- **Up to 30 mA per Current Sink**
- **11-Bit Configurable Dimming Resolution**
- **PWM Input for Content Adjustable Brightness Control (CABC)**
- **Fully Configurable LED Grouping and Control**
- **Four Configurable Over-Voltage Protection Thresholds (16V, 24V, 32V, and 40V)**
- **Selectable 500 kHz and 1MHz Switching Frequency**
- **30 mm^2 Total Solution Size**

APPLICATIONS

- **Power Source for Smart Phone Illumination**
- **Display, Keypad and Indicator Illumination**

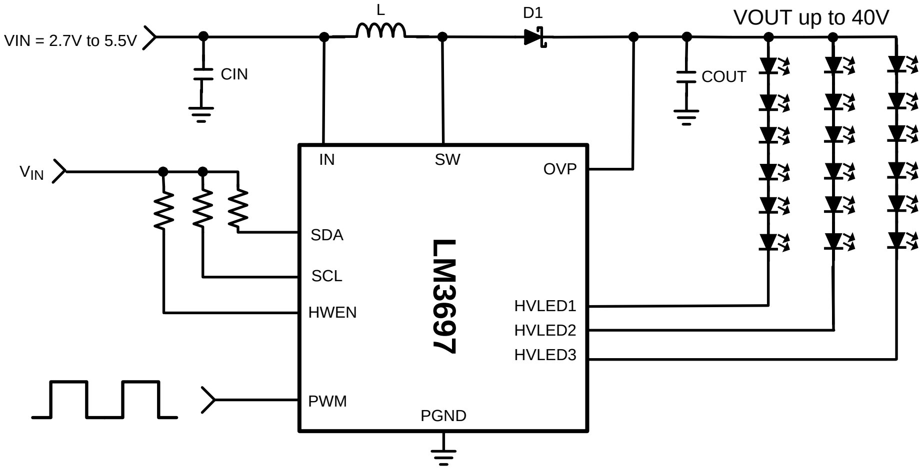
DESCRIPTION

The LM3697 is a high-efficiency three string power source for backlight or keypad LEDs in smart-phone handsets. The high-voltage inductive boost converter provides the power for three series LED strings for display backlight and keypad functions (HVLED1, HVLED2 and HVLED3).

An additional feature is a Pulse Width Modulation (PWM) control input for content adjustable backlight control, which can be used to control any high-voltage current sink.

The LM3697 is fully configurable via an I^{2}C-compatible interface. The device is available in a 12-bump (1.26 mm ± 30 µm x 1.61 mm ± 30 µm x 0.6 mm ± 75 um) DSBGA and operates over a 2.7V to 5.5V input voltage range and a −40°C to +85°C temperature range.

Typical Application Circuit



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Application Circuit Component List

Component	Manufacturer	Value	Part Number	Size (mm)	Current/Voltage Rating (Resistance)
L	TDK	10 µH	VLF302512MT-100M	2.5 mm x 3.0 mm x 1.2 mm	620 mA/0.25Ω
COUT	TDK	1 µF	C2012X5R1H105	0805	50V
CIN	TDK	2.2 µF	C1005X5R1A225	0402	10V
Diode	On-Semi	Schottky	NSR0240V2T1G	SOD-523	40V, 250 mA

Connection Diagram

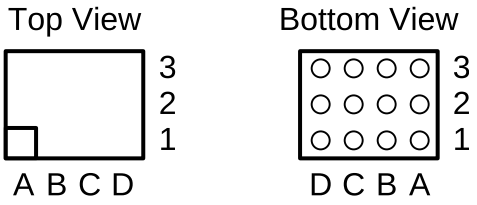

Figure 1. 12-Bump DSBGA Package YFQ0012CAA

Pin Descriptions/Functions

Pin	Name	Description
A1	PWM	PWM Brightness Control Input for CABC operation. PWM is a high-impedance input and cannot be left floating, if not used connect to GND.
A2	SDA	Serial Data Connection for I^2C-Compatible Interface.
A3	HWEN	Hardware enable input. Drive this pin high to enable the device. Drive this pin low to force the device into a low power shutdown. HWEN is a high-impedance input and cannot be left floating.
B1	HVLED1	Input Terminal to high-voltage Current Sink #1 (40V max). The boost converter regulates the minimum of HVLED1, HVLED2 and HVLED3 to V_{HR}.
B2	SCL	Serial Clock Connection for I^2C-Compatible Interface.
B3	IN	Input Voltage Connection. Bypass IN to GND with a minimum 2.2 µF ceramic capacitor.
C1	HVLED2	Input Terminal to high-voltage Current Sink #2 (40V max). The boost converter regulates the minimum of HVLED1, HVLED2 and HVLED3 to V_{HR}.
C2	GND	Ground
C3	GND	Ground
D1	HVLED3	Input Terminal to high-voltage Current Sink #3 (40V max). The boost converter regulates the minimum of HVLED1, HVLED2 and HVLED3 to V_{HR}.
D2	OVP	Over-Voltage Sense Input. Connect OVP to the positive terminal of the inductive boost's output capacitor (COUT).
D3	SW	Drain Connection for the internal NFET. Connect SW to the junction of the inductor and the Schottky diode anode.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS (1) (2)

V_{IN} to GND	−0.3V to +6V
V_{SW}, V_{OVP}, V_{HVLED1}, V_{HVLED2}, V_{HVLED3} to GND	−0.3V to +45V
V_{SCL}, V_{SDA}, V_{PWM} to GND	−0.3V to +6V
V_{HWEN} to GND	−0.3V to +6V
Continuous Power Dissipation	Internally Limited
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	− 65°C to +150°C
Maximum Lead Temperature (Soldering)	(3)
ESD Rating Human Body Model (4) Charged Device Model (5)	 2.0kV 1500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) For detailed soldering specifications and information, please refer to Texas Instruments Application Note 1112: DSBGA Wafer Level Chip Scale Package (SNVA009) available at www.ti.com.
(4) ESD Human Body Model, ESD-HBM JESD22-A114.
(5) ESD Charged Device Model, ESD-CDM JESD22-C101.

OPERATING RATINGS (1) (2)

V_{IN} to GND	2.7V to 5.5V
V_{SW}, V_{OVP}, V_{HVLED1}, V_{VHLED2}, V_{HVLED3} to GND	0V to +40V
Junction Temperature Range (T_J) (3) (4)	−40°C to +125°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=+140°C (typ.) and disengages at T_J=+125°C (typ.).
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

THERMAL PROPERTIES

Thermal Resistance Junction to Ambient (θ_{JA})(1)	55.3°C/W

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102 mm x 76 mm x 1.6 mm with a 2 x 1 array of thermal vias. The ground plane on the board is 50 mm x 50 mm. Thickness of copper layers are 36 µm/18 µm/18 µm/36 µm (1.5 oz/1oz/1oz/1.5 oz). Ambient temperature in simulation is 22°C in still air. Power dissipation is 1W. The value of θ_{JA} of this product in the DSBGA package could fall in a range as wide as 60°C/W to 110°C/W (if not wider), depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists special care must be paid to thermal dissipation issues.

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ELECTRICAL CHARACTERISTICS (1) (2)

Limits in standard type face are for T_A = +25°C and those in **boldface type** apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). Unless otherwise specified V_{IN} = 3.6V.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{SHDN}	Shutdown Current	2.7V ≤ V_{IN} ≤ 5.5V, HWEN = GND			1	**3.0**	µA
I_{LED_MIN}	Minimum LED Current	Full-Scale Current = 20.2 mA Exponential Mapping			6.0		µA
T_{SD}	Thermal Shutdown				140		°C
	Hysteresis				15		
Boost Converter							
$I_{HVLED(1/2/3)}$	Output Current Regulation (HVLED1, HVLED2, HVLED3)	2.7V ≤ V_{IN} ≤ 5.5V, Full-Scale Current = 20.2 mA, Brightness Code = 0xFF		**18.38**	20.2	**22.02**	mA
I_{MATCH_HV}	HVLED1 to HVLED2 or HVLED3 Matching (3)	2.7V ≤ V_{IN} ≤ 5.5V	Control Bank A, Exponential Mapping, Autoheadroom Off, PWM Off, I_{LED} = 20.2 mA	**−2.5**		**2.5**	%
			Control Bank A, Exponential Mapping, Autoheadroom Off, PWM Off, I_{LED} = 500 µA	**-8.5**		**8.5**	%
V_{REG_CS}	Regulated Current Sink Headroom Voltage	Auto-headroom off			400		mV
V_{HR_HV}	Minimum Current Sink Headroom Voltage for HVLED Current Sinks	I_{LED} = 95% of nominal, Full-Scale Current = 20.2 mA			190	**275**	mV
R_{DSON}	NMOS Switch On Resistance	I_{SW} = 500 mA			0.3		Ω
I_{CL_BOOST}	NMOS Switch Current Limit	V_{IN} = 3.6V		**880**	1000	**1120**	mA
V_{OVP}	Output Over-Voltage Protection	ON Threshold, 2.7V ≤ V_{IN} ≤ 5.5V OVP select bits = 11		**38.75**	40	**41.1**	V
		Hysteresis			1		
f_{SW}	Switching Frequency	2.7V ≤ V_{IN} ≤ 5.5V	Boost Frequency Select Bit = 0	**450**	500	**550**	kHz
			Boost Frequency Select Bit = 1	**900**	1000	**1100**	
D_{MAX}	Maximum Duty Cycle				94		%
HWEN Input							
V_{HWEN}	Logic Thresholds	Logic Low		**0**		**0.4**	V
		Logic High		**1.2**		**V_{IN}**	
PWM Input							
V_{PWM_L}	Input Logic Low	2.7V ≤ V_{IN} ≤ 5.5V		**0**		**400**	mV
V_{PWM_H}	Input Logic High	2.7V ≤ V_{IN} ≤ 5.5V		**1.31**		**V_{IN}**	V
t_{PWM}	Minimum PWM input pulse	2.7V ≤ V_{IN} ≤ 5.5V	PWM Zero Detect enabled			**0.75**	µs
I^2C-Compatible Voltage Specifications (SCL, SDA)							
V_{IL}	Input Logic Low	2.7V ≤ V_{IN} ≤ 5.5V		**0**		**400**	mV
V_{IH}	Input Logic High	2.7V ≤ V_{IN} ≤ 5.5V		**1.29**		**V_{IN}**	V
V_{OL}	Output Logic Low (SDA)	I_{LOAD} = 3 mA				**400**	mV
I^2C-Compatible Timing Specifications (SCL, SDA) (4), (see Figure 2)							
t_1	SCL (Clock Period)			**2.5**			µs
t_2	Data In Setup Time to SCL High			**100**			ns
t_3	Data Out Stable After SCL Low			**0**			ns

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(1) All voltages are with respect to the potential at the GND pin.

(2) Min and Max limits are verified by design, test, or statistical analysis. Typical (Typ) numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = 3.6V and T_A = +25°C.

(3) LED current sink matching in the high-voltage current sinks (HVLED1 through HVLED3) is given as the maximum matching value between any two current sinks, where the matching between any two high voltage current sinks (X and Y) is given as (IHVLEDX (or I_{HVLEDY}) - $I_{AVE(X-Y)}$)/($I_{AVE(X-Y)}$) x 100. In this test all three HVLED current sinks are assigned to Bank A.

(4) SCL and SDA must be glitch-free in order for proper brightness control to be realized.

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ELECTRICAL CHARACTERISTICS (1) (2) (continued)

Limits in standard type face are for T_A = +25°C and those in **boldface type** apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). Unless otherwise specified V_{IN} = 3.6V.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_4	SDA Low Setup Time to SCL Low (Start)			**100**			ns
t_5	SDA High Hold Time After SCL High (Stop)			**100**			ns
Internal POR Threshold and HWEN Timing Specification							
V_{POR}	POR Reset Release Voltage Threshold	V_{IN} = 3.6V	VIN ramp time = 100 µs	**1.7**	1.9	**2.1**	V
t_{HWEN}	First I^2C Start Pulse after HWEN High	2.7V ≤ V_{IN} ≤ 5.5V	POR Reset complete		5	**20**	µs

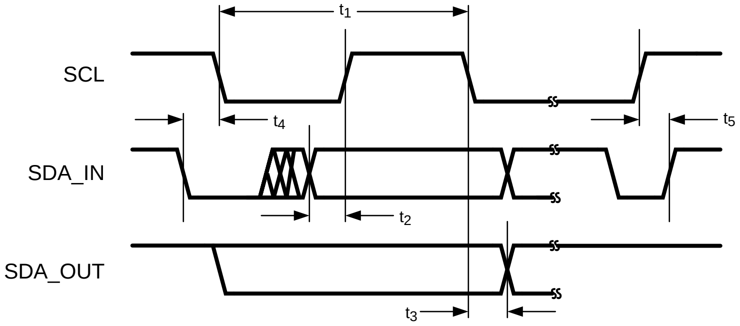

Figure 2. I^2C-Compatible Interface Timing

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

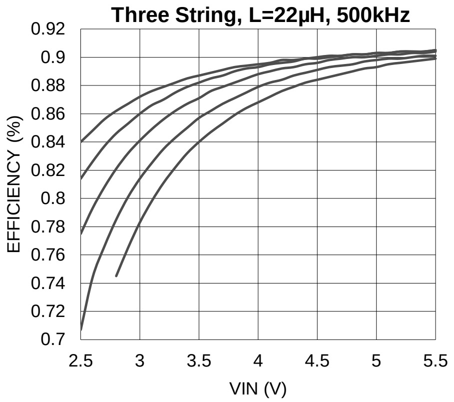

Figure 3. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

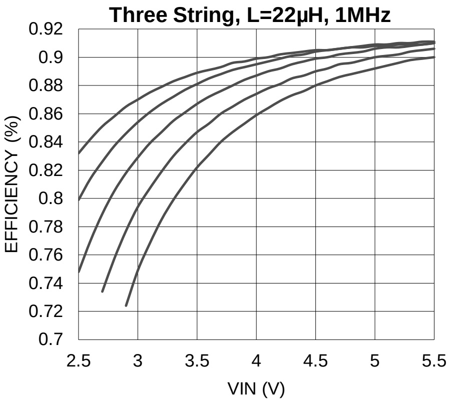

Figure 4. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom:2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

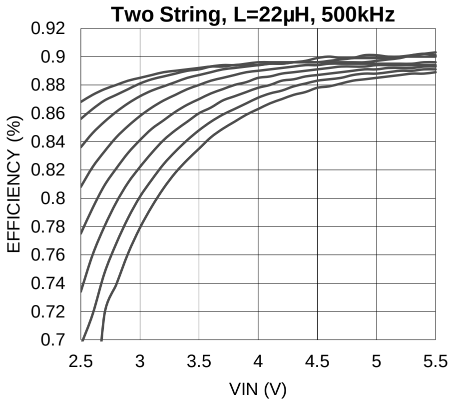

Figure 5. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom:2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

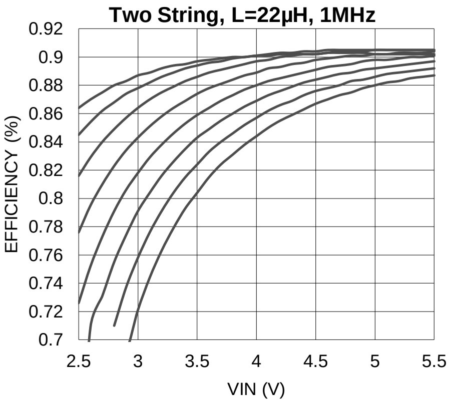

Figure 6. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom:1x3, 1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

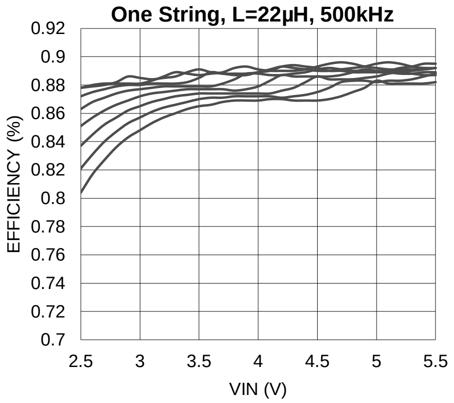

Figure 7. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom:1x3, 1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

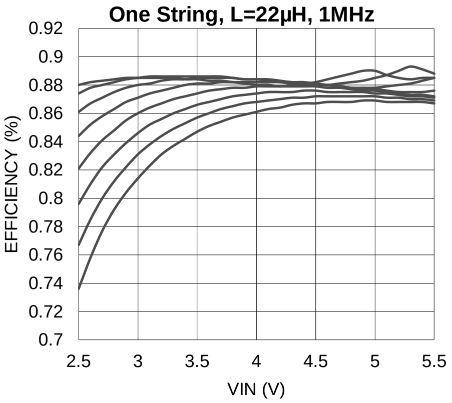

Figure 8. LED Efficiency vs VIN, 20.2 mA/String

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

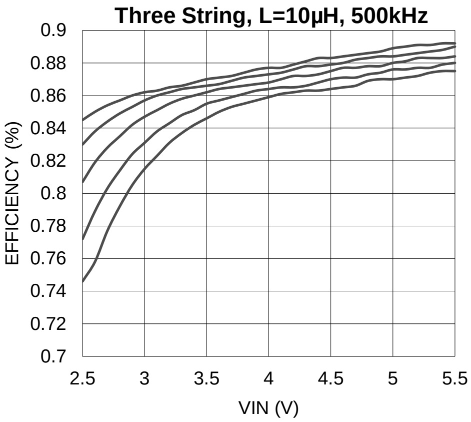

Figure 9. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

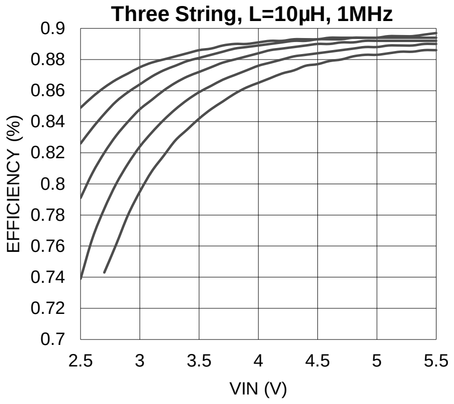

Figure 10. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom:2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

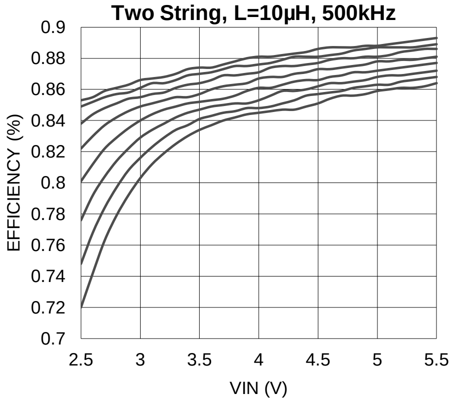

Figure 11. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom:2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

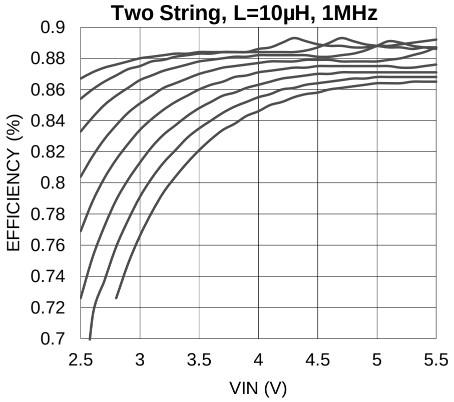

Figure 12. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom:1x3, 1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

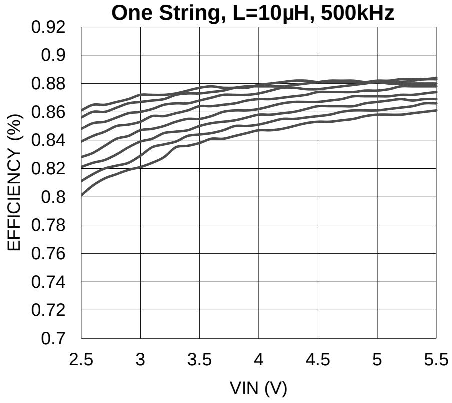

Figure 13. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom:1x3, 1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

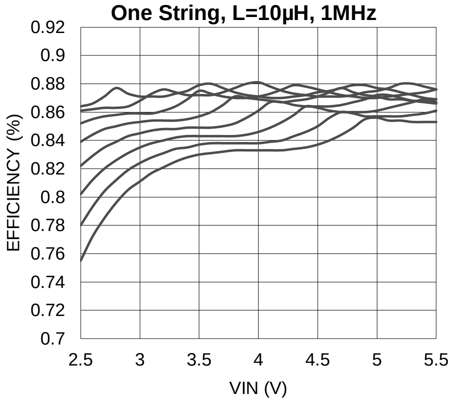

Figure 14. LED Efficiency vs VIN, 20.2 mA/String

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

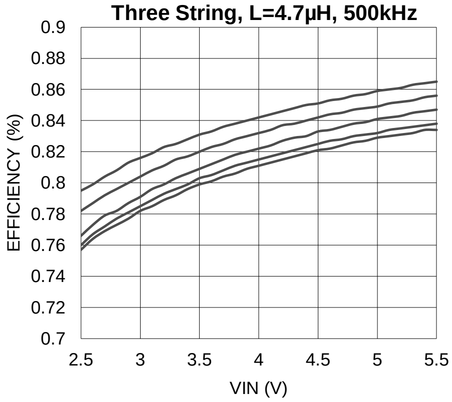

Figure 15. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom:3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

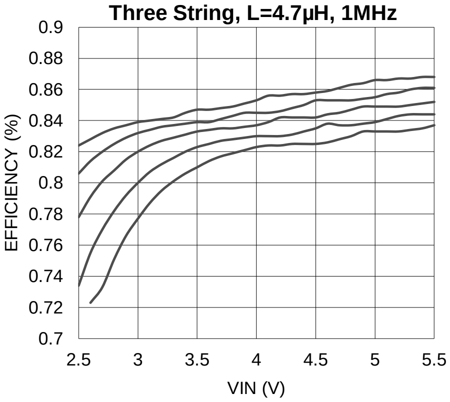

Figure 16. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom:2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

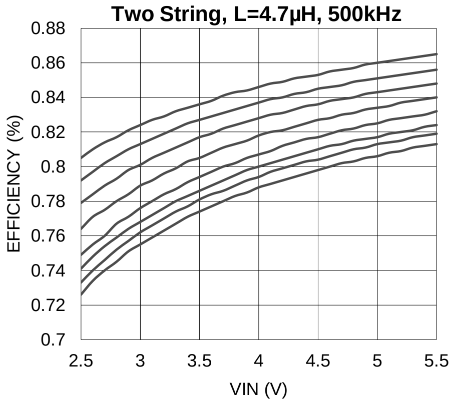

Figure 17. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom:2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

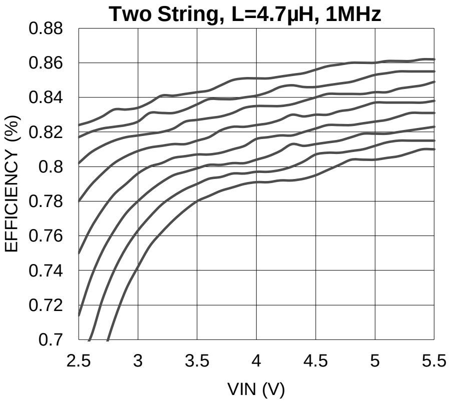

Figure 18. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom:1x3, 1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

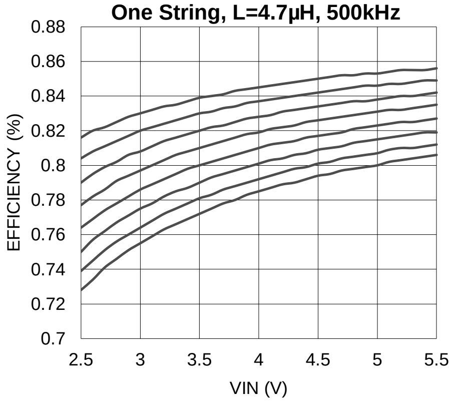

Figure 19. LED Efficiency vs VIN, 20.2 mA/String

Top to Bottom:1x3, 1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

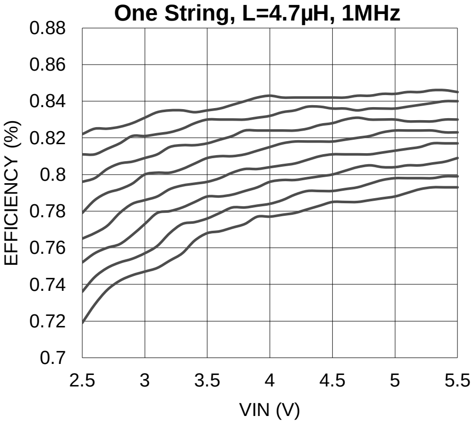

Figure 20. LED Efficiency vs VIN, 20.2 mA/String

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

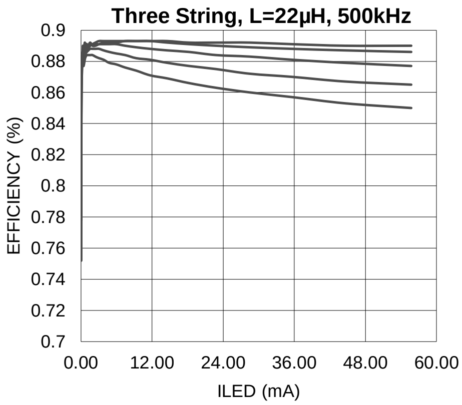
Top to Bottom:3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 21. LED Efficiency vs ILED, VIN=3.6V

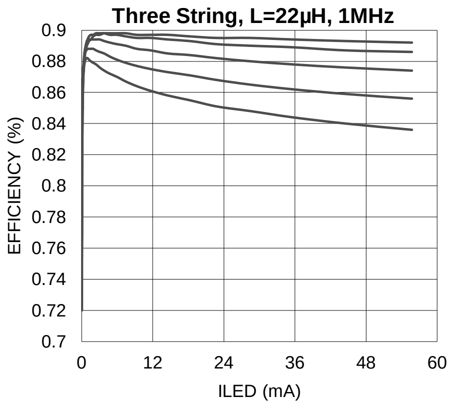
Top to Bottom:3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 22. LED Efficiency vs ILED, VIN=3.6V

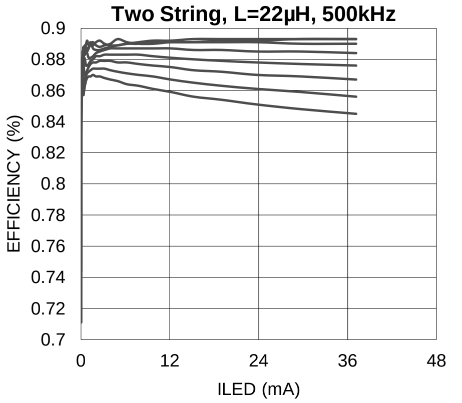
Top to Bottom:2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

Figure 23. LED Efficiency vs ILED, VIN=3.6V

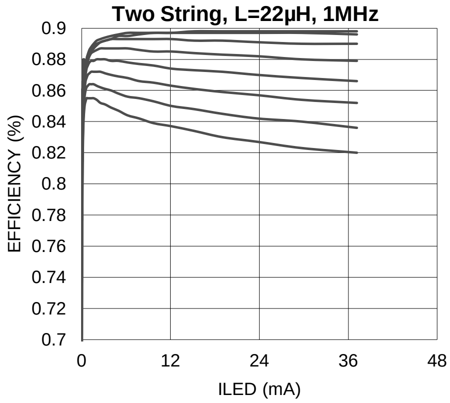
Top to Bottom:2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

Figure 24. LED Efficiency vs ILED, VIN=3.6V

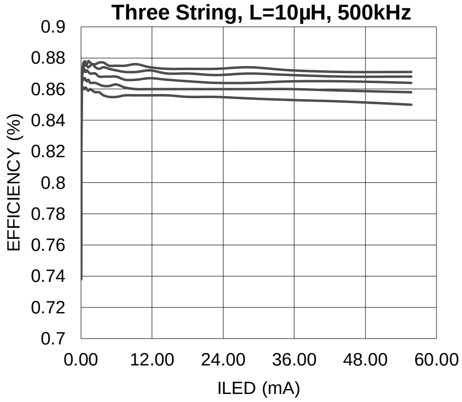
Top to Bottom:3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 25. LED Efficiency vs ILED, VIN=3.6V

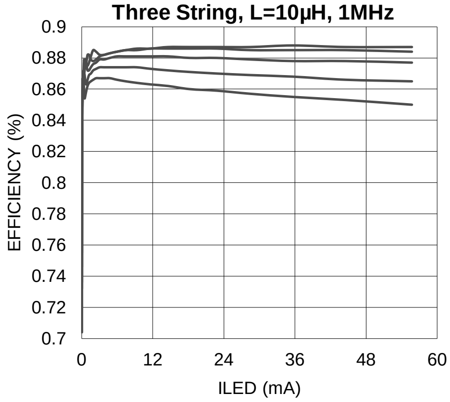
Top to Bottom:3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 26. LED Efficiency vs ILED, VIN=3.6V

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

Top to Bottom:2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

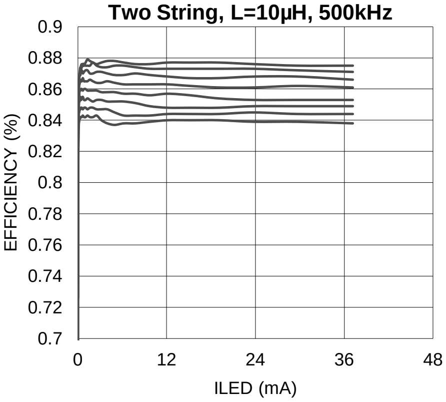

Figure 27. LED Efficiency vs ILED, VIN=3.6V

Top to Bottom:2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

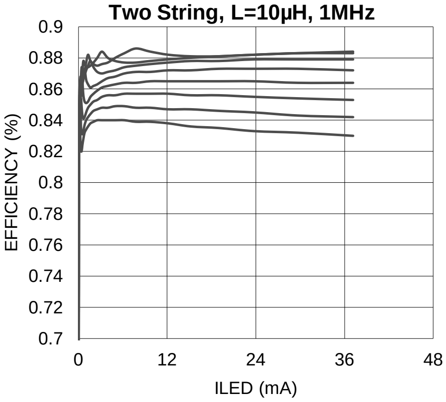

Figure 28. LED Efficiency vs ILED, VIN=3.6V

Top to Bottom:3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

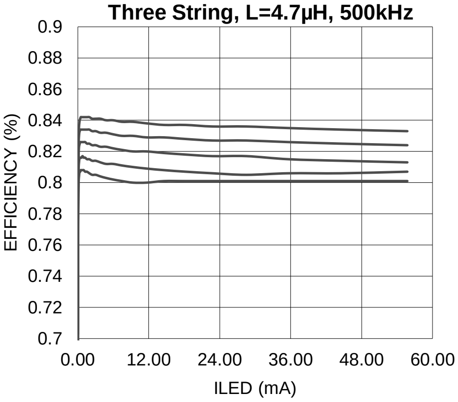

Figure 29. LED Efficiency vs ILED, VIN=3.6V

Top to Bottom:3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

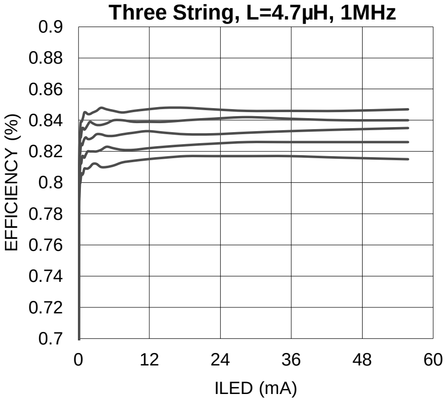

Figure 30. LED Efficiency vs ILED, VIN=3.6V

Top to Bottom:2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

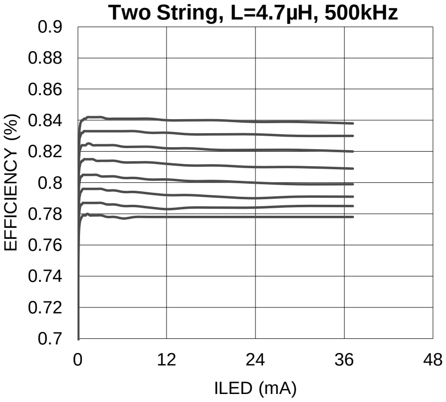

Figure 31. LED Efficiency vs ILED, VIN=3.6V

Top to Bottom:2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

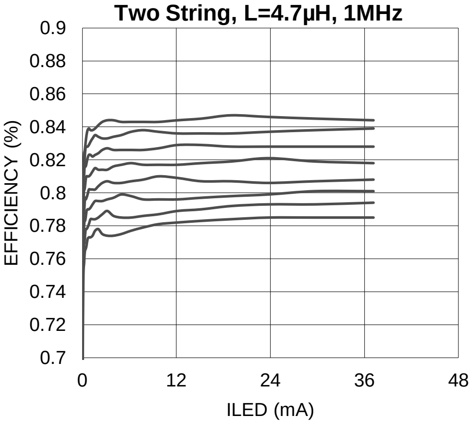

Figure 32. LED Efficiency vs ILED, VIN=3.6V

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

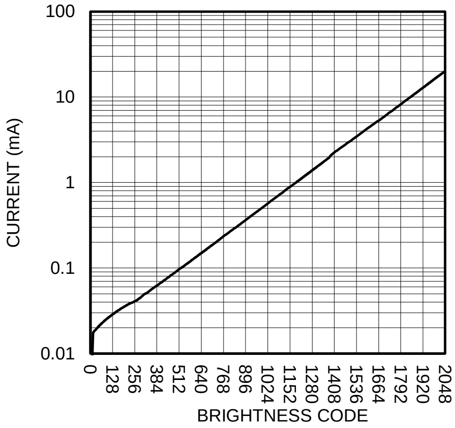

Figure 33. HVLED Current vs. Brightness Code (VIN=3.6V, Exponential Mapping)

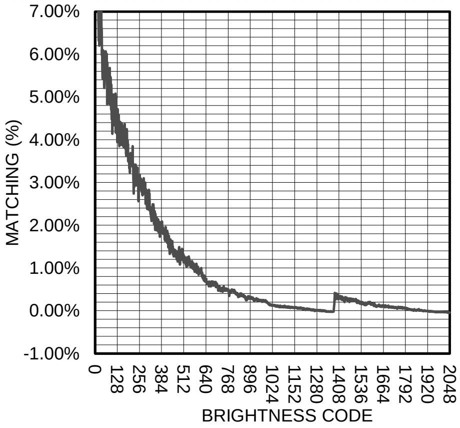

Figure 34. HVLED Matching vs. Code (VIN=3.6V, Exponential Mapping)

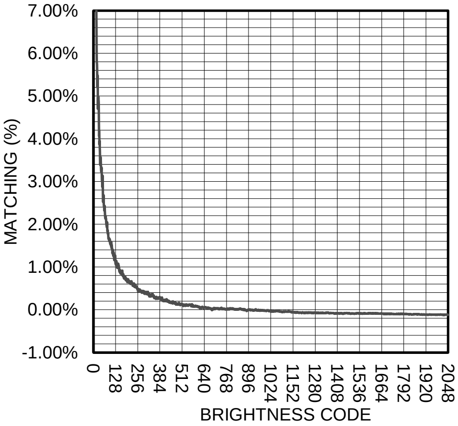

Figure 35. HVLED Matching vs. Code (VIN=3.6V, Linear Mapping)

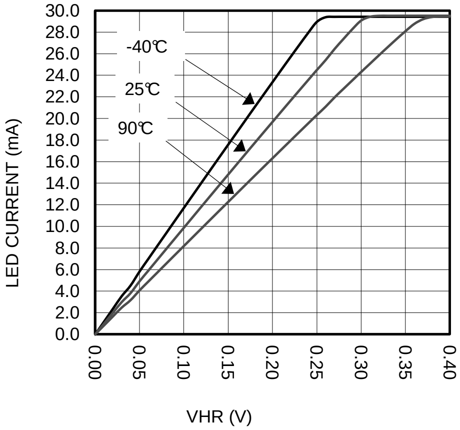

Figure 36. HVLED Current vs. Current Sink Headroom Voltage

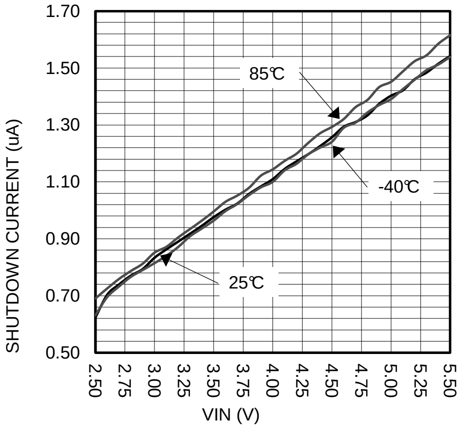

Figure 37. Shutdown Current vs. VIN and Temperature

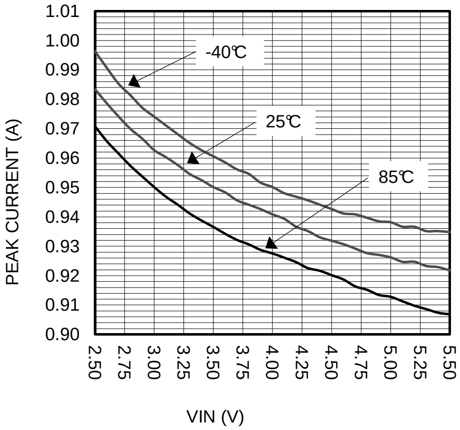

Figure 38. Open Loop Current Limit vs. VIN and Temperature

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

(50% Duty Cycle, ILED FULL_SCALE = 20.2mA)

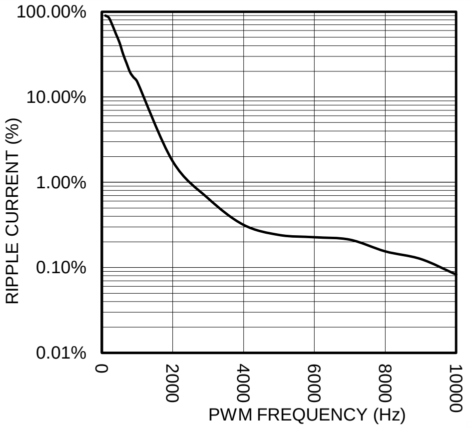
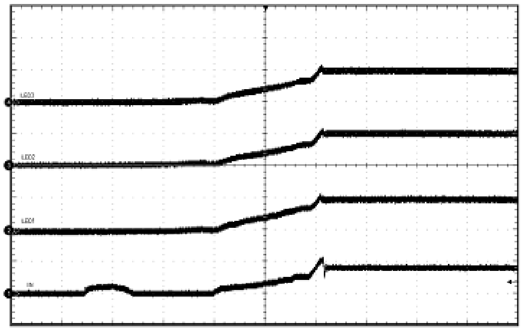


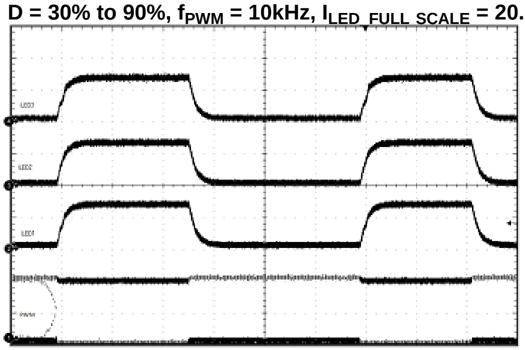
Figure 39. LED Current Ripple vs f_{PWM}



Ch1: 500 mA/div; Ch2-4: 20 mA/div; 500 usec/div

Figure 40. Startup Response (VIN = 3.6V,2x8 LEDs,20mA/string)

D = 30% to 90%, f_{PWM} = 10kHz, $I_{LED\_FULL\ SCALE}$ = 20.2mA



Ch1 = 2V/div; Ch2-4 = 10 mA/div; 2 msec/div

Figure 41. Response to Step Change in PWM Input Duty Cycle

(f_{PWM} = 34kHz, $I_{LED\_FULL\ SCALE}$ = 20.2mA)

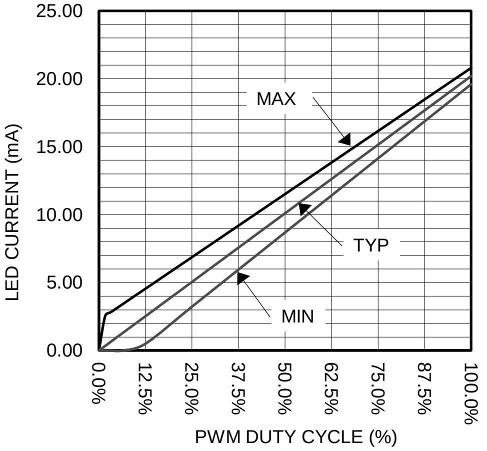
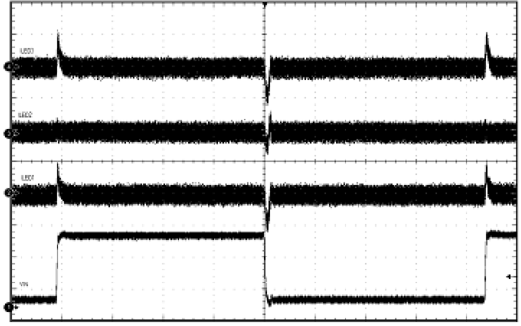


Figure 42. HVLED Current vs PWM Input Duty Cycle

Typical Application Circuit, 3x6 LEDs, 20.2mA/string



Ch1: 300mV/div; Ch2-4: 2 mA/div; 1 msec/div

Figure 43. Line Step Response

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FUNCTIONAL DESCRIPTION

The LM3697 provides the power for three high-voltage LED strings. The three high-voltage LED strings are powered from an integrated boost converter. The device is configured over an I^2C-compatible interface. The LM3697 provides a Pulse Width Modulation (PWM) input for content adjustable brightness control.

PWM Input

The PWM input can be assigned to either of the high-voltage control banks. When assigned to a control bank, the programmed current in the control bank becomes a function of the duty cycle (D_{PWM}) at the PWM input and the control bank brightness setting. When PWM is disabled D_{PWM} is equal to one.

HWEN Input

HWEN is the global hardware enable to the LM3697. HWEN must be pulled high to enable the device. HWEN is a high-impedance input so it cannot be left floating. When HWEN is pulled low the LM3697 is placed in shutdown, and all the registers are reset to their default state.

Thermal Shutdown

The LM3697 contains a thermal shutdown protection. In the event the die temperature reaches +140°C, the boost, charge pump, and current sinks will shut down until the die temperature drops to typically +125°C.

Functional Block Diagram

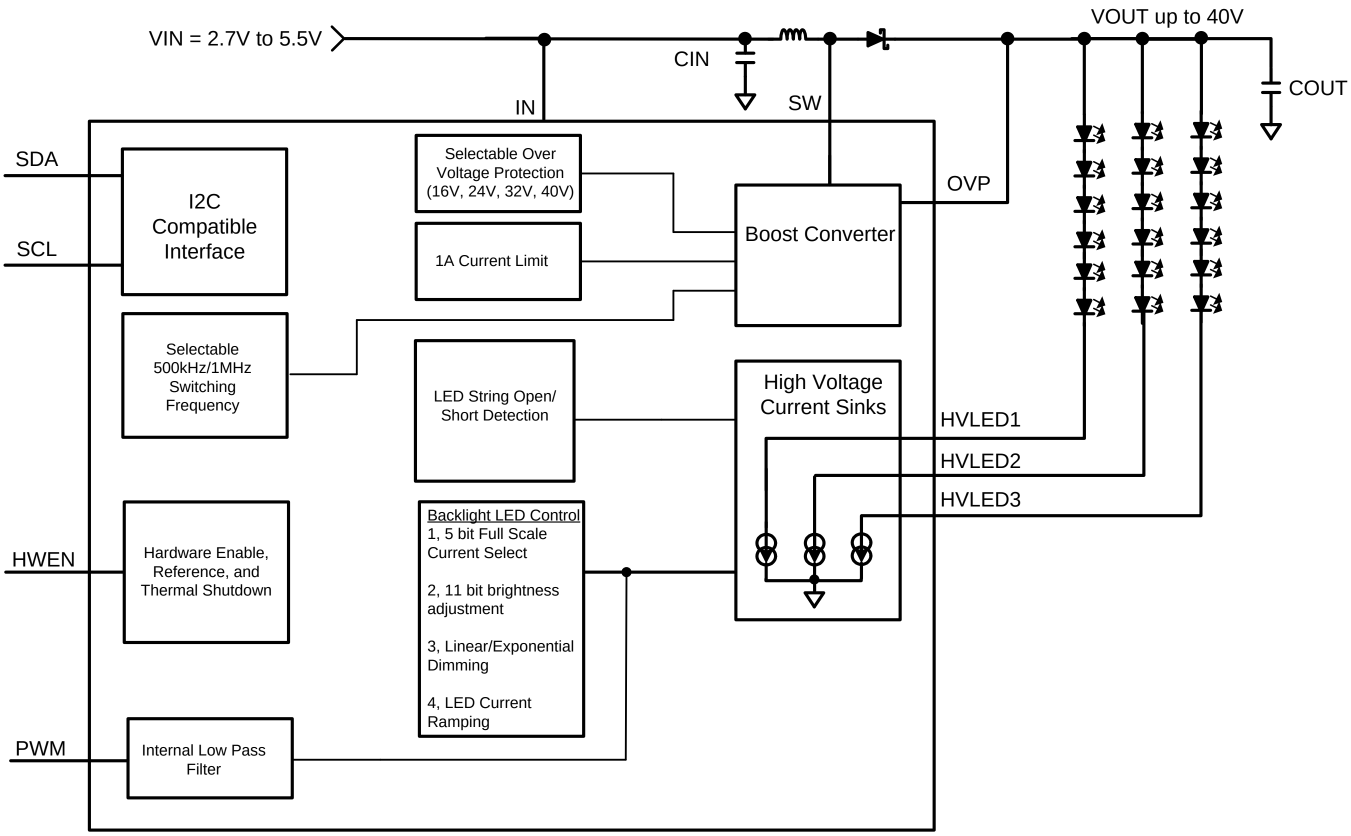

Figure 44. Functional Block Diagram

High-Voltage LED Control

High-Voltage Boost Converter

The high-voltage boost converter provides power for the three high-voltage current sinks (HVLED1, HVLED2 and HVLED3). The boost circuit operates using a 4.7 µH to 22 µH inductor and a 1 µF output capacitor. The selectable 500 kHz or 1 MHz switching frequency allows for use of small external components and provides for high boost-converter efficiency. HVLED1, HVLED2 and HVLED3 feature an adaptive current regulation scheme where the feedback point (HVLED1, HVLED2 and HVLED3) regulates the LED headroom voltage V_{HR_HV}. When there are different voltage requirements in the high-voltage LED strings (string mismatch), the LM3697 will regulate the feedback point of the highest voltage string to V_{HR_HV} and drop the excess voltage of the lower voltage string across the lower strings current sink.

High-Voltage Current Sinks (HVLED1, HVLED2 and HVLED3)

HVLED1, HVLED2 and HVLED3 control the current in the high-voltage LED strings as configured by Control Bank A or B. Each Control Bank has 5-bit full-scale current programmability and 11-bit brightness control. Assignment of the high-voltage current sinks to control bank is done through the HVLED Current Sink Output Configuration register (see Table 5).

High-Voltage Current String Biasing

Each high-voltage current string can be powered from the LM3697's boost output (COUT) or from an external source. The feedback enable bits (HVLED Current Sink Feedback Enables register bits [2:0]) determine where the high-voltage current string anodes will be connected. When set to '1' (default) the high-voltage current sink inputs are included in the boost feedback loop. This allows the boost converter to adjust its output voltage in order to maintain the LED headroom voltage V_{HR_HV} at the current sink input.

When powered from alternate sources the feedback enable bits should be set to '0'. This removes the particular current sink from the boost feedback loop. In these configurations the application must ensure that the headroom voltage across the high-voltage current sink is high enough to prevent the current sink from going into dropout (see the TYPICAL PERFORMANCE CHARACTERISTICS for data on the high-voltage LED current vs V_{HR_HV}).

Setting the HVLED Current Sink Feedback Enables register bits also determines triggering of the shorted high-voltage LED String Fault flag (see Fault Flags/Protection Features section).

Boost Switching-Frequency Select

The LM3697's boost converter has two switching frequency settings. The switching frequency setting is controlled via the Boost Frequency Select bit (bit 0 in the Boost Control register). Operating at the 500 kHz switching frequency results in better efficiency under lighter load conditions due to the decreased switching losses. In this mode the inductor must be between 10 µH and 22 µH. Operating at the 1MHz switching frequency results in better efficiency under higher load conditions resulting in lower conduction losses in the MOSFETs and inductor. In this mode the inductor can be between 4.7 µH and 22 µH.

Automatic Switching Frequency Shift

The LM3697 has an automatic frequency select mode (bit 3 in the Boost Control register) to optimize the frequency vs load dependent losses. In Auto-Frequency mode the boost converter switching frequency is changed based on the high-voltage LED current. The threshold (Control A/B brightness code) at which the frequency switch-over occurs is configurable via the Auto-Frequency Threshold register. The Auto-Frequency Threshold register contains an 8-bit code which is compared to the 8 MSB's of the brightness code. When the brightness code is greater than the Auto-Frequency Threshold value the boost converter switching frequency will be 1 MHz. When the brightness code is less than or equal to the Auto-Frequency Threshold register the boost converter switching frequency will be 500 kHz.

Figure 45 illustrates the LED efficiency improvement (3p5s LED configuration with 4.7 µH inductor) when the Auto-Frequency feature is enabled. When the LED brightness is less than or equal to 0x6C, the switching frequency is 500 Khz, and it improves the LED efficiency by up to 6%. When the LED brightness is greater than 0x6C, the switching frequency is 1Mhz, and it improves LED efficiency by up to 2.2%.

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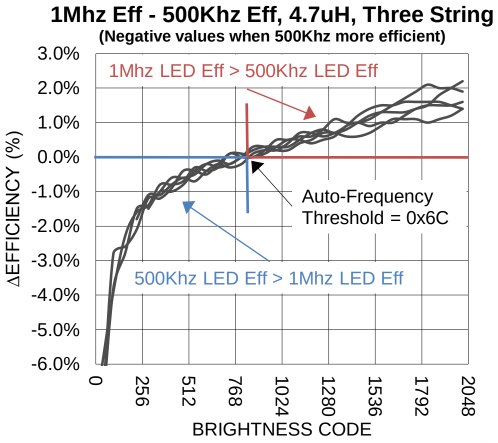

Figure 45. Auto-Frequency LED Efficiency Improvement Illustration

Table 1 summarizes the general recommendations for Auto-Frequency Threshold setting vs Inductance values and LED string configurations. These are general recommendations — the optimum Auto-Frequency Threshold setting should be evaluated for each application.

Table 1. Auto-Frequency Threshold Settings

	Three String			Two String		
Inductor	Auto-Frequency	Peak Efficiency Improvement	Peak Configuration	Auto-Frequency	Peak Efficiency Improvement	Peak Configuration
	Threshold			Threshold		
4.7 µH	6C	2.20%	3p5s	AC	1.10%	2p6s
10 µH	74	1.70%	3p4s	B4	1.30%	2p5s
22 µH	7C	0.70%	3p3s	BC	0.70%	2p4s

Brightness Register Current Control

The LM3697 features Brightness Register Current Control for simple user-adjustable current control set by writing directly to the appropriate Control Bank Brightness Registers. The current for Control Banks A & B is a function of the full-scale LED current, the 11-bit code in the respective brightness register, and the PWM input duty cycle (if PWM is enabled). The Control A/B brightness should always be written with LSB's first and MSB's last. The preferred operating mode is to control the high-voltage LED brightness by setting the 3 LSB's to zero and using only the upper 8 MSB's. In this mode the LM3697 will use the full 11-bit brightness code while ramping the high-voltage LED brightness.

PWM Control

The LM3697's PWM input can be enabled for Control Banks A or B (see Table 14). Once enabled, the LED current becomes a function of the code in the Control Bank Brightness Configuration Register and the PWM input-duty cycle.

The PWM input accepts a logic level voltage and internally filters it to an analog control voltage. This results in a linear response of duty cycle to current, where 100% duty cycle corresponds to the programmed brightness code multiplied by the Full-Scale Current setting.

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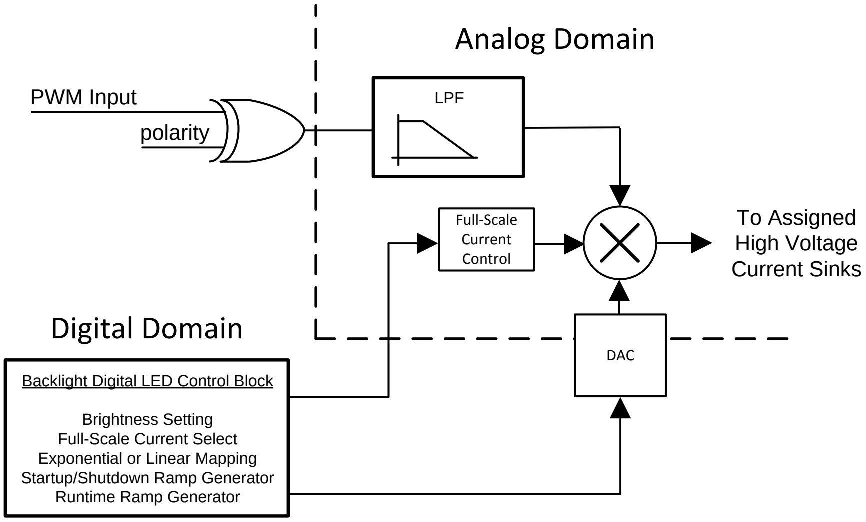

Figure 46. PWM Input Architecture

PWM Input Frequency Range

The usable input frequency range for the PWM input is governed on the low end by the cutoff frequency of the internal low-pass filter (540 Hz, Q = 0.33) and on the high end by the propagation delays through the internal logic. For frequencies below 2 kHz the current ripple begins to become a larger portion of the DC LED current. Additionally, at lower PWM frequencies the boost output voltage ripple increases, causing a non-linear response from the PWM duty cycle to the average LED current due to the response time of the boost. For the best response of current vs. duty cycle, the PWM input frequency should be kept between 2 kHz and 100 kHz.

PWM Input Polarity

The PWM Input can be set for active low polarity, where the LED current is a function of the negative duty cycle. This is set via the PWM Configuration register (see Table 14).

PWM Zero Detection

The LM3697 incorporates a feature to detect when the PWM input is near zero. After the near zero pulse width has been detected the PWM pulse must be greater than t_{PWM} to affect the HVLED output current (see ELECTRICAL CHARACTERISTICS (1) (2)). Bit 3 in the PWM Configuration register is used to disable this feature.

Startup/Shutdown Ramp

The high-voltage LED startup and shutdown ramp times are independently configurable in the Startup/Shutdown Transition Time Register (see Table 6). There are 16 different Startup and 16 different Shutdown times. The startup times can be programmed independently from the shutdown times, but each Control bank is not independently configurable.

The startup ramp time is from when the Control Bank is enabled to when the LED current reaches its initial set point. The shutdown ramp time is from when the Control Bank is disabled to when the LED current reaches 0.

Run-Time Ramp

Current ramping from one brightness level to the next is programmed via the Run-Time Transition Time Register (see Table 7). There are 16 different ramp-up times and 16 different ramp-down times. The ramp-up time can be programmed independently from the ramp-down time, but each Control Bank cannot be independently programmed. For example, programming a ramp-up or ramp-down time is a global setting for all high-voltage LED Control Banks.

---

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are verified by design, test, or statistical analysis. Typical (Typ) numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = 3.6V and T_A = +25°C.

High-Voltage Control A/B Ramp Select

The LM3697 provides three options for Control A/B ramp times. When the Run-time Ramp Select bits are set to 00 the control bank will use both the Startup/Shutdown and Run-time ramp times. When the Run-time Ramp Select bits are set to 01 the control bank will use the Startup/Shutdown ramp times for both startup/shutdown and run-time. When the Run-time Ramp Select bits are set to 1x the control bank will use a zero usec Run-time ramp.

LED Current Mapping Modes

All control banks can be programmed for either exponential or linear mapping modes (see Figure 47). These modes determine the transfer characteristic of backlight code to LED current. Independent mapping of Control Banks A and B is not allowed, both banks will use the same mapping mode.

Exponential Mapping

In Exponential Mapping Mode the brightness code to backlight current transfer function is given by the equation:

$$I_{LED} = I_{LED\_FULLSCALE} \text{ x } 0.85^{\left(44 - \frac{Code + 1}{5.8181818}\right)} \text{ x } D_{PWM} \qquad (1)$$

Where $I_{LED\_FULLSCALE}$ is the full-scale LED current setting (see Table 10) , Code is the 8-bit backlight code in the Control Brightness MSB register and D_{PWM} is the PWM Duty Cycle. In Exponential Mapping Mode the current ramp (either up or down) appears to the human eye as a more uniform transition then the linear ramp. This is due to the logarithmic response of the eye.

Linear Mapping

In Linear Mapping Mode the brightness code to backlight current has a linear relationship and follows the equation:

$$I_{LED} = I_{LED\_FULLSCALE} \text{ x } \frac{1}{255} \text{ x Code x } D_{PWM} \qquad (2)$$

Where $I_{LED\_FULLSCALE}$ is the full-scale LED current setting, Code is the 8-bit backlight code in the Control Brightness MSB register and D_{PWM} is the PWM Duty Cycle.

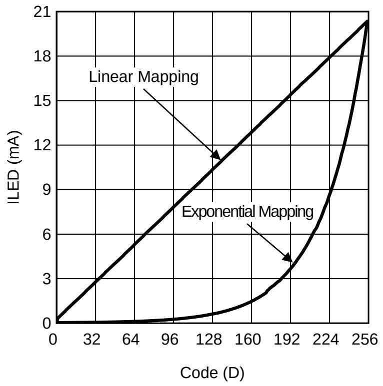

Figure 47. LED Current Mapping Modes

Fault Flags/Protection Features

The LM3697 contains both an LED open and LED short fault detection. These fault detections are designed to be used in production level testing and not normal operation. For the fault flags to operate, they must be enabled via the LED Fault Enable Register (see Table 22). The following sections detail the proper procedure for reading back open and short faults in the high-voltage LED strings.

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Open LED String (HVLED)

An open LED string is detected when the voltage at the input to any active high-voltage current sink has fallen below 200 mV, and the boost output voltage has hit the OVP threshold. This test assumes that the HVLED string that is being detected for an open is connected to the LM3697's boost output (COUT+) (see Table 20). For an HVLED string not connected to the LM3697's boost output voltage, but connected to another voltage source, the boost output will not trigger the OVP flag. In this case an open LED string will not be detected.

The procedure for detecting an open fault in the HVLED current sinks (provided they are connected to the boost output voltage) is:

- Apply power to the LM3697
- Enable Open Fault (Register 0xB4, bit [0] = 1)
- Assign HVLED1, HVLED2 and HVLED3 to Bank A (Register 0x10, Bits [2:0] = (0, 0, 0)
- Set the startup ramp times to the fastest setting (Register 0x11 = 0x00)
- Set Bank A full-scale current to 20.2 mA (Register 0x17 = 0x13)
- Configure HVLED1, HVLED2 and HVLED3 for LED string anode connected to COUT (Register 0x19, bits[2:0] = (1,1,1))
- Set Bank A brightness to max (Register 0x21 = 0xFF)
- Enable Bank A (Register 0x24 Bit[0] = 1
- Wait 4 ms
- Read back bits[2:0] of register 0xB0. Bit [0] = 1 (HVLED1 open). Bit [1] = 1 (HVLED2 open). Bit [2] = 1 (HVLED3 open)
- Disable all banks (Register 0x24 = 0x00)

Shorted LED String (HVLED)

The LM3697 features an LED short fault flag indicating one or more of the HVLED strings have experienced a short. The method for detecting a shorted HVLED strings is if the current sink is enabled and the string voltage (V_{OUT} - $V_{HVLED1/2/3}$) falls to below (V_{IN} - 1V) . This test must be performed on one HVLED string at a time. Performing the test with more than one current sink enabled can result in a faulty reading.

The procedure for detecting a short in an HVLED string is:

- Apply power to the LM3697
- Enable Short Fault (Register 0xB4, bit [1] = 1)
- Assign HVLED1 to Bank A (Register 0x10, Bits [2:0] = (1, 1, 0)
- Set the startup ramp times to the fastest setting (Register 0x11 = 0x00)
- Set Bank A full-scale current to 20.2 mA (Register 0x17 = 0x13)
- Enable Feedback on the HVLED Current Sinks (Register 0x19, bits[2:0] = (1,1,1))
- Set Bank A brightness to max (Register 0x21 = 0xFF)
- Enable Bank A (Register 0x24 Bit[0] = 1)
- Wait 4 ms
- Read back bits[0] of register 0xB2. 1 = HVLED1 short.
- Disable all banks (Register 0x24 = 0x00)
- Repeat the procedure for the HVLED2 and HVLED3 strings

Over-Voltage Protection (Inductive Boost)

The over-voltage protection threshold (OVP) on the LM3697 has 4 different configurable options (16V, 24V, 32V, and 40V). The OVP protects the device and associated circuitry from high voltages in the event the high-voltage LED string becomes open. During normal operation, the LM3697's inductive boost converter will boost the output up so as to maintain V_{HR} at the active, high-voltage (COUT connected) current sink inputs. When a high-voltage LED string becomes open, the feedback mechanism is broken, and the boost converter will over-boost the output. When the output voltage reaches the OVP threshold the boost converter will stop switching, thus allowing the output node to discharge. When the output discharges to V_{OVP} – 1V the boost converter will begin switching again. The OVP sense is at the OVP pin, so this pin must be connected directly to the inductive boost output capacitor's positive terminal.

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For high-voltage current sinks that have the HVLED Current Sink Feedback Enable setting such that the high-voltage current sinks anodes are not connected to COUT (feedback is disabled), the over-voltage sense mechanism is not in place to protect the input to the high-voltage current sink. In this situation the application must ensure that the voltage at HVLED1, HVLED2 or HVLED3 doesn't exceed 40V.

The default setting for OVP is set at 16V. For applications that require higher than 16V at the boost output, the OVP threshold must be programmed to a higher level after powerup.

Current Limit (Inductive Boost)

The NMOS switch current limit for the LM3697's inductive boost is set at 1A. When the current through the LM3697's NFET switch hits this over-current protection threshold (OCP), the device turns the NFET off and the inductor's energy is discharged into the output capacitor. Switching is then resumed at the next cycle. The current limit protection circuitry can operate continuously each switching cycle. The result is that during high-output power conditions the device can continuously run in current limit. Under these conditions the LM3697's inductive boost converter stops regulating the headroom voltage across the high-voltage current sinks. This results in a drop in the LED current.

I^{2}C-Compatible Interface

Start And Stop Conditions

The LM3697 is controlled via an I^{2}C-compatible interface. START and STOP conditions classify the beginning and the end of the I^{2}C session. A START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I^{2}C master always generates START and STOP conditions. The I^{2}C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I^{2}C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW.

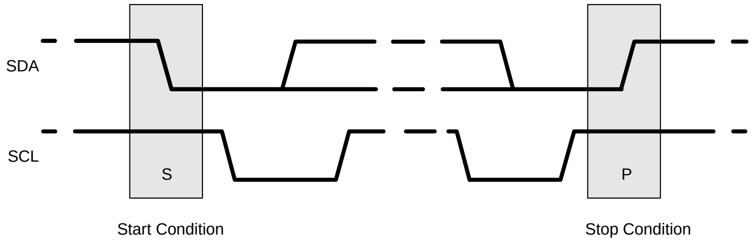

Figure 48. Start and Stop Sequences

I^{2}C-Compatible Address

The chip address for the LM3697 is 0110110 (36h). After the START condition, the I^{2}C master sends the 7-bit chip address followed by an eighth read or write bit (R/W). R/W= 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the chip address selects the register address to which the data will be written. The third byte contains the data for the selected register.

Transferring Data

Every byte on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse (9th clock pulse) is generated by the master. The master releases SDA (HIGH) during the 9th clock pulse. The LM3697 pulls down SDA during the 9th clock pulse signifying an acknowledge. An acknowledge is generated after each byte has been received.

Table 2 lists the available registers within the LM3697.

LM3697 Register Descriptions

Table 2. LM3697 Register Descriptions

Name	Address	Power On Reset	Operation
Revision	0x00	0x00	Dynamic
Software Reset	0x01	0x00	Dynamic
HVLED Current Sink Output Configuration	0x10	0x06	Static
Control A Startup/Shutdown Ramp Time	0x11	0x00	Static
Control B Startup/Shutdown Ramp Time	0x12	0x00	Static
Control A/B Runtime Ramp Time	0x13	0x00	Static
Control A/B Runtime Ramp Configuration	0x14	0x00	Static
Reserved	0x15	0x33	Static
Brightness Configuration	0x16	0x00	Static
Control A Full Scale Current Setting	0x17	0x13	Static
Control B Full Scale Current Setting	0x18	0x13	Static
HVLED Current Sink Feedback Enables	0x19	0x07	Static
Boost Control	0x1A	0x00	Static
Auto-Frequency Threshold	0x1B	0xCF	Static
PWM Configuration	0x1C	0x0C	Dynamic(1)
Control A Brightness LSB	0x20	0x00	Dynamic
Control A Brightness MSB	0x21	0x00	Dynamic
Control B Brightness LSB	0x22	0x00	Dynamic
Control B Brightness MSB	0x23	0x00	Dynamic
Control Bank Enables	0x24	0x00	Dynamic
HVLED Open Faults	0xB0	0x00	Production Test Only
HVLED Short Faults	0xB2	0x00	Production Test Only
LED Fault Enables	0xB4	0x00	Production Test Only

(1) The PWM input should always be in the inactive state when setting the Control bank PWM Enable bit. The PWM configuration bits should only be changed when the PWM is disabled for both Control Banks.

Table 3. Revision (Address 0x00)

Bits [7:4] Not Used	Bits [3:0] Silicon Revision
Reserved	0000 = Rev. A Silicon

Table 4. Software Reset (Address 0x01)

Bits [7:1] Not Used	Bit [0] Silicon Revision
Reserved	0 = Normal Operation 1 = Software Reset (self-clearing)

Table 5. HVLED Current Sink Output Configuration (Address 0x10)

Bits [7:3] Not Used	Bit [2] HVLED3 Configuration	Bit [1] HVLED2 Configuration	Bit [0] HVLED1 Configuration
Reserved	0 = Control A 1 = Control B (default)	0 = Control A 1 = Control B (default)	0 = Control A (default) 1 = Control B

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Table 6. Control A & B Startup/Shutdown Ramp Time (Address 0x11 and 0x12)

Bits [7:4] Startup Ramp	Bits [3:0] Shutdown Ramp
0000 = 2048µs (default) 0001 = 262ms 0010 = 524ms 0011 = 1.049s 0100 = 2.09s 0101 = 4.194 s 0110 = 8.389s 0111 = 16.78s 1000 = 33.55s 1001 = 41.94s 1010 = 50.33s 1011 = 58.72s 1100 = 67.11s 1101 = 83.88s 1110 = 100.66s 1111 = 117.44s	0000 = 2048µs (default) 0001 = 262ms 0010 = 524ms 0011 = 1.049s 0100 = 2.097s 0101 = 4.194s 0110 = 8.389s 0111 = 16.78s 1000 = 33.55s 1001 = 41.94s 1010 = 50.33s 1011 = 58.72s 1100 = 67.11s 1101 = 83.88s 1110 = 100.66s 1111 = 117.44s

Table 7. Control A & B Run-Time Ramp Time (Address 0x13)

Bits [7:4] Transition Time Ramp Up	Bits [3:0] Transition Time Ramp Down
000 = 2048µs (default) 001 = 262ms 010 = 524ms 011 = 1.049s 100 = 2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s 1000 = 33.55s 1001 = 41.94s 1010 = 50.33s 1011 = 58.72s 1100 = 67.11s 1101 = 83.88s 1110 = 100.66s 1111 = 117.44s	000 = 2048µs (default) 001 = 262ms 010 = 524ms 011 = 1.049s 100 = 2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s 1000 = 33.55s 1001 = 41.94s 1010 = 50.33s 1011 = 58.72s 1100 = 67.11s 1101 = 83.88s 1110 = 100.66s 1111 = 117.44s

Table 8. Control A & B Run-Time Ramp Configuration (Address 0x14)

Bits [7:4] Not Used	Bits [3:2] Control B Run-time Ramp Select	Bits [1:0] Control A Run-time Ramp Select
Reserved	00 = Control A/B Runtime Ramp Times (default) 01 = Control B Startup/Shutdown Ramp Times 1x = 0 us Ramp Time	00 = Control A/B Runtime Ramp Times (default) 01 = Control A Startup/Shutdown Ramp Times 1x = 0 us Ramp Time

Table 9. Control A/B Brightness Configuration (Address 0x16)

Bits [7:4] Not Used	Bit [3] Control B Dither Disable	Bit [2] Control A Dither Disable	Bit [1] Not Used	Bit [0] Control A/B Mapping Mode
Reserved	0 Enable (default) 1 Disable	0 Enable (default) 1 Disable	Reserved	0 Exponential (default) 1 Linear

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Table 10. Control A-B Full-Scale Current Setting (Address 0x17 and 0x18)

Bits [7:5] Not Used	Bits [4:0] Control A, B Full-Scale Current Select Bits
Reserved	00000 = 5mA
	10011 = 20.2mA (default)
	11111 = 29.8mA (0.8mA steps, FS = 5 + code * 0.8mA)

Table 11. HVLED Current Sink Feedback Enables (Address 0x19)

Bits [7:3] Not Used	Bit [2] HVLED3 Feedback Enable	Bit [1] HVLED2 Feedback Enable	Bit [0] HVLED1 Feedback Enable
Reserved	0 = LED anode is NOT CONNECTED to COUT 1 = LED anode is CONNECTED to COUT (default)	0 = LED anode is NOT CONNECTED to COUT 1 = LED anode is CONNECTED to COUT (default)	0 = LED anode is NOT CONNECTED to COUT 1 = LED anode is CONNECTED to COUT (default)

Table 12. Boost Control (Address 0x1A)

Bits [7:5] Not Used	Bit [4] Auto-Headroom Enable	Bit [3] Auto-Frequency Enable	Bits [2:1] Boost OVP Select	Bit [0] Boost Frequency Select
Reserved	0 = Disable (default) 1 = Enable	0 = Disable (default) 1 = Enable	00 = 16V (default) 01 = 24V 10 = 32V 11 = 40V	0 = 500 kHz (default) 1 = 1MHz

Table 13. Auto-Frequency Threshold (Address 0x1B)

Bits [7:0]
Auto-Frequency Threshold (default = 11001111)

Table 14. PWM Configuration (Address 0x1C)

Bits [7:4] Not Used	Bit [3] PWM Zero Detection Enable	Bit [2] PWM Polarity	Bit [1] Control B PWM Enable	Bit [0] Control A PWM Enable
Reserved	0 = Disable 1 = Enable (default)	0 = Active Low 1 = Active High (default)	0 = Disable (default) 1 = Enable	0 = Disable (default) 1 = Enable

Table 15. Control A Brightness LSB (Address 0x20)

Bits [7:3] Not Used	Bits [2:0] Control A Brightness [2:0]
Reserved	Brightness LSB

Table 16. Control A Brightness MSB (Address 0x21)

Bits [7:0] Control A Brightness [11:3]
Brightness MSB (Ramping starts when MSB is written)
When the Mapping Mode is set for exponential mapping (Control Bank_Brightness Configuration Register Bit [2] = 0), the current approximates the equation: $I_{LED} = I_{LED\_FULLSCALE} \times 0.85^{\left(44 - \frac{Code + 1}{5.8181818}\right)} \times D_{PWM}$ (3)
When the Mapping Mode is set for linear mapping (Control Bank_Brightness Configuration Register Bit [2] = 1), the current approximates the equation: $I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code$ (4)

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Table 17. Control B Brightness LSB (Address 0x22)

Bits [7:3] **Not Used**	**Bits [2:0]** **Control B Brightness [2:0]**
Reserved	Brightness LSB

Table 18. Control B Brightness MSB (Address 0x23)

Bits [7:0] **Control B Brightness [11:3]**
Brightness MSB (Ramping starts when MSB is written)
When the Mapping Mode is set for exponential mapping (Control Bank_Brightness Configuration Register Bit [2] = 0), the current approximates the equation: $I_{LED} = I_{LED\_FULLSCALE} \times 0.85^{\left(44 - \frac{Code + 1}{5.8181818}\right)} \times D_{PWM}$ (5)
When the Mapping Mode is set for linear mapping (Control Bank_Brightness Configuration Register Bit [2] = 1), the current approximates the equation: $I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code$ (6)

Table 19. Control Bank Enables (Address 0x24)

Bit [7:2] **Not Used**	**Bit [1]** **Control B Enable**	**Bit [0]** **Control A Enable**
Reserved	0 = Disable (default) 1 = Enable	0 = Disable (default) 1 = Enable

Table 20. HVLED Open Faults (Address 0xB0)

Bits [7:3] **Not Used**	**Bit [2]** **HVLED3 Open**	**Bit [1]** **HVLED2 Open**	**Bit [0]** **HVLED1 Open**
Reserved	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open

Table 21. HVLED Short Faults (Address 0xB2)

Bits [7:3] **Not Used**	**Bit [2]** **HVLED3 Short**	**Bit [1]** **HVLED2 Short**	**Bit [0]** **HVLED1 Short**
Reserved	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short

Table 22. LED Fault Enable (Address 0xB4)

Bits [7:2] **Not Used**	**Bit [1]** **Short Faults Enable**	**Bit [0]** **Open Faults Enable**
Reserved	0 = Disable (default) 1 = Enable	0 = Disable (default) 1 = Enable

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APPLICATION INFORMATION

Boost Converter Maximum Output Power (Boost)

The LM3697's maximum output power is governed by two factors: the peak current limit (I_{CL} = 880 mA min), and the maximum output voltage (V_{OVP}). When the application causes either of these limits to be reached it is possible that the proper current regulation and matching between LED current strings will not be met.

Peak Current Limited

In the case of a peak current limited situation, when the peak of the inductor current hits the LM3697's current limit, the NFET switch turns off for the remainder of the switching period. If this happens each switching cycle the LM3697 will regulate the peak of the inductor current instead of the headroom across the current sinks. This can result in the dropout of the boost output connected current sinks, and the LED current dropping below its programmed level.

The peak current in a boost converter is dependent on the value of the inductor, total LED current in the boost (IOUT), the boost output voltage (VOUT) (which is the highest voltage LED string + V_{HR}), the input voltage (VIN), the switching frequency, and the efficiency (Output Power/Input Power). Additionally, the peak current is different depending on whether the inductor current is continuous during the entire switching period (CCM), or discontinuous (DCM) where it goes to 0 before the switching period ends. For Continuous Conduction Mode the peak inductor current is given by:

$$\text{IPEAK} = \frac{\text{IOUT x VOUT}}{\text{VIN x efficiency}} + \left[\frac{\text{VIN}}{2 \text{ x } f_{SW} \text{ x L}} \text{ x } \left(1 - \frac{\text{VIN x efficiency}}{\text{VOUT}}\right)\right] \tag{7}$$

For Discontinuous Conduction Mode the peak inductor current is given by:

$$I_{PEAK} = \sqrt{\frac{2 \times I_{OUT}}{f_{SW} \times L \times \text{efficiency}} \times \left(V_{OUT} - V_{IN} \times \text{efficiency}\right)} \tag{8}$$

To determine which mode the circuit is operating in (CCM or DCM) it is necessary to perform a calculation to test whether the inductor current ripple is less than the anticipated input current (I_{IN}). If ΔI_L is less than I_{IN} then the device will be operating in CCM. If ΔI_L is greater than I_{IN} then the device is operating in DCM.

$$\frac{I_{OUT} \times V_{OUT}}{V_{IN} \times \text{efficiency}} > \frac{V_{IN}}{f_{SW} \times L} \times \left(1 - \frac{V_{IN} \times \text{efficiency}}{V_{OUT}}\right) \tag{9}$$

Typically at currents high enough to reach the LM3697's peak current limit, the device will be operating in CCM.

The following figures show the output current and voltage derating for a 10 µH and a 22 µH inductor. These plots take equations (1) and (2) from above and plot VOUT and IOUT with varying VIN, a constant peak current of 880 mA (I_{CL_MIN}), 500 kHz switching frequency, and a constant efficiency of 85%. Using these curves can give a good design guideline on selecting the correct inductor for a given output power requirement. A 10 µH inductor will typically be a smaller device with lower on resistance, but the peak currents will be higher. A 22 µH inductor provides for lower peak currents but a larger sized device is required to match the DC resistance of a 10 µH inductor.

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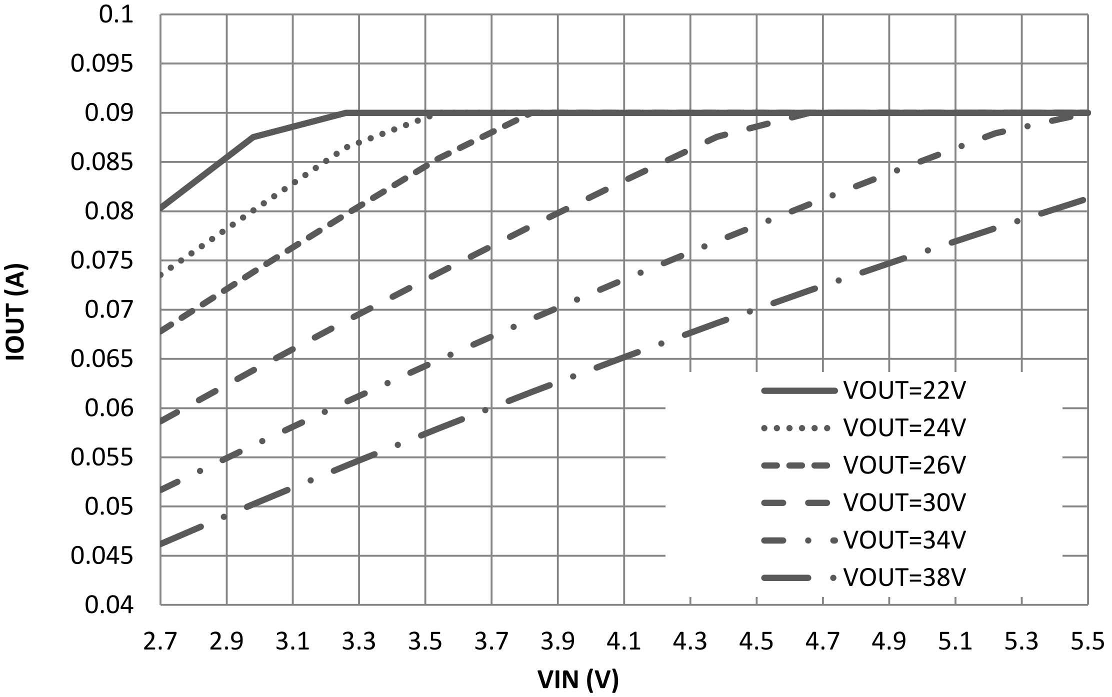

Figure 49. Maximum Output Power (22 µH)

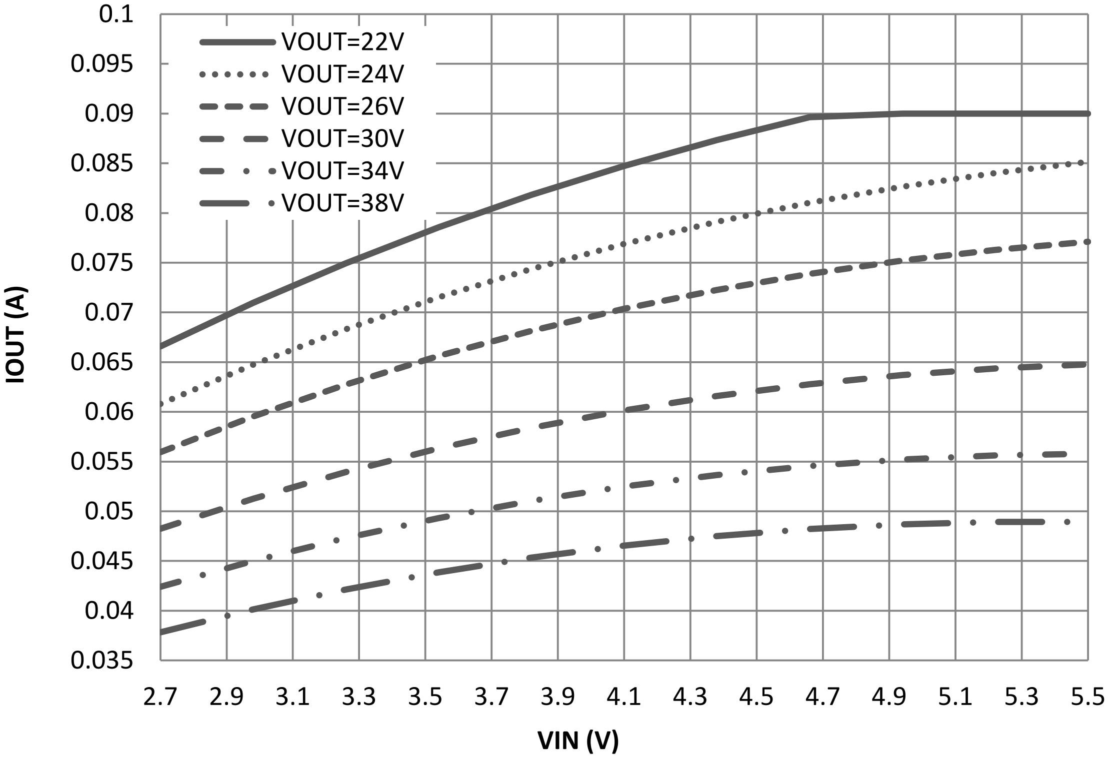

Figure 50. Maximum Output Power (10 µH)

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Output Voltage Limited

In the case of an output voltage limited situation, when the boost output voltage hits the LM3697's OVP threshold, the NFET turns off and stays off until the output voltage falls below the hysteresis level (typically 1V below the OVP threshold). This results in the boost converter regulating the output voltage to the programmed OVP threshold (16V, 24V, 32V, or 40V), causing the current sinks to go into dropout. The default OVP threshold is set at 16V. For LED strings higher than typically 4 series LEDs, the OVP will have to be programmed higher after power-up or after a HWEN reset.

Layout Guidelines and Component Selection (Boost)

The LM3697's inductive boost converter sees a high switched voltage (up to 40V) at the SW pin, and a step current (up to 1A) through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling (I = CdV/dt). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW pin and the OVP pin due to parasitic inductance in the step current conducting path (V = Ldi/dt). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise. Figure 51 highlights these two noise-generating components.

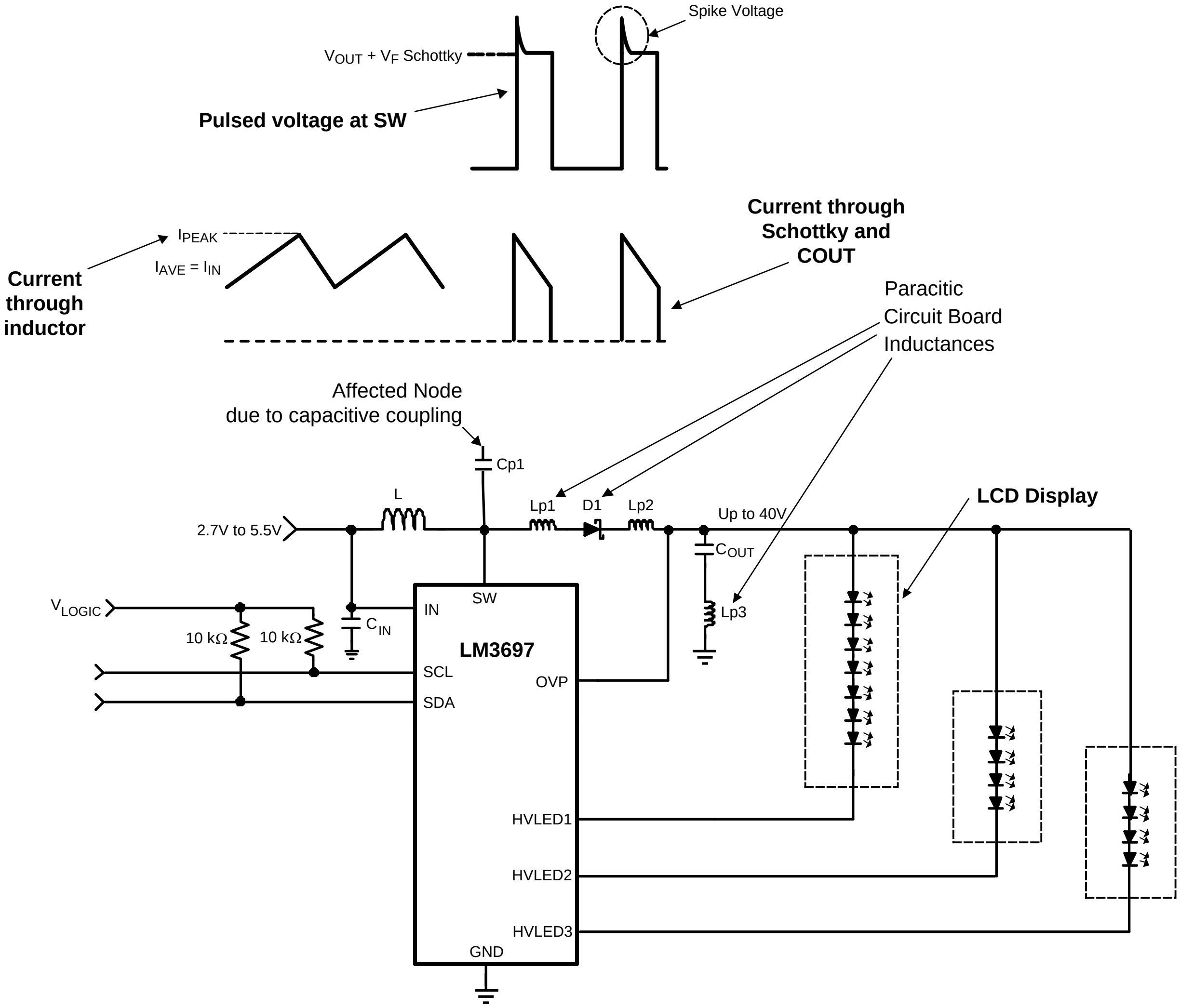

Figure 51. LM3697's Inductive Boost Converter Showing Pulsed Voltage at SW (High dV/dt) and Current Through Schottky and COUT (High dI/dt)

The following list details the main (layout sensitive) areas of the LM3697's inductive boost converter in order of decreasing importance:

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1. **Output Capacitor**
   - Schottky Cathode to COUT+
   - COUT− to GND
2. **Schottky Diode**
   - SW Pin to Schottky Anode
   - Schottky Cathode to COUT+
3. **Inductor**
   - SW Node PCB capacitance to other traces
4. **Input Capacitor**
   - CIN+ to IN pin

Boost Output Capacitor Selection and Placement

The LM3697's inductive boost converter requires a 1 µF output capacitor. The voltage rating of the capacitor depends on the selected OVP setting. For the 16V setting a 16V capacitor must be used. For the 24V setting a 25V capacitor must be used. For the 32V setting, a 35V capacitor must be used. For the 40V setting a 50V capacitor must be used. Pay careful attention to the capacitor's tolerance and DC bias response. For proper operation the degradation in capacitance due to tolerance, DC bias, and temperature, should stay above 0.4µF. This might require placing two devices in parallel in order to maintain the required output capacitance over the device operating range, and series LED configuration.

Because the output capacitor is in the path of the inductor current discharge path it will see a high-current step from 0 to I_{PEAK} each time the switch turns off and the Schottky diode turns on. Any inductance along this series path from the cathode of the diode through COUT and back into the LM3697's GND pin will contribute to voltage spikes (V_{SPIKE} = LP_ × dI/dt) at SW and OUT. These spikes can potentially over-voltage the SW pin, or feed through to GND. To avoid this, COUT+ must be connected as close as possible to the Cathode of the Schottky diode, and COUT− must be connected as close as possible to the LM3697's GND bump. The best placement for COUT is on the same layer as the LM3697 in order to avoid any vias that can add excessive series inductance.

Schottky Diode Placement

The Schottky diode must have a reverse breakdown voltage greater than the LM3697's maximum output voltage (see Over-Voltage Protection (Inductive Boost) section). Additionally, the diode must have an average current rating high enough to handle the LM3697's maximum output current, and at the same time the diode's peak current rating must be high enough to handle the peak inductor current. Schottky diodes are required due to their lower forward voltage drop (0.3V to 0.5V) and their fast recovery time.

In the LM3697's boost circuit the Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode sees a high-current step from 0 to I_{PEAK} each time the switch turns off and the diode turns on. Any inductance in series with the diode will cause a voltage spike (V_{SPIKE} = LP_ × dI/dt) at SW and OUT. This can potentially over-voltage the SW pin, or feed through to VOUT and through the output capacitor and into GND. Connecting the anode of the diode as close as possible to the SW pin and the cathode of the diode as close as possible to COUT+ will reduce the inductance (LP_) and minimize these voltage spikes.

Inductor Placement

The node where the inductor connects to the LM3697's SW bump has 2 issues. First, a large switched voltage (0 to VOUT + VF_SCHOTTKY) appears on this node every switching cycle. This switched voltage can be capacitively coupled into nearby nodes. Second, there is a relatively large current (input current) on the traces connecting the input supply to the inductor and connecting the inductor to the SW bump. Any resistance in this path can cause voltage drops that can negatively affect efficiency and reduce the input operating voltage range.

To reduce the capacitive coupling of the signal on SW into nearby traces, the SW bump-to-inductor connection must be minimized in area. This limits the PCB capacitance from SW to other traces. Additionally, high-impedance nodes that are more susceptible to electric field coupling need to be routed away from SW and not directly adjacent or beneath. This is especially true for traces such as SCL, SDA, HWEN, and PWM. A GND plane placed directly below SW will dramatically reduce the capacitance from SW into nearby traces.

Lastly, limit the trace resistance of the VIN-to-inductor connection and from the inductor-to-SW connection, by use of short, wide traces.

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Boost Input Capacitor Selection and Placement

The input capacitor on the LM3697 filters the voltage ripple due to the switching action of the inductive boost and the capacitive charge pump doubler. A ceramic capacitor of at least 2.2 µF must be used.

For the LM3697's boost converter, the input capacitor filters the inductor current ripple and the internal MOSFET driver currents during turn on of the internal power switch. The driver current requirement can range from 50 mA at 2.7V to over 200 mA at 5.5V with fast durations of approximately 10 ns to 20 ns. This will appear as high di/dt current pulses coming from the input capacitor each time the switch turns on. Close placement of the input capacitor to the IN pin and to the GND pin is critical since any series inductance between IN and CIN+ or CIN− and GND can create voltage spikes that could appear on the VIN supply line and in the GND plane.

Close placement of the input bypass capacitor at the input side of the inductor is also critical. The source impedance (inductance and resistance) from the input supply, along with the input capacitor of the LM3697, form a series RLC circuit. If the output resistance from the source (RS) is low enough the circuit will be underdamped and will have a resonant frequency (typically the case). Depending on the size of LS the resonant frequency could occur below, close to, or above the LM3697's switching frequency. This can cause the supply current ripple to be:

1. Approximately equal to the inductor current ripple when the resonant frequency occurs well above the LM3697's switching frequency;
2. Greater than the inductor current ripple when the resonant frequency occurs near the switching frequency; or
3. Less than the inductor current ripple when the resonant frequency occurs well below the switching frequency. Figure 52 shows the series RLC circuit formed from the output impedance of the supply and the input capacitor.

The circuit is redrawn for the AC case where the VIN supply is replaced with a short to GND and the LM3697 + Inductor is replaced with a current source (ΔIL). Equation 1 is the criteria for an underdamped response. Equation 2 is the resonant frequency. Equation 3 is the approximated supply current ripple as a function of LS, RS, and CIN.

As an example, consider a 3.6V supply with 0.1Ω of series resistance connected to C_{IN} through 50 nH of connecting traces. This results in an under-damped input-filter circuit with a resonant frequency of 712 kHz. Since both the 1 MHz and 500 kHz switching frequency options lie close to the resonant frequency of the input filter, the supply current ripple is probably larger than the inductor current ripple. In this case, using equation 3, the supply current ripple can be approximated as 1.68 times the inductor current ripple (using a 500 kHz switching frequency) and 0.86 times the inductor current ripple using a 1 MHz switching frequency. Increasing the series inductance (LS) to 500 nH causes the resonant frequency to move to around 225 kHz, and the supply current ripple to be approximately 0.25 times the inductor current ripple (500 kHz switching frequency) and 0.053 times for a 1 MHz switching frequency.

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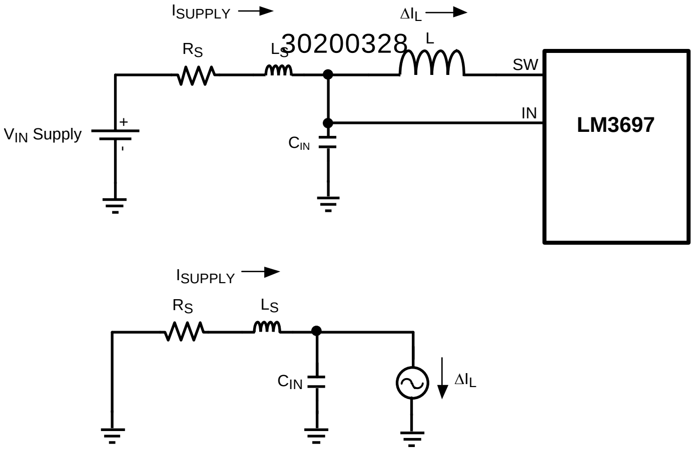

1. $$\frac{1}{L_S \times C_{IN}} > \frac{R_S^2}{4 \times L_S^2}$$

2. $$f_{RESONANT} = \frac{1}{2\pi\sqrt{L_S \times C_{IN}}}$$

3. $$I_{SUPPLYRIPPLE} \approx \Delta I_L \times \frac{\frac{1}{2\pi \times 500\ \text{kHz} \times C_{IN}}}{\sqrt{R_S^2 + \left(2\pi \times 500\ \text{kHz} \times L_S - \frac{1}{2\pi \times 500\ \text{kHz} \times C_{IN}}\right)^2}}$$

Figure 52. Input RLC Network

REVISION HISTORY

Changes from Original (November 2013) to Revision A **Page**

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3697YFQR	ACTIVE	DSBGA	YFQ	12	3000	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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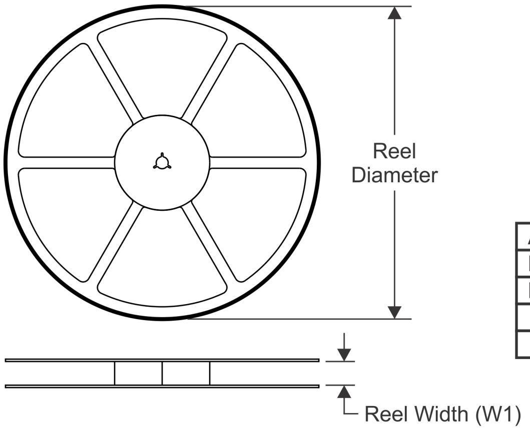
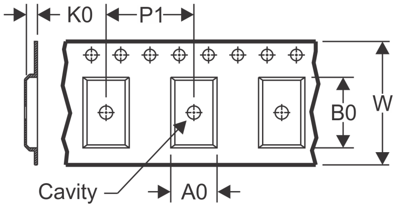
TAPE AND REEL INFORMATION

REEL DIMENSIONS

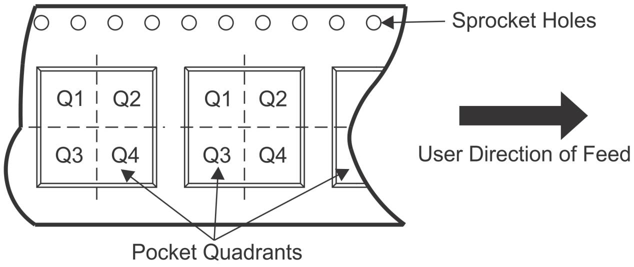


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

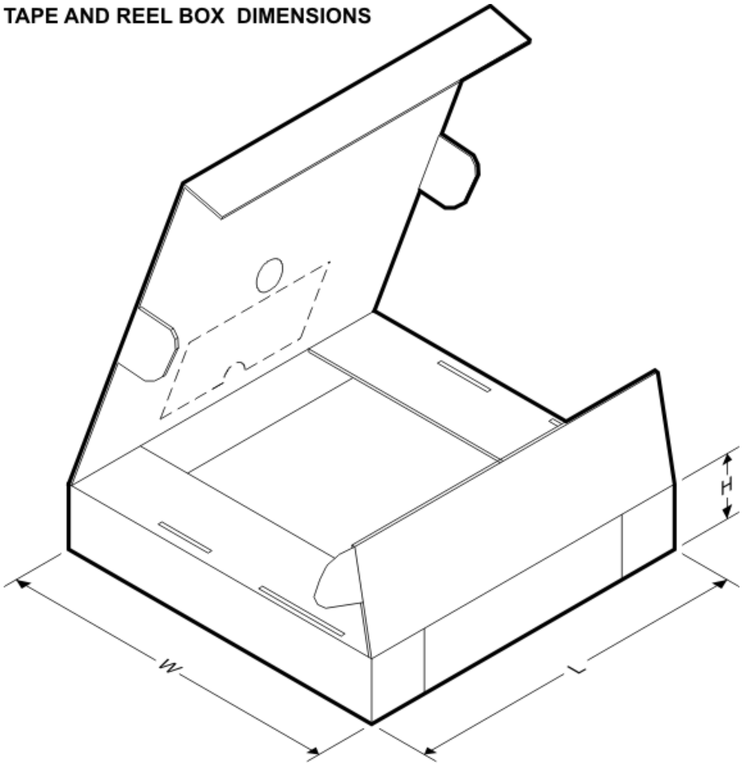
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3697YFQR	DSBGA	YFQ	12	3000	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1

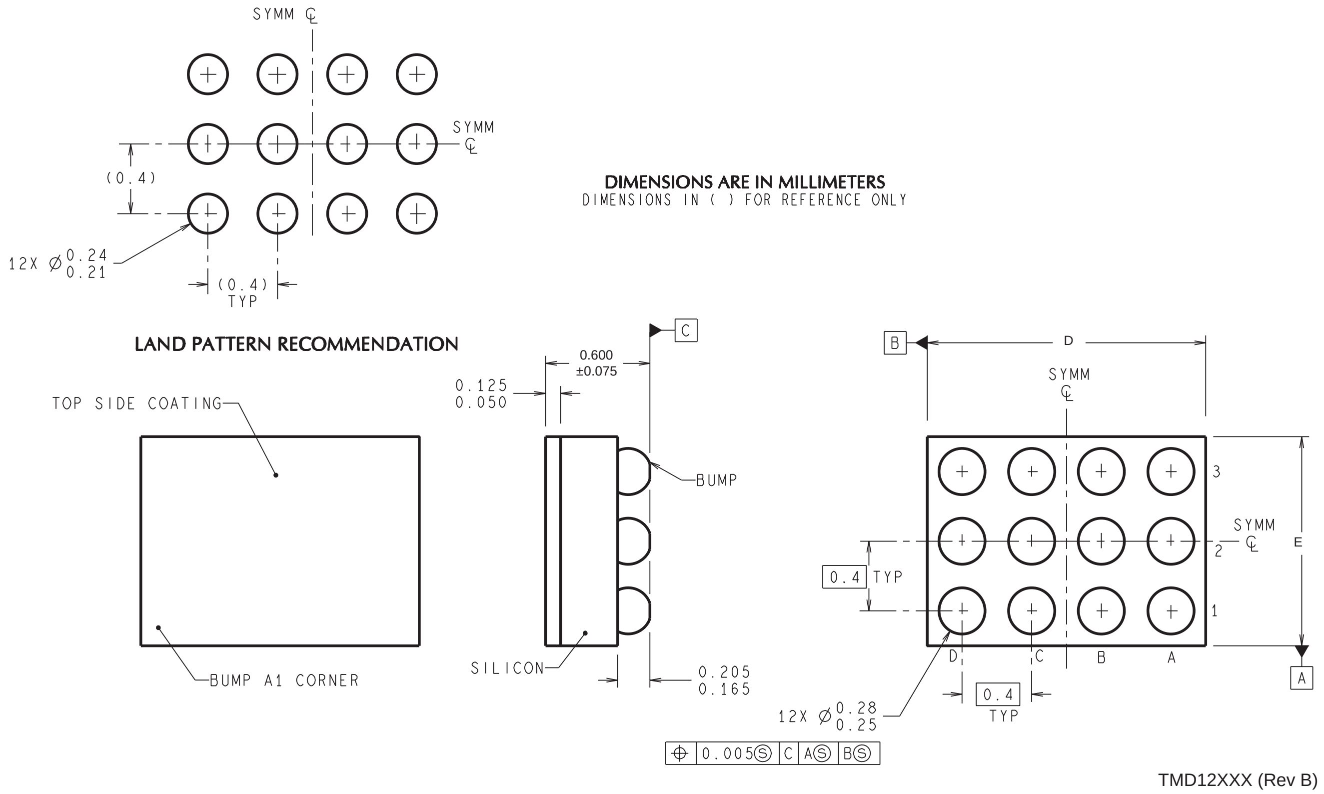
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3697YFQR	DSBGA	YFQ	12	3000	210.0	185.0	35.0

YFQ0012



D: Max = 1.64 mm, Min = 1.58 mm

E: Max = 1.29 mm, Min = 1.23 mm

4215079/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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