LM4140 High Precision Low Noise Low Dropout Voltage Reference

Check for Samples: LM4140

FEATURES

- **High Initial Accuracy: 0.1%**
- **Ultra Low Noise**
- **Low Temperature Coefficient: 3 ppm/°C (A grade)**
- **Low Voltage Operation: 1.8V**
- **Low Dropout Voltage: 20 mV (typ) @ 1mA**
- **Supply Current: 230 µA (typ), ≤ 1 µA Disable Mode**
- **Enable Pin**
- **Output Voltage Options: 1.024V, 1.250V, 2.048V, 2.500V, and 4.096V**
- **Custom Voltages from 0.5V to 4.5V**
- **Temperature Range (0°C to 70°C)**

APPLICATIONS SUMMARY

- **Portable, Battery Powered Equipment**
- **Instrumentation and Test Equipment**
- **Automotive**
- **Industrial Process Control**
- **Data Acquisition Systems**
- **Medical Equipment**
- **Precision Scales**
- **Servo Systems**
- **Battery Charging**

DESCRIPTION

The LM4140 series of precision references are designed to combine high accuracy, low drift and noise with low power dissipation in a small package.

The LM4140 is the industry's first reference with output voltage options lower than the bandgap voltage.

The key to the advance performance of the LM4140 is the use of EEPROM registers and CMOS DACs for temperature coefficient curvature correction and trimming of the output voltage accuracy of the device during the final production testing.

The major advantage of this method is the much higher resolution available with DACs than is available economically with most methods utilized by other bandgap references.

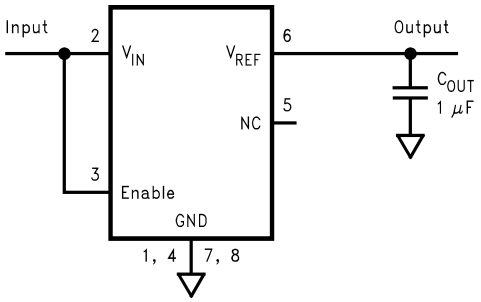
The low input and dropout voltage, low supply current and output drive capability of the LM4140 makes this product an ideal choice for battery powered and portable applications.

The LM4140 is available in three grades (A, B, C) with 0.1% initial accuracy and 3, 6 and 10 ppm/°C temperature coefficients. For even lower Tempco, contact Texas Instruments.

The device performance is specified over the temperature range (0°C to +70°C) and is available in compact 8-pin package.

For other output voltage options from 0.5V to 4.5V, contact Texas Instruments.

Typical Application



C_{OUT}, Output bypass capacitor. See text for selection detail.

Figure 1.

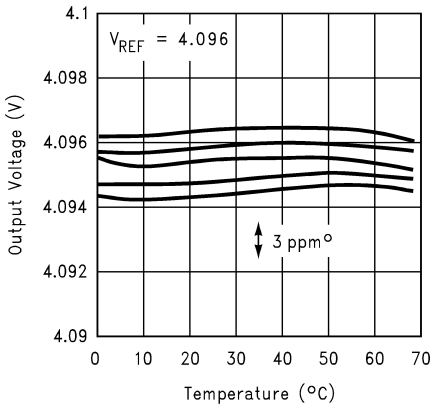


Figure 2. Typical Temperature Coefficient (Sample of 5 Parts)

Connection Diagram

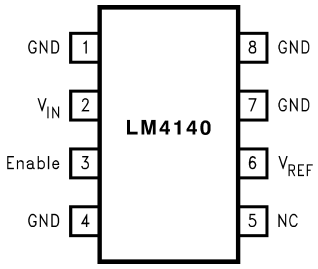


Figure 3. 8-Lead Surface Mount
Package Number D0008A
Top View

PIN DESCRIPTIONS

V_{ref} (Pin 6):	Reference Output. Capable of sourcing up to 8mA.
Input (Pin 2):	Positive Supply.
Ground (Pins 1, 4, 7, 8):	Negative Supply or Ground Connection. These pins must be connected to ground.
Enable (Pin 3):	Pulled to input for normal operation. Forcing this pin to ground will turn-off the output.
NC (Pin 5):	This pin must be left open.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Maximum Voltage on any Input pin	−0.3V to 5.6V
Output Short-Circuit Duration	Indefinite
Power Dissipation (T_A = 25°C) (3)	345mW
ESD Susceptibility (4) Human Body Model Machine Model	 2 kV 200V
Lead Temperature: Soldering, (10 sec.)	 +260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) Without PCB copper enhancements. The maximum power dissipation must be de-rated at elevated temperatures and is limited by T_{JMAX} (maximum junction temperature), θ_{J-A} (junction to ambient thermal resistance) and T_A (ambient temperature). The maximum power dissipation at any temperature is: $PDiss_{MAX} = (T_{JMAX} - T_A)/\theta_{J-A}$ up to the value listed in the Absolute Maximum Ratings. The θ_{J-A} for the SO-8 package is 160°C/W.

(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Operating Range (1)

Storage Temperature Range	−65°C to +150°C
Ambient Temperature Range	0°C to 70°C
Junction Temperature Range	0°C to 80°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

LM4140 Electrical Charateristics

Unless otherwise specified, V_{IN} = 3.0V for the LM4140-1.024 and LM4140-1.250, V_{IN} = 5.0V for all other voltage options, $V_{EN} = V_{IN}$. C_{OUT} = 1µF (1), I_{LOAD} = 1mA, $T_A = T_J$ = 25°C. Limits with standard typeface are for T_A = 25°C, and limits in **boldface type** apply over 0°C to 70°C temperature range.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{REF}	Output Voltage Initial Accuracy (4) LM4140B-1.024 LM4140B-1.250 LM4140B-2.048 LM4140B-2.500 LM4140B-4.096				±0.1	%
	LM4140C-1.024 LM4140C-1.250 LM4140C-2.048 LM4140C-2.500 LM4140C-4.096				±0.1	

(1) For proper operation, a 1µF capacitor is required between the output pin and the GND pin of the device. (See Application Hints for details)

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

(3) Typical numbers are at 25°C and represent the most likely parametric norm.

(4) High temperature and mechanical stress associated with PCB assembly can have significant impact on the initial accuracy of the LM4140 and may create significant shifts in V_{REF}. See Application Hints section regarding accuracy and PCB layout consideration.

LM4140
Electrical Charateristics (continued)

Unless otherwise specified, V_{IN} = 3.0V for the LM4140-1.024 and LM4140-1.250, V_{IN} = 5.0V for all other voltage options, V_{EN} = V_{IN}. C_{OUT} = 1µF (1), I_{LOAD} = 1mA, T_A = T_J = 25°C. Limits with standard typeface are for T_A = 25°C, and limits in **boldface type** apply over 0°C to 70°C temperature range.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
TCV_{REF}/°C	Temperature Coefficient: A Grade B Grade C Grade	0°C ≤ T_A ≤ + 70°C			 **3** **6** **10**	ppm/°C
$\Delta V_{REF}/\Delta V_{IN}$	Line Regulation					ppm/V
	1.024V and 1.250V options	1.8V ≤ V_{IN} ≤ 5.5V		50	300	
					350	
	All other voltage options	V_{ref} + 200mV ≤ V_{IN} ≤ 5.5V		20	200 **250**	
$\Delta V_{REF}/\Delta I_{LOAD}$	Load Regulation	1 mA ≤ I_{LOAD} ≤ 8mA				ppm/mA
	All other voltage options			1	20	
					150	
	4.096V Option			5	35	
					150	
ΔV_{REF}	Long-Term Stability	1000 Hrs		60		ppm
ΔV_{REF}	Thermal Hysteresis (5)	0°C ≤ T_A ≤ + 70°C		20		ppm
Operating Voltage	LM4140-1.024, LM4140-1.250	I_L = 1 mA to 8 mA	**1.8**		**5.5**	V
V_{IN}-V_{REF}	Dropout Voltage (6) LM4140-2.048, LM4140-2.500	I_L = 1 mA		20	40 **45**	mV
		I_L = 8 mA		160	235 **400**	
	LM4140-4.096	I_L = 1 mA		20	40 **45**	
		I_L = 8 mA		195	270 **490**	
V_N	Output Noise Voltage (7)	0.1 Hz to 10 Hz		2.2		μV_{PP}
$I_{S(ON)}$	Supply Current	I_{LOAD} = 0 mA				µA
	All other voltage options			230	320	
					375	
	4.096V Option			265	350	
					400	
$I_{S(OFF)}$	Supply Current	V_{Enable} < 0.4V		.01	**1**	µA
V_H	Logic High Input Voltage		**0.8V_{IN}**			V
I_H	Logic High Input Current			2		nA
V_L	Logic Low Input Voltage				**0.4**	V
I_L	Logic Low Input Current			1		nA
I_{SC}	Short Circuit Current		**8.5**	20	35 **40**	mA

(5) Thermal hysteresis is defined as the changes in +25°C output voltage before and after the cycling of the device from 0°C to 70°C.
(6) Dropout voltage is defined as the minimum input to output differential voltage at which the output voltage drops by 0.5% below the value measured with V_{IN} = 3.0V for the LM4140-1.024 and LM4140-1.250, V_{IN} = 5.0V for all other voltage options.
(7) The output noise is based on 1.024V option. Output noise is linearly proportional to V_{REF}.

LM4140 Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C, No Load, C_{OUT} = 1µF, V_{IN} = 3.0V for LM4140-1.024 and LM4140-1.250, and 5V for all other voltage options. V_{IN} = V_{EN}.

Power Up/Down Ground Current

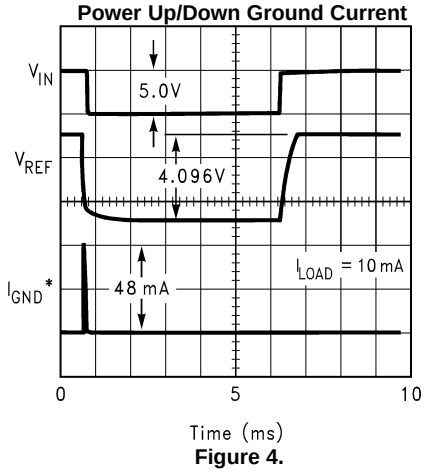


Figure 4.

Enable Response

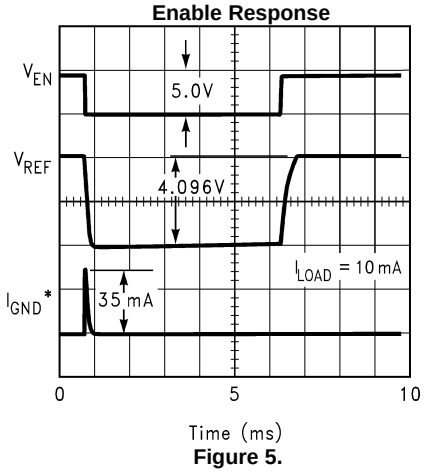


Figure 5.

* The 1µF output capacitor is actively discharged to ground. See ON/OFF OPERATION section for more details.

Line Transient Response

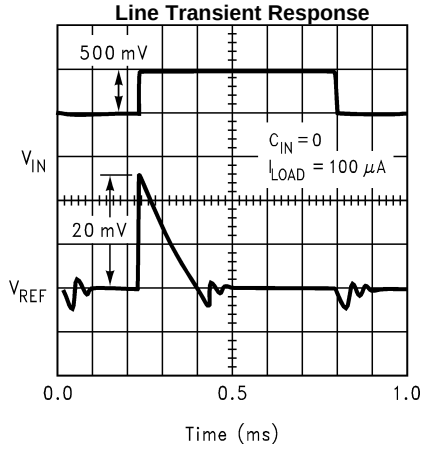


Figure 6.

Load Transient Response

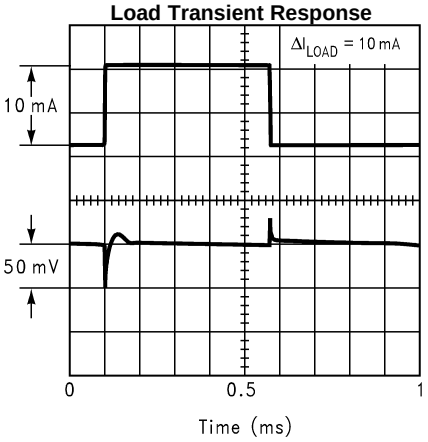


Figure 7.

Output Impedance

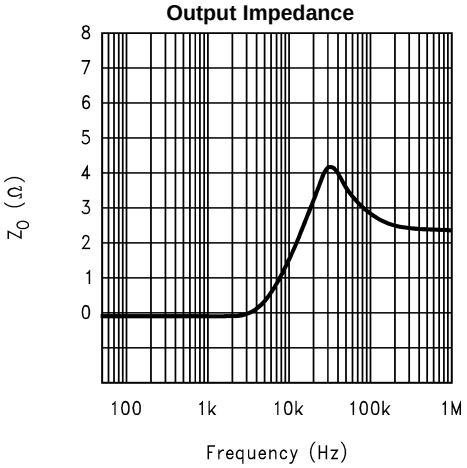


Figure 8.

Power Supply Rejection Ratio

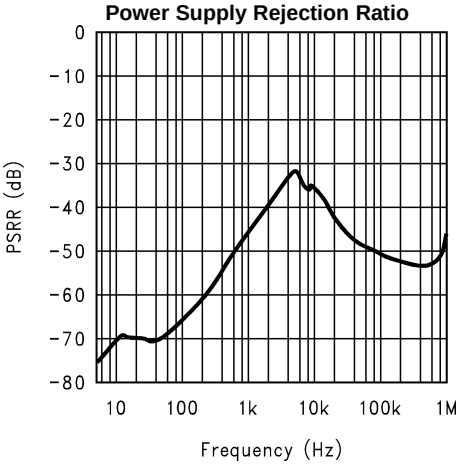
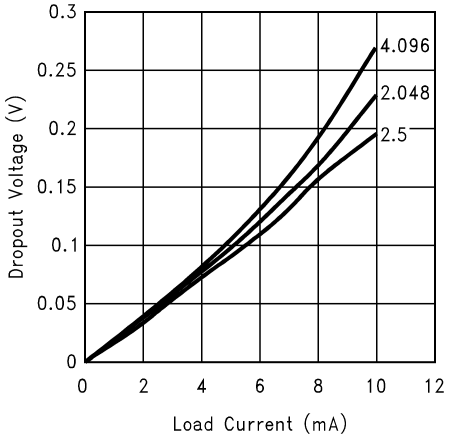


Figure 9.

LM4140 Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, No Load, C_{OUT} = 1µF, V_{IN} = 3.0V for LM4140-1.024 and LM4140-1.250, and 5V for all other voltage options. V_{IN} = V_{EN}.

Dropout Voltage vs Load Current



Note: 1.024V and 1.250V options require 1.8V supply.

Figure 10.

Output Voltage Change vs Sink Current (I_{SINK})

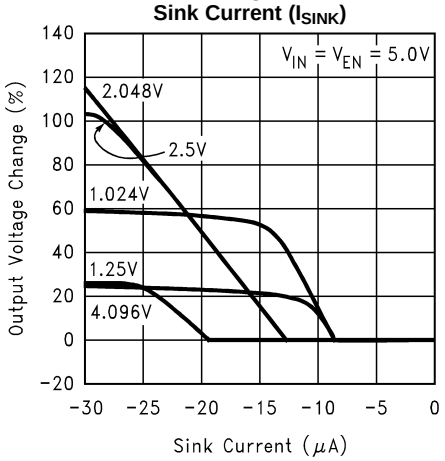


Figure 11.

Total Current ($I_{S(OFF)}$) vs Supply Voltage

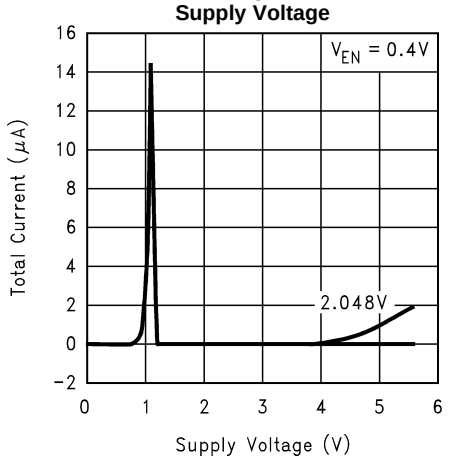


Figure 12.

Total Current ($I_{S(ON)}$) vs Supply Voltage

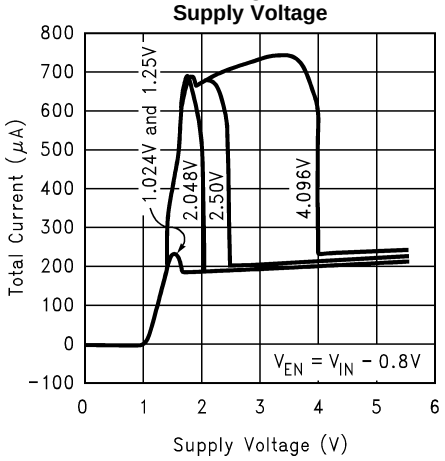


Figure 13.

Spectral Noise Density (0.1Hz to 10Hz)

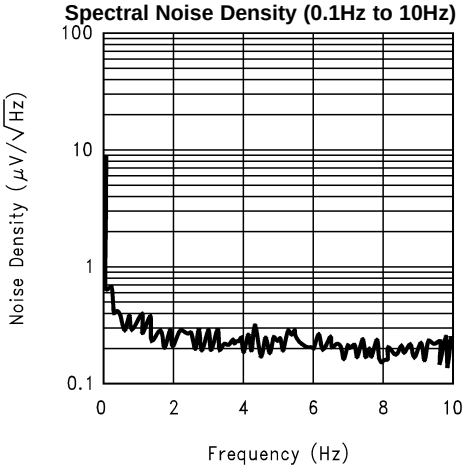


Figure 14.

Spectral Noise Density (10Hz to 100kHz)

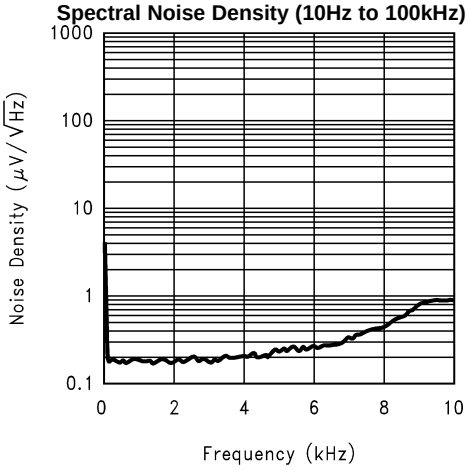


Figure 15.

LM4140 Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, No Load, C_{OUT} = 1µF, V_{IN} = 3.0V for LM4140-1.024 and LM4140-1.250, and 5V for all other voltage options. V_{IN} = V_{EN}.

Ground Current vs Load Current

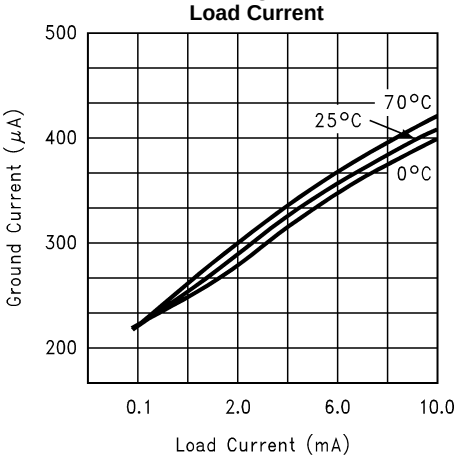


Figure 16.

Long Term Drift

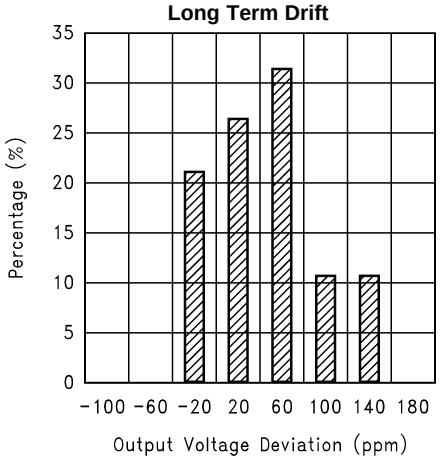


Figure 17.

Load Regulation vs Temperature

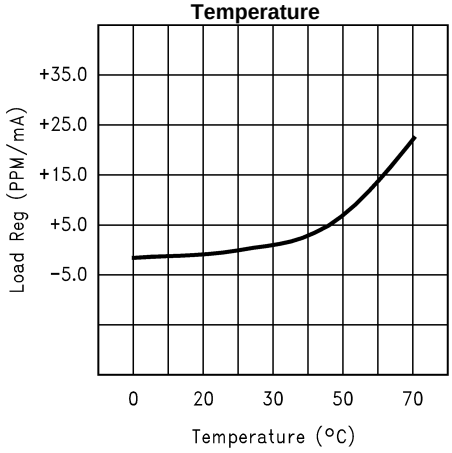


Figure 18.

Output Voltage vs Load Current

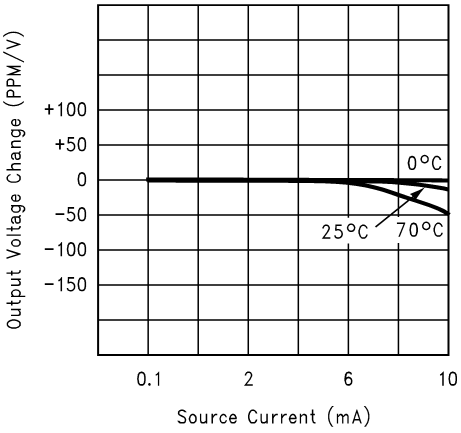


Figure 19.

Line Regulation vs Temperature

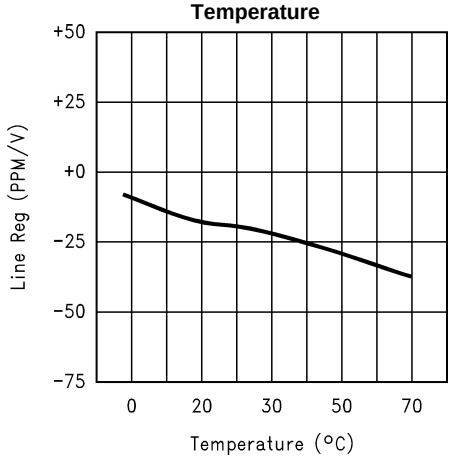


Figure 20.

I_Q vs Temperature

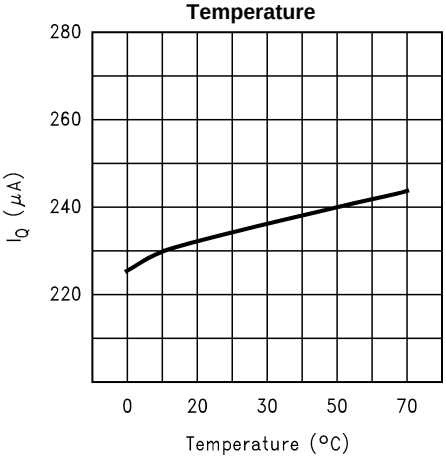


Figure 21.

LM4140 Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, No Load, C_{OUT} = 1µF, V_{IN} = 3.0V for LM4140-1.024 and LM4140-1.250, and 5V for all other voltage options. V_{IN} = V_{EN}.

Short Circuit Current vs Temperature

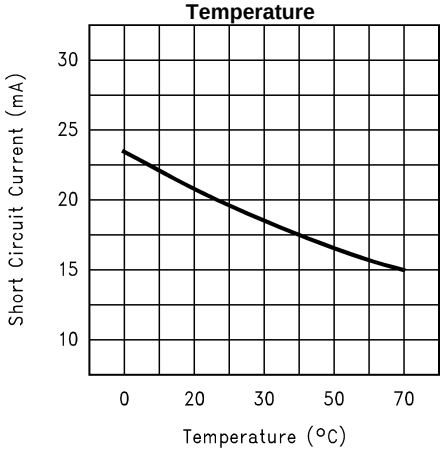


Figure 22.

Dropout Voltage vs Load Current (V_{OUT}) = 2.0V

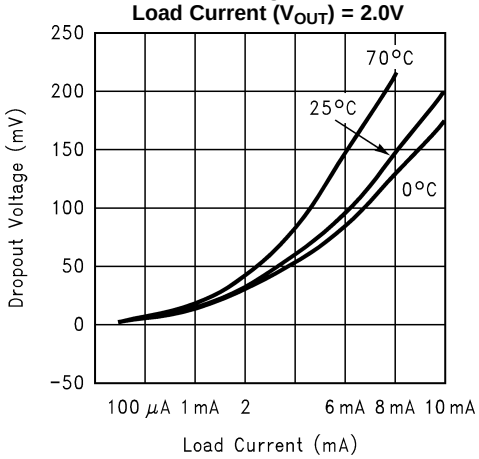


Figure 23.

APPLICATION HINTS

INPUT CAPACITORS

Although not always required, an input capacitor is recommended. A supply bypass capacitor on the input assures that the reference is working from a source with low impedance, which improves stability. A bypass capacitor can also improve transient response by providing a reservoir of stored energy that the reference can utilize in case where the load current demand suddenly increases. The value used for C_{IN} may be used without limit. Refer to the Typical Application section for examples of input capacitors.

OUTPUT CAPACITORS

The LM4140 requires a 1µF (nominally) output capacitor for loop stability (compensation) as well as transient response. During the sudden changes in load current demand, the output capacitor must source or sink current during the time it takes the control loop of the LM4140 to respond.

This capacitor must be selected to meet the requirements of minimum capacitance and equivalent series resistance (ESR) range.

In general, the capacitor value must be at least 0.2µF (over the actual ambient operating temperature), and the ESR must be within the range indicated in Figure 24, Figure 25 and Figure 26.

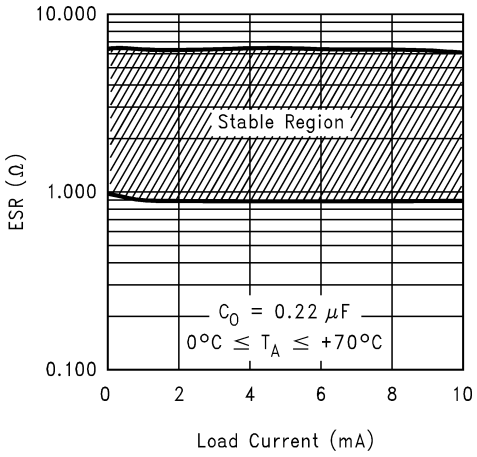


Figure 24. 0.22 µF ESR Range

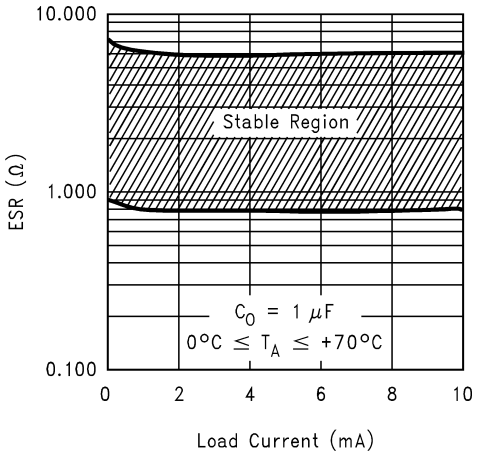


Figure 25. 1 µF ESR Range

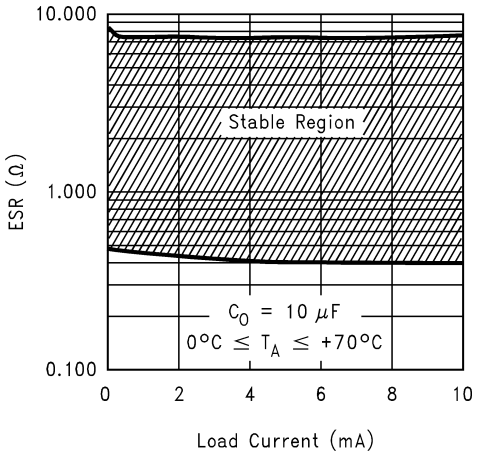


Figure 26. 10 µF ESR Range

TANTALUM CAPACITORS

Surface-mountable solid tantalum capacitors offer a good combination of small physical size for the capacitance value, and ESR in the range needed for by the LM4140. The results of testing the LM4140 stability with surface mount solid tantalum capacitors show good stability with values in the range of 0.1µF. However, optimum performance is achieved with a 1µF capacitor.

Tantalum capacitors that have been verified as suitable for use with the LM4140 are shown in Table 1.

Table 1. Surface-Mount Tantalum Capacitor Selection Guide

1µF Surface-Mount Tantalums	
Manufacturer	**Part Number**
Kemet	T491A105M010AS
NEC	NRU105N10
Siemens	B45196-E3105-K
Nichicon	F931C105MA
Sprague	293D105X0016A2T
2.2µF Surface-Mount Tantalums	
Kemet	T491A225M010AS
NEC	NRU225M06
Siemens	B45196/2.2/10/10
Nichicon	F930J225MA
Sprague	293D225X0010A2T

ALUMINUM ELECTROLYTIC CAPACITORS

Although probably not a good choice for a production design, because of relatively large physical size, an aluminium electrolytic capacitor can be used in the design prototype for an LM4140 reference. A 1µF capacitor meeting the ESR conditions can be used. If the operating temperature drops below 0°C, the reference may not remain stable, as the ESR of the aluminium electrolytic capacitor will increase, and may exceed the limits indicated in the figures.

MULTILAYER CERAMIC CAPACITORS

Surface-mountable multilayer ceramic capacitors may be an attractive choice because of their relatively small physical size and excellent RF characteristics.

However, they sometimes have an ESR values lower than the minimum required by the LM4140, and relatively large capacitance change with temperature. The manufacturer's datasheet for the capacitor should be consulted before selecting a value. Test results of LM4140 stability using multilayer ceramic capacitors show that a minimum of 0.2µF is usually needed.

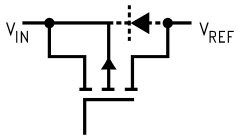
Multilayer ceramic capacitors that have been verified as suitable for use with the LM4140 are shown in Table 2.

Table 2. Surface-Mount Ceramic Capacitors Selection Guide

2.2µF Surface-Mount Ceramic	
Manufacturer	**Part Number**
Tokin	1E225ZY5U-C203
Murata	GRM42-6Y5V225Z16
4.7µF Surface-Mount Ceramic	
Tokin	1E475ZY5U-C304

REVERSE CURRENT PATH

The P-channel Pass transistor used in the LM4140 has an inherent diode connected between the V_{IN} and V_{REF} pins (see diagram below).



Forcing the output to voltages higher than the input, or pulling V_{IN} below voltage stored on the output capacitor by more than a V_{be}, will forward bias this diode and current will flow from the V_{REF} terminal to V_{IN}. No damage to the LM4140 will occur under these conditions as long as the current flowing into the output pin does not exceed 50mA.

ON/OFF OPERATION

The LM4140 is designed to quickly reduce both V_{REF} and I_Q to zero when turned-off. V_{REF} is restored in less than 200µs when turned-on. During the turn-off, the charge across the output capacitor is discharged to ground through internal circuitry.

The LM4140 is turned-off by pulling the enable input low, and turned-on by driving the input high. If this feature is not to be used, the enable pin should be tied to the V_{IN} to keep the reference on at all times (the enable pin must not be left floating).

To ensure proper operation, the signal source used to drive the enable pin must be able to swing above and below the specified high and low voltage thresholds which ensure an ON or OFF state (see LM4140 Electrical Charateristics).

The ON/OFF signal may come from either a totem-pole output, or an open-collector output with pull-up resistor to the LM4140 input voltage. This high-level voltage may exceed the LM4140 input voltage, but must remain within the Absolute Maximum Rating for the enable pin.

OUTPUT ACCURACY

Like all references, either series or shunt, the after assembly accuracy is made up of primarily three components: initial accuracy itself, thermal hysteresis and effects of the PCB assembly stress.

LM4140 provides an excellent output initial accuracy of 0.1% and temperature coefficient of 6ppm/°C (B Grade).

For best accuracy and precision, the LM4140 junction temperature should not exceed 70°C.

The thermal hysteresis curve on this datasheet are performance characteristics of three typical parts selected at random from a sample of 40 parts.

Parts are mounted in a socket to minimize the effect of PCB's mechnical expansion and contraction. Readings are taken at 25°C following multiple temperature cycles to 0°C and 70°C. The labels on the X axis of the graph indicates the device temperature cycle prior to measurement at 25°C.

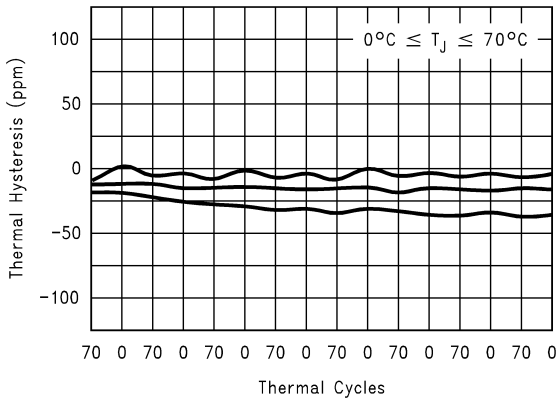


Figure 27. Typical Thermal Hysteresis

The mechanical stress due to the PCB's mechanical and thermal stress can cause an output voltage shift more than the true thermal coefficient of the device. References in surface mount packages are more susceptible to these stresses because of the small amount of plastic molding which support the leads.

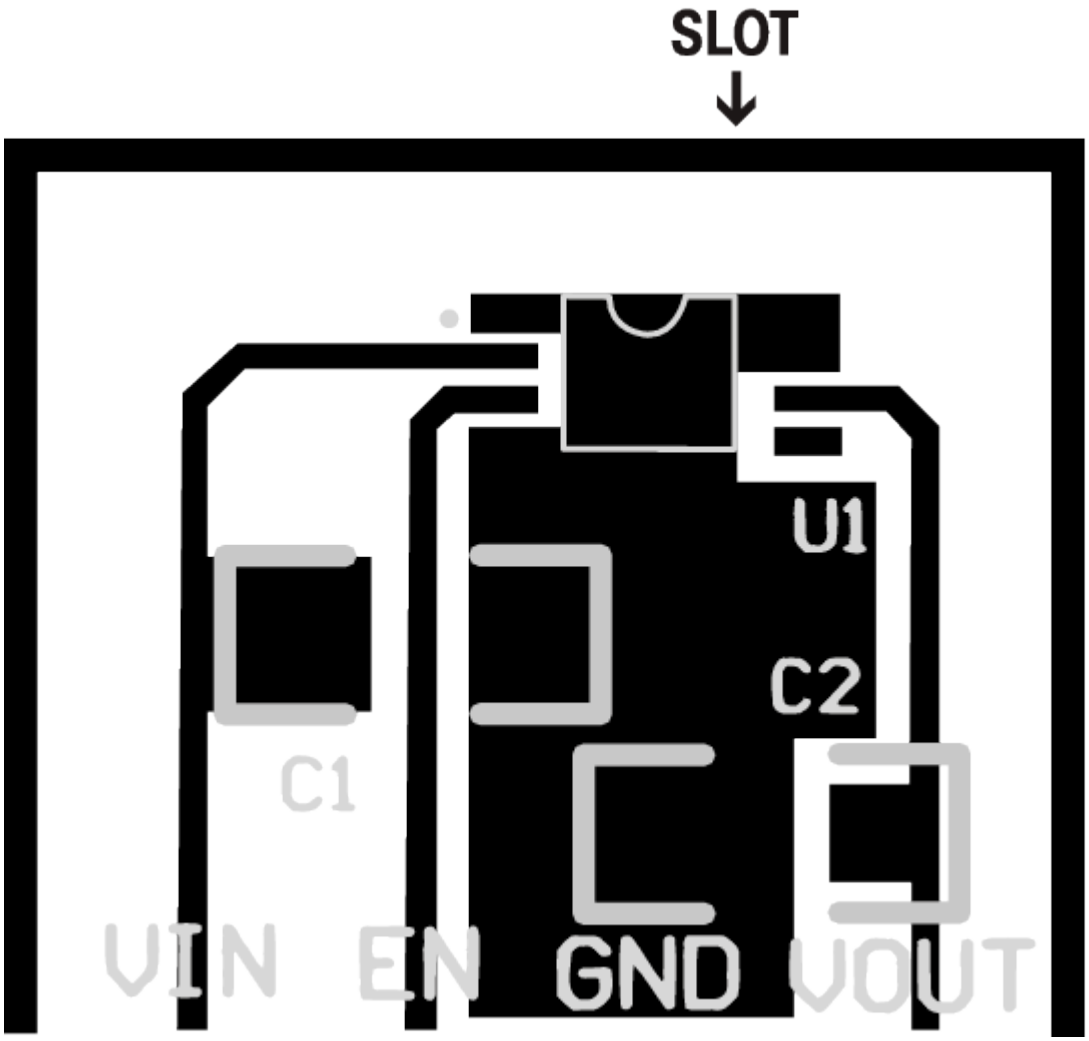
Following the recommendations on PCB LAYOUT CONSIDERATION section can minimize the mechanical stress on the device.

PCB LAYOUT CONSIDERATION

The simplest ways to reduce the stress related shifts are:

1. Mounting the device near the edges or the corners of the board where mechanical stress is at its minimum. The center of the board generally has the highest mechanical and thermal expansion stress.
2. Mechanical isolation of the device by creating an island by cutting a U shape slot on the PCB for mounting the device. This approach would also provide some thermal isolation from the rest of the circuit.

Figure 28 is a recommended printed board layout with a slot cut on three sides of the circuit layout to serve as a strain relief.



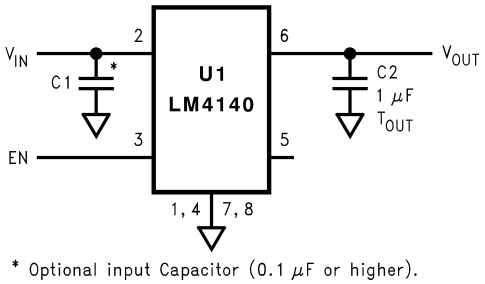


Figure 28. Suggested PCB Layout with Slot

Typical Application Circuits

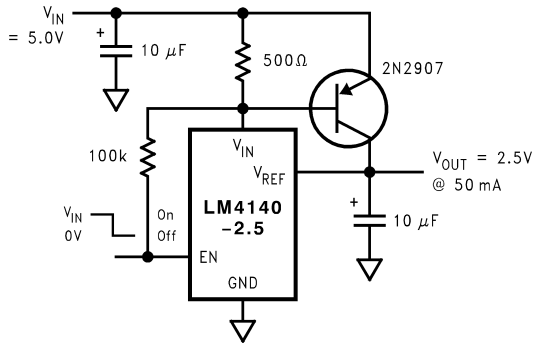


Figure 29. Boosted Output Current

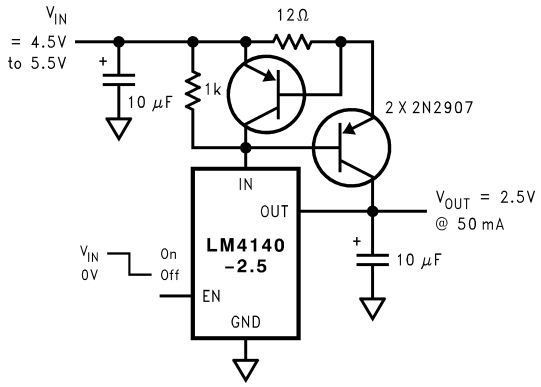


Figure 30. Boosted Ouput Current with Current Limiter

* Low Noise Op Amp such as OP-27

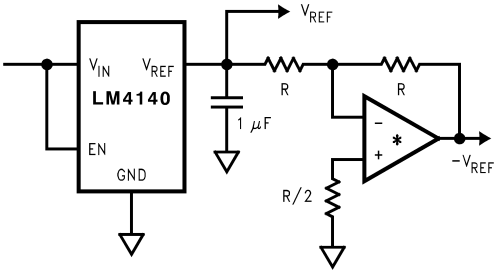


Figure 31. Complimentary Outputs

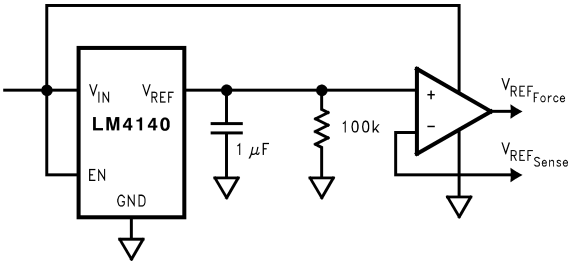
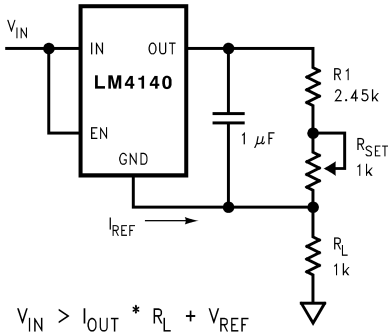


Figure 32. Voltage Reference with Force and Sense Output



$V_{IN} > I_{OUT} * R_L + V_{REF}$

$I_{OUT} = (V_{REF}/(R_1 + R_{SET})) + I_{REF}$

$R1 = 2.45k$ for

$I_L = 1\,mA$ using LM4120-2.5

Figure 33. Precision Programmable Current Source

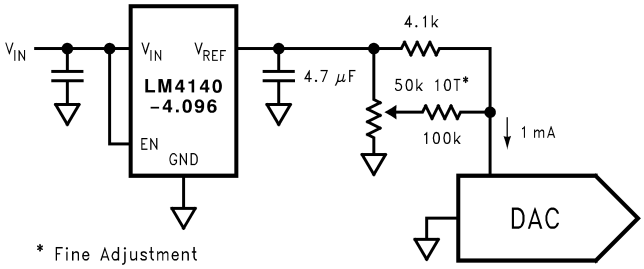


Figure 34. Precision DAC Reference

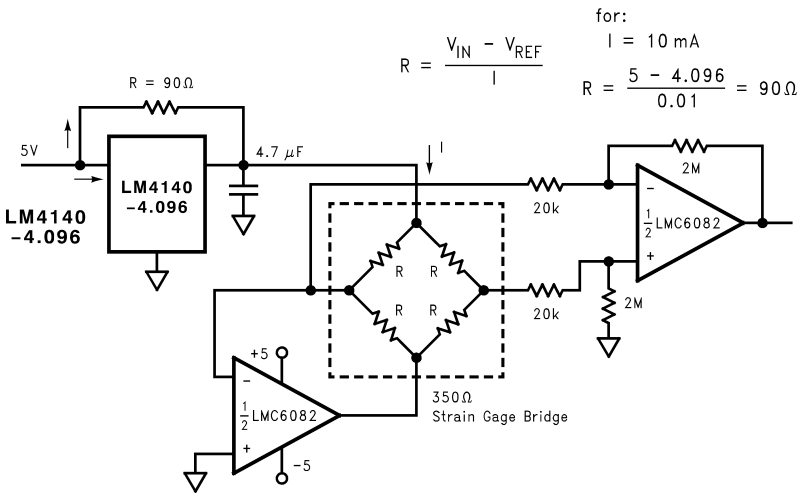


Figure 35. Strain Gauge Conditioner for 350Ω Bridge

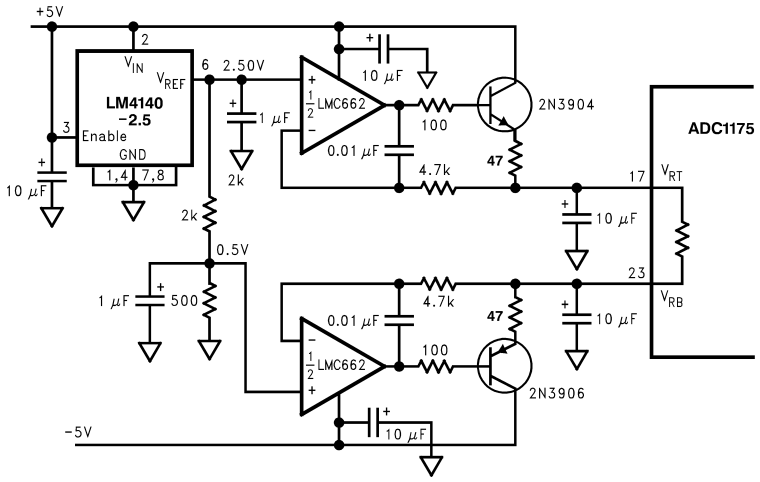


Figure 36.

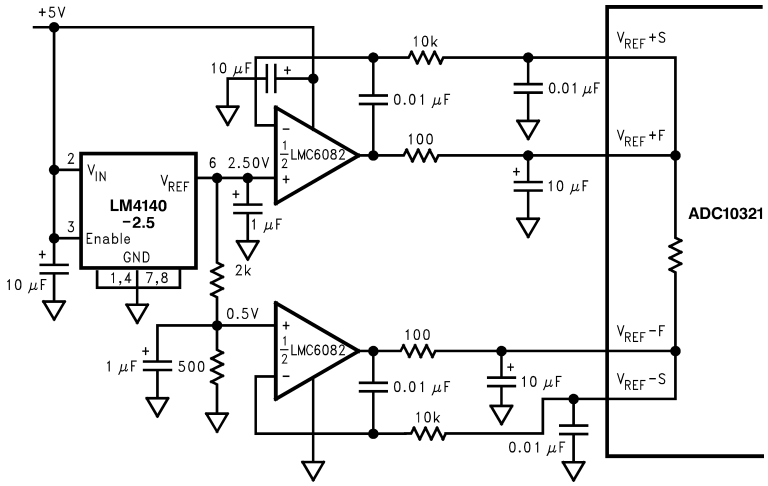


Figure 37.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4140ACM-1.0	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140A CM1.0	Samples
LM4140ACM-1.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM1.0	Samples
LM4140ACM-1.2	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140A CM1.2	Samples
LM4140ACM-1.2/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM1.2	Samples
LM4140ACM-2.0	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140A CM2.0	Samples
LM4140ACM-2.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM2.0	Samples
LM4140ACM-2.5	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140A CM2.5	Samples
LM4140ACM-2.5/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM2.5	Samples
LM4140ACM-4.1	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140A CM4.1	Samples
LM4140ACM-4.1/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM4.1	Samples
LM4140ACMX-2.5	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	4140A CM2.5	Samples
LM4140ACMX-2.5/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM2.5	Samples
LM4140ACMX-4.1	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	4140A CM4.1	Samples
LM4140ACMX-4.1/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140A CM4.1	Samples
LM4140BCM-1.0	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140B CM1.0	Samples
LM4140BCM-1.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM1.0	Samples
LM4140BCM-1.2	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140B CM1.2	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4140BCM-1.2/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM1.2	Samples
LM4140BCM-2.0	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140B CM2.0	Samples
LM4140BCM-2.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM2.0	Samples
LM4140BCM-2.5	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140B CM2.5	Samples
LM4140BCM-2.5/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM2.5	Samples
LM4140BCM-4.1	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140B CM4.1	Samples
LM4140BCM-4.1/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM4.1	Samples
LM4140BCMX-1.0	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	4140B CM1.0	Samples
LM4140BCMX-1.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM1.0	Samples
LM4140BCMX-2.5	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	4140B CM2.5	Samples
LM4140BCMX-2.5/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM2.5	Samples
LM4140BCMX-4.1	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	4140B CM4.1	Samples
LM4140BCMX-4.1/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140B CM4.1	Samples
LM4140CCM-1.0	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140C CM1.0	Samples
LM4140CCM-1.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM1.0	Samples
LM4140CCM-1.2	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140C CM1.2	Samples
LM4140CCM-1.2/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM1.2	Samples
LM4140CCM-2.0	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140C CM2.0	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4140CCM-2.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM2.0	Samples
LM4140CCM-2.5	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140C CM2.5	Samples
LM4140CCM-2.5/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM2.5	Samples
LM4140CCM-4.1	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	4140C CM4.1	Samples
LM4140CCM-4.1/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM4.1	Samples
LM4140CCMX-1.0	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	4140C CM1.0	Samples
LM4140CCMX-1.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM1.0	Samples
LM4140CCMX-1.2	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	4140C CM1.2	Samples
LM4140CCMX-1.2/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM1.2	Samples
LM4140CCMX-2.5	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	4140C CM2.5	Samples
LM4140CCMX-2.5/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM2.5	Samples
LM4140CCMX-4.1	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	4140C CM4.1	Samples
LM4140CCMX-4.1/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	4140C CM4.1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

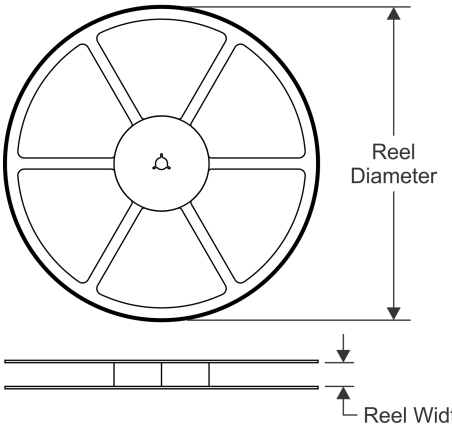
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

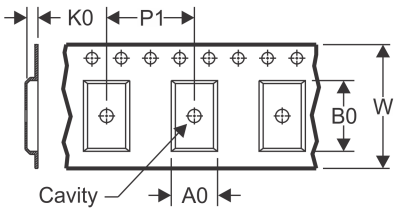
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

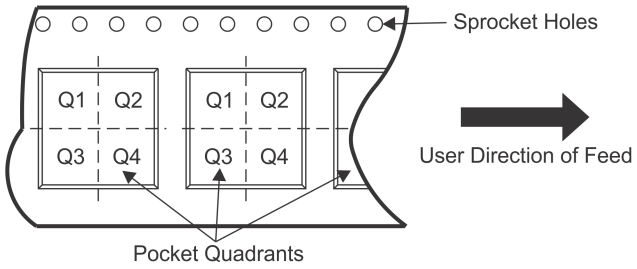


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

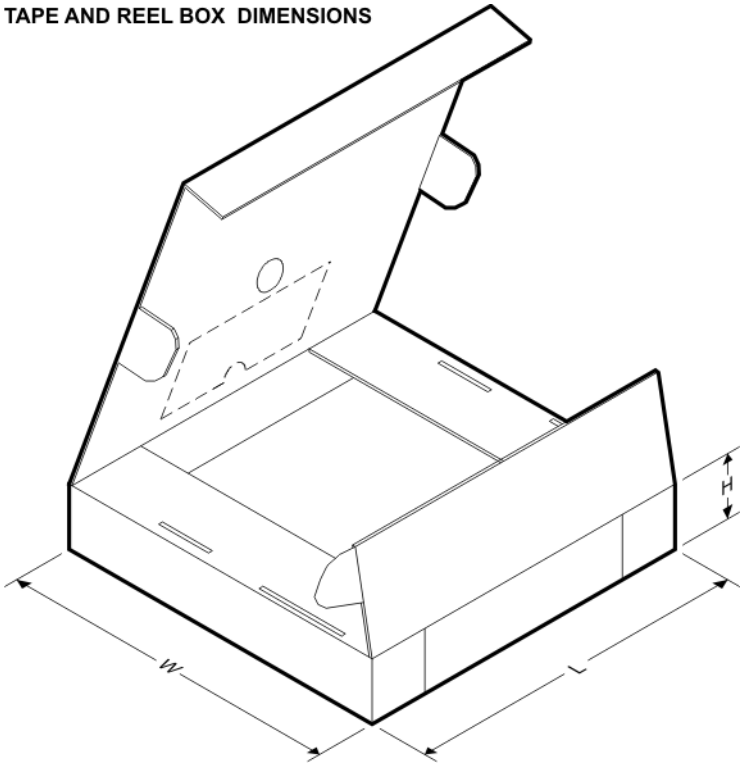
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4140ACMX-2.5	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140ACMX-2.5/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140ACMX-4.1	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140ACMX-4.1/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140BCMX-1.0	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140BCMX-1.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140BCMX-2.5	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140BCMX-2.5/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140BCMX-4.1	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140BCMX-4.1/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140CCMX-1.0	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140CCMX-1.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140CCMX-1.2	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140CCMX-1.2/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140CCMX-2.5	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140CCMX-2.5/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140CCMX-4.1	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4140CCMX-4.1/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

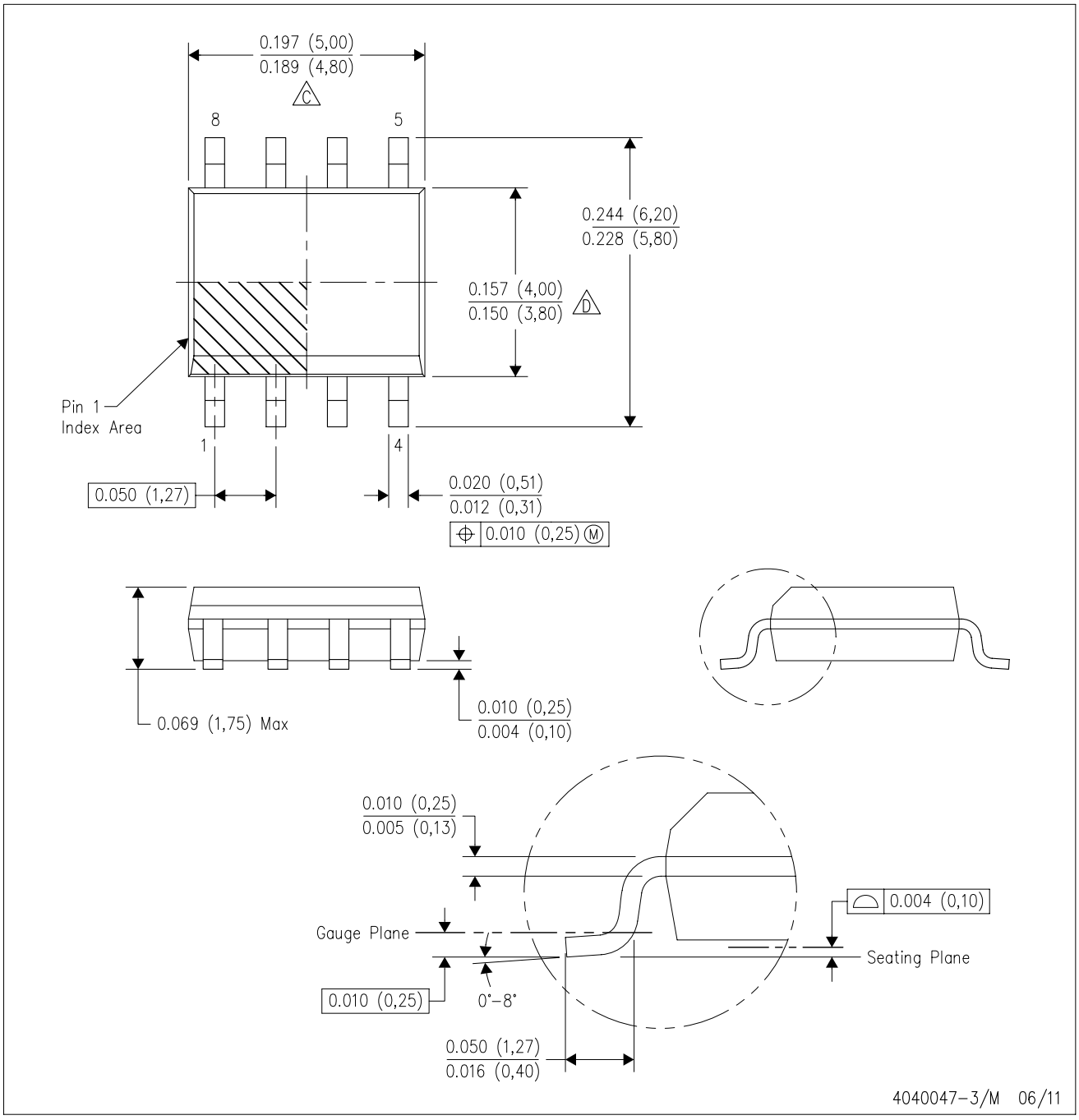
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4140ACMX-2.5	SOIC	D	8	2500	367.0	367.0	35.0
LM4140ACMX-2.5/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140ACMX-4.1	SOIC	D	8	2500	367.0	367.0	35.0
LM4140ACMX-4.1/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140BCMX-1.0	SOIC	D	8	2500	367.0	367.0	35.0
LM4140BCMX-1.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140BCMX-2.5	SOIC	D	8	2500	367.0	367.0	35.0
LM4140BCMX-2.5/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140BCMX-4.1	SOIC	D	8	2500	367.0	367.0	35.0
LM4140BCMX-4.1/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140CCMX-1.0	SOIC	D	8	2500	367.0	367.0	35.0
LM4140CCMX-1.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140CCMX-1.2	SOIC	D	8	2500	367.0	367.0	35.0
LM4140CCMX-1.2/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140CCMX-2.5	SOIC	D	8	2500	367.0	367.0	35.0
LM4140CCMX-2.5/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4140CCMX-4.1	SOIC	D	8	2500	367.0	367.0	35.0
LM4140CCMX-4.1/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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