

## LMC555 CMOS Timer

Check for Samples: [LMC555](#)

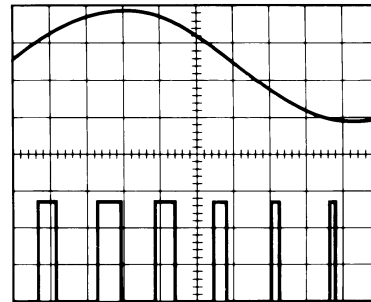
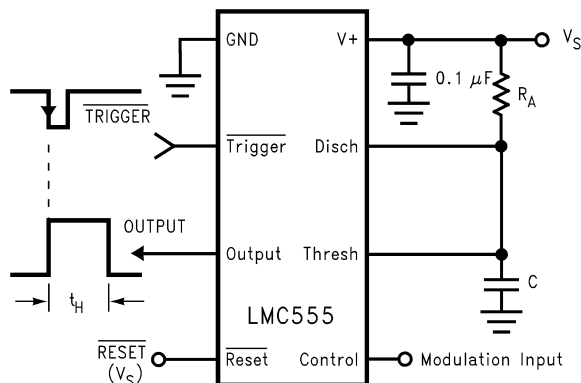
### FEATURES

- Less than 1 mW Typical Power Dissipation at 5V Supply
- 3 MHz Astable Frequency Capability
- 1.5V Supply Operating Voltage Ensured
- Output Fully Compatible with TTL and CMOS Logic at 5V Supply
- Tested to  $-10$  mA,  $+50$  mA Output Current Levels
- Reduced Supply Current Spikes During Output Transitions
- Extremely Low Reset, Trigger, and Threshold Currents
- Excellent Temperature Stability
- Pin-for-Pin Compatible with 555 Series of Timers
- Available in 8-pin VSSOP Package and 8-Bump DSBGA package

### DESCRIPTION

The LMC555 is a CMOS version of the industry standard 555 series general purpose timers. In addition to the standard package (SOIC, VSSOP, and PDIP) the LMC555 is also available in a chip sized package (8 Bump DSBGA) using TI's DSBGA package technology. The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the stable mode the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of Texas Instruments' LMC MOS process extends both the frequency range and low supply capability.

### Pulse Width Modulator



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Connection Diagram

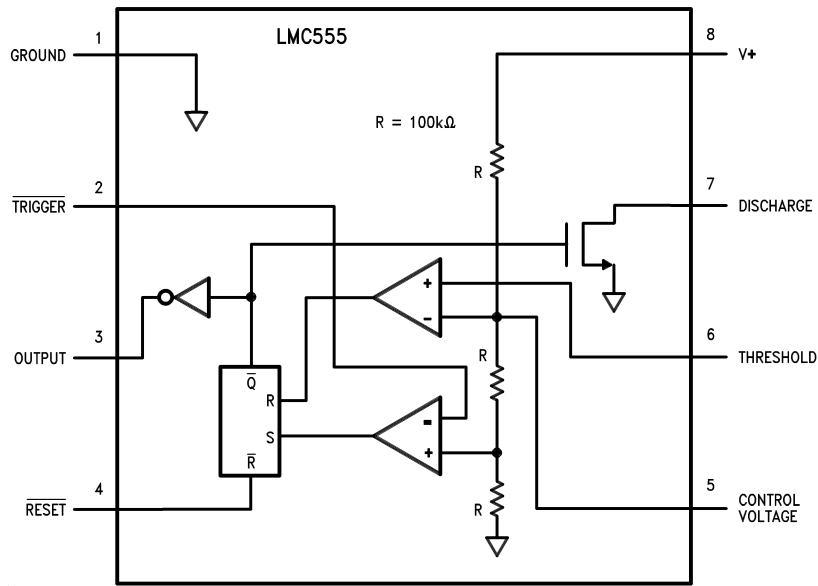


Figure 1. 8-Pin SOIC, VSSOP, PDIP Top View

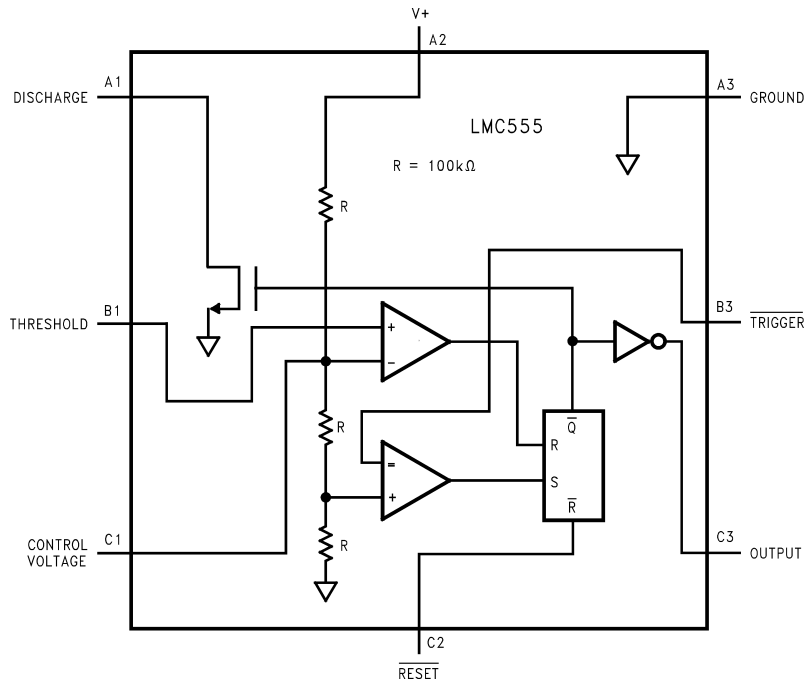


Figure 2. 8-Bump DSBGA Top View (Bump Side Down)

**Table 1. Pin Descriptions**

Pin Name	Package Pin Numbers	
	8-Pin SOIC, VSSOP, and PDIP	8-Bump DSBGA
GND	1	A3
Trigger	2	B3
Output	3	C3
Reset	4	C2
Control Voltage	5	C1
Threshold	6	B1
Discharge	7	A1
V <sup>+</sup>	8	A2



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings<sup>(1)(2)(3)</sup>**

Supply Voltage, V <sup>+</sup>	15V
Input Voltages, V <sub>TRIG</sub> , V <sub>RES</sub> , V <sub>CTRL</sub> , V <sub>THRESH</sub>	-0.3V to V <sub>S</sub> + 0.3V
Output Voltages, V <sub>O</sub> , V <sub>DIS</sub>	15V
Output Current I <sub>O</sub> , I <sub>DIS</sub>	100 mA
Storage Temperature Range	-65°C to +150°C
Soldering specification for PDIP package:	
Soldering (10 seconds)	260°C
Soldering specification for all other packages: see product folder at <a href="http://www.ti.com">www.ti.com</a> and <a href="http://www.ti.com/lit/SNOA549">http://www.ti.com/lit/SNOA549</a>	

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (2) See AN-1112 ([SNVA009](#)) for DSBGA considerations.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

**Operating Ratings<sup>(1)(2)</sup>**

Temperature Range	
LMC555IM	-40°C to +125°C
LMC555CM/MM/N/TP	-40°C to +85°C
Thermal Resistance (θ <sub>JA</sub> ) <sup>(1)</sup>	
SOIC, 8-Pin	169°C/W
VSSOP, 8-Pin	225°C/W
PDIP, 8-Pin	111°C/W
8-Bump DSBGA	220°C/W
Maximum Allowable Power Dissipation @25°C	
PDIP-8	1126 mW
SOIC-8	740 mW
VSSOP-8	555 mW
8-Bump DSBGA	568 mW

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- (2) See AN-1112 ([SNVA009](#)) for DSBGA considerations.

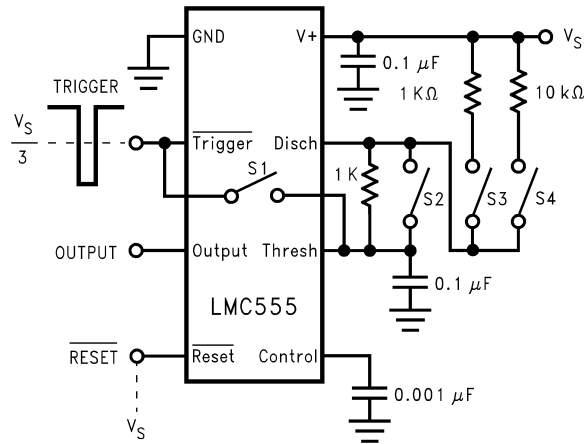
**Electrical Characteristics**<sup>(1) (2)</sup>Test Circuit, T = 25°C, all switches open,  $\overline{\text{RESET}}$  to  $V_S$  unless otherwise noted

Parameter		Test Conditions	Min	Typ	Max	Units (Limits)
$I_S$	Supply Current	$V_S = 1.5V$ $V_S = 5V$ $V_S = 12V$		50 100 150	150 250 400	$\mu A$
$V_{CTRL}$	Control Voltage	$V_S = 1.5V$ $V_S = 5V$ $V_S = 12V$	0.8 2.9 7.4	1.0 3.3 8.0	1.2 3.8 8.6	V
$V_{DIS}$	Discharge Saturation Voltage	$V_S = 1.5V, I_{DIS} = 1 \text{ mA}$ $V_S = 5V, I_{DIS} = 10 \text{ mA}$		75 150	150 300	mV
$V_{OL}$	Output Voltage (Low)	$V_S = 1.5V, I_O = 1 \text{ mA}$ $V_S = 5V, I_O = 8 \text{ mA}$ $V_S = 12V, I_O = 50 \text{ mA}$		0.2 0.3 1.0	0.4 0.6 2.0	V
$V_{OH}$	Output Voltage (High)	$V_S = 1.5V, I_O = -0.25 \text{ mA}$ $V_S = 5V, I_O = -2 \text{ mA}$ $V_S = 12V, I_O = -10 \text{ mA}$	1.0 4.4 10.5	1.25 4.7 11.3		V
$V_{TRIG}$	Trigger Voltage	$V_S = 1.5V$ $V_S = 12V$	0.4 3.7	0.5 4.0	0.6 4.3	V
$I_{TRIG}$	Trigger Current	$V_S = 5V$		10		pA
$V_{RES}$	Reset Voltage	$V_S = 1.5V$ <sup>(3)</sup> $V_S = 12V$	0.4 0.4	0.7 0.75	1.0 1.1	V
$I_{RES}$	Reset Current	$V_S = 5V$		10		pA
$I_{THRESH}$	Threshold Current	$V_S = 5V$		10		pA
$I_{DIS}$	Discharge Leakage	$V_S = 12V$		1.0	100	nA
t	Timing Accuracy	SW 2, 4 Closed $V_S = 1.5V$ $V_S = 5V$ $V_S = 12V$	0.9 1.0 1.0	1.1 1.1 1.1	1.25 1.20 1.25	ms
$\Delta t/\Delta V_S$	Timing Shift with Supply	$V_S = 5V \pm 1V$		0.3		%/V
$\Delta t/\Delta T$	Timing Shift with Temperature	$V_S = 5V$		75		ppm/°C
$f_A$	Astable Frequency	SW 1, 3 Closed, $V_S = 12V$	4.0	4.8	5.6	kHz
$f_{MAX}$	Maximum Frequency	Max. Freq. Test Circuit, $V_S = 5V$		3.0		MHz
$t_R, t_F$	Output Rise and Fall Times	Max. Freq. Test Circuit $V_S = 5V, C_L = 10 \text{ pF}$		15		ns
$t_{PD}$	Trigger Propagation Delay	$V_S = 5V$ , Measure Delay from Trigger to Output		100		ns

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.

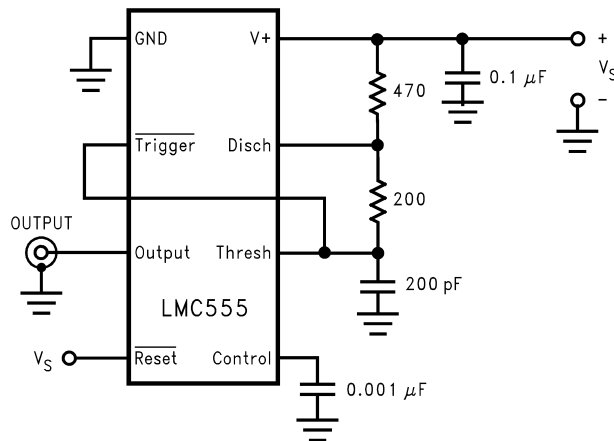
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

(3) If the  $\overline{\text{RESET}}$  pin is to be used at temperatures of  $-20^\circ\text{C}$  and below  $V_S$  is required to be 2.0V or greater.



For device pinout, please see [Table 1](#).

**Figure 3. Test Circuit**



For device pinout, please see [Table 1](#).

**Figure 4. Maximum Frequency Test Circuit**

APPLICATION INFORMATION

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (Figure 5). The external capacitor is initially held discharged by internal circuitry. Upon application of a negative trigger pulse of less than  $1/3 V_S$  to the Trigger terminal, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

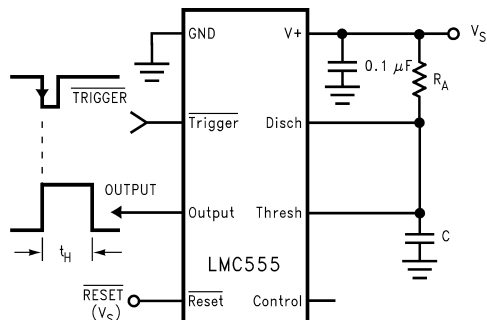
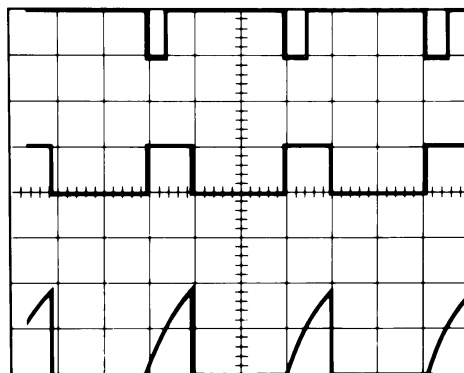


Figure 5. Monostable (One-Shot)

The voltage across the capacitor then increases exponentially for a period of  $t_H = 1.1 R_A C$ , which is also the time that the output stays high, at the end of which time the voltage equals  $2/3 V_S$ . The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 6 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



$V_{CC} = 5V$   
 TIME = 0.1 ms/Div.  
 $R_A = 9.1 k\Omega$   
 $C = 0.01 \mu F$

Top Trace: Input 5 V/Div.  
 Middle Trace: Output 5 V/Div.  
 Bottom Trace: Capacitor Voltage 2 V/Div.

Figure 6. Monostable Waveforms

Reset overrides Trigger, which can override threshold. Therefore the trigger pulse must be shorter than the desired  $t_H$ . The minimum pulse width for the Trigger is 20ns, and it is 400ns for the Reset. During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal. The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not use, it is recommended that it be connected to  $V_+$  to avoid any possibility of false triggering. Figure 7 is a nomograph for easy determination of RC values for various time delays.

NOTE

In monostable operation, the trigger should be driven high before the end of timing cycle.

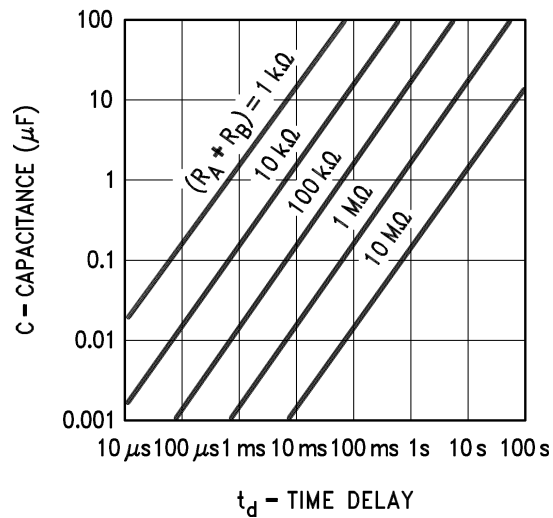


Figure 7. Time Delay

### ASTABLE OPERATION

If the circuit is connected as shown in Figure 8 (Trigger and Threshold terminals connected together) it will trigger itself and free run as a multivibrator. The external capacitor charges through R<sub>A</sub> + R<sub>B</sub> and discharges through R<sub>B</sub>. Thus the duty cycle may be precisely set by the ratio of these two resistors.

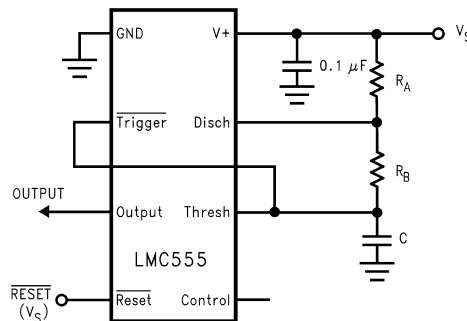
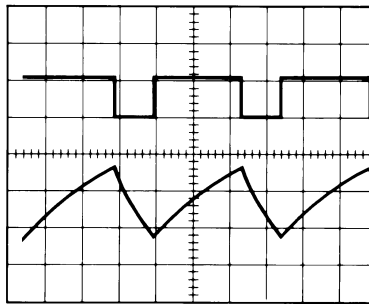


Figure 8. Astable (Variable Duty Cycle Oscillator)

In this mode of operation, the capacitor charges and discharges between 1/3 V<sub>S</sub> and 2/3 V<sub>S</sub>. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 9 shows the waveform generated in this mode of operation.



$V_{CC} = 5V$   
 $TIME = 20 \mu s/Div.$   
 $R_A = 3.9 k\Omega$   
 $R_B = 9 k\Omega$   
 $C = 0.01 \mu F$

Top Trace: Output 5 V/Div.  
 Bottom Trace: Capacitor Voltage 1 V/Div.

**Figure 9. Astable Waveforms**

The charge time (output high) is given by

$$t_1 = 0.693 (R_A + R_B)C \tag{1}$$

And the discharge time (output low) by:

$$t_2 = 0.693 (R_B)C \tag{2}$$

Thus the total period is:

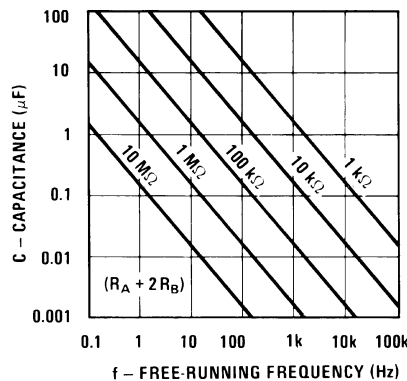
$$T = t_1 + t_2 = 0.693 (R_A + 2R_B)C \tag{3}$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C} \tag{4}$$

Figure 10 may be used for quick determination of these RC Values. The duty cycle, as a fraction of total period that the output is low, is:

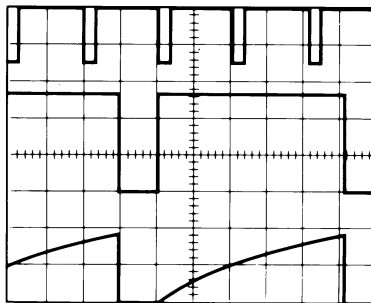
$$D = \frac{R_B}{R_A + 2R_B} \tag{5}$$



**Figure 10. Free Running Frequency**

### FREQUENCY DIVIDER

The monostable circuit of Figure 5 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 11 shows the waveforms generated in a divide by three circuit.



$V_{CC} = 5V$       Top Trace: Input 4 V/Div.  
 TIME = 20  $\mu s$ /Div.    Middle Trace: Output 2 V/Div.  
 $R_A = 9.1 k\Omega$       Bottom Trace: Capacitor 2 V/Div.  
 $C = 0.01 \mu F$

Figure 11. Frequency Divider Waveforms

### PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to the Control Voltage Terminal. Figure 12 shows the circuit, and in Figure 13 are some waveform examples.

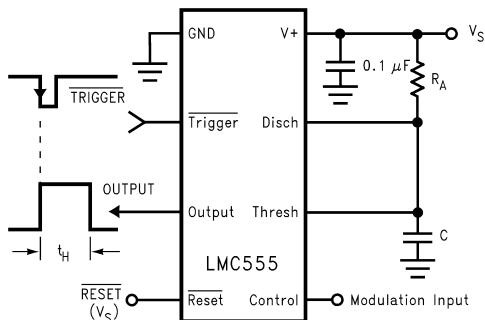
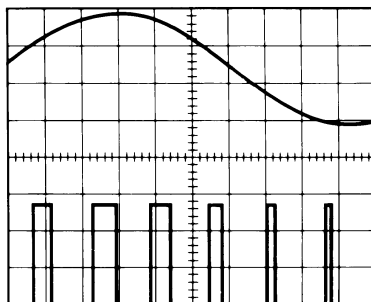


Figure 12. Pulse Width Modulator



$V_{CC} = 5V$       Top Trace: Modulation 1 V/Div.  
 TIME = 0.2 ms/Div.    Bottom Trace: Output Voltage 2 V/Div.  
 $R_A = 9.1 k\Omega$   
 $C = 0.01 \mu F$

Figure 13. Pulse Width Modulator Waveforms

### PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in Figure 14, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 15 shows the waveforms generated for a triangle wave modulation signal.

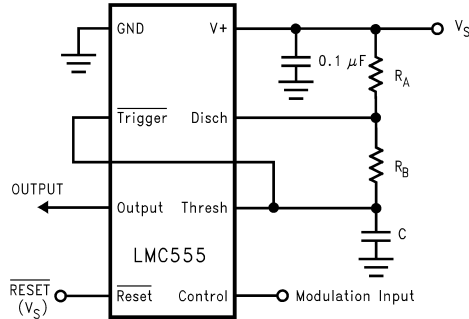
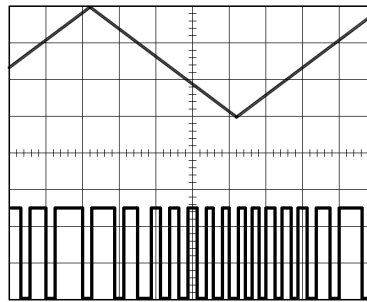


Figure 14. Pulse Position Modulator



V<sub>CC</sub> = 5V  
 TIME = 0.1 ms/Div.  
 R<sub>A</sub> = 3.9 kΩ  
 R<sub>B</sub> = 3 kΩ  
 C = 0.01 μF

Top Trace: Modulation Input 1 V/Div.  
 Bottom Trace: Output Voltage 2 V/Div.

Figure 15. Pulse Position Modulator Waveforms

### 50% DUTY CYCLE OSCILLATOR

The frequency of oscillation is

$$f = 1/(1.4 R_C C)$$

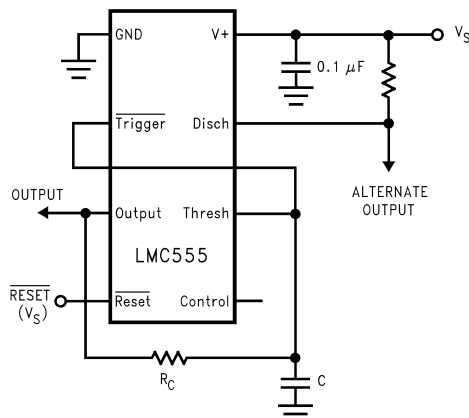


Figure 16. 50% Duty Cycle Oscillator



## REVISION HISTORY

Changes from Revision I (March 2013) to Revision J	Page
• Changed layout of National Data Sheet to TI format .....	10

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMC555CM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMC 555CM	<a href="#">Samples</a>
LMC555CM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC 555CM	<a href="#">Samples</a>
LMC555CMM	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	ZC5	<a href="#">Samples</a>
LMC555CMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	ZC5	<a href="#">Samples</a>
LMC555CMMX	ACTIVE	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 85	ZC5	<a href="#">Samples</a>
LMC555CMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	ZC5	<a href="#">Samples</a>
LMC555CMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMC 555CM	<a href="#">Samples</a>
LMC555CMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC 555CM	<a href="#">Samples</a>
LMC555CN	ACTIVE	PDIP	P	8	40	TBD	Call TI	Call TI	-40 to 85	LMC 555CN	<a href="#">Samples</a>
LMC555CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-40 to 85	LMC 555CN	<a href="#">Samples</a>
LMC555CTP/NOPB	ACTIVE	DSBGA	YPB	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F 02	<a href="#">Samples</a>
LMC555CTPX/NOPB	ACTIVE	DSBGA	YPB	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F 02	<a href="#">Samples</a>
LMC555IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC 555IM	<a href="#">Samples</a>
LMC555IMX/NOPB	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMC 555IM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

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(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC555CMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC555CMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC555CMMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC555CMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC555CMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC555CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC555CTP/NOPB	DSBGA	YPB	8	250	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LMC555CTPX/NOPB	DSBGA	YPB	8	3000	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1

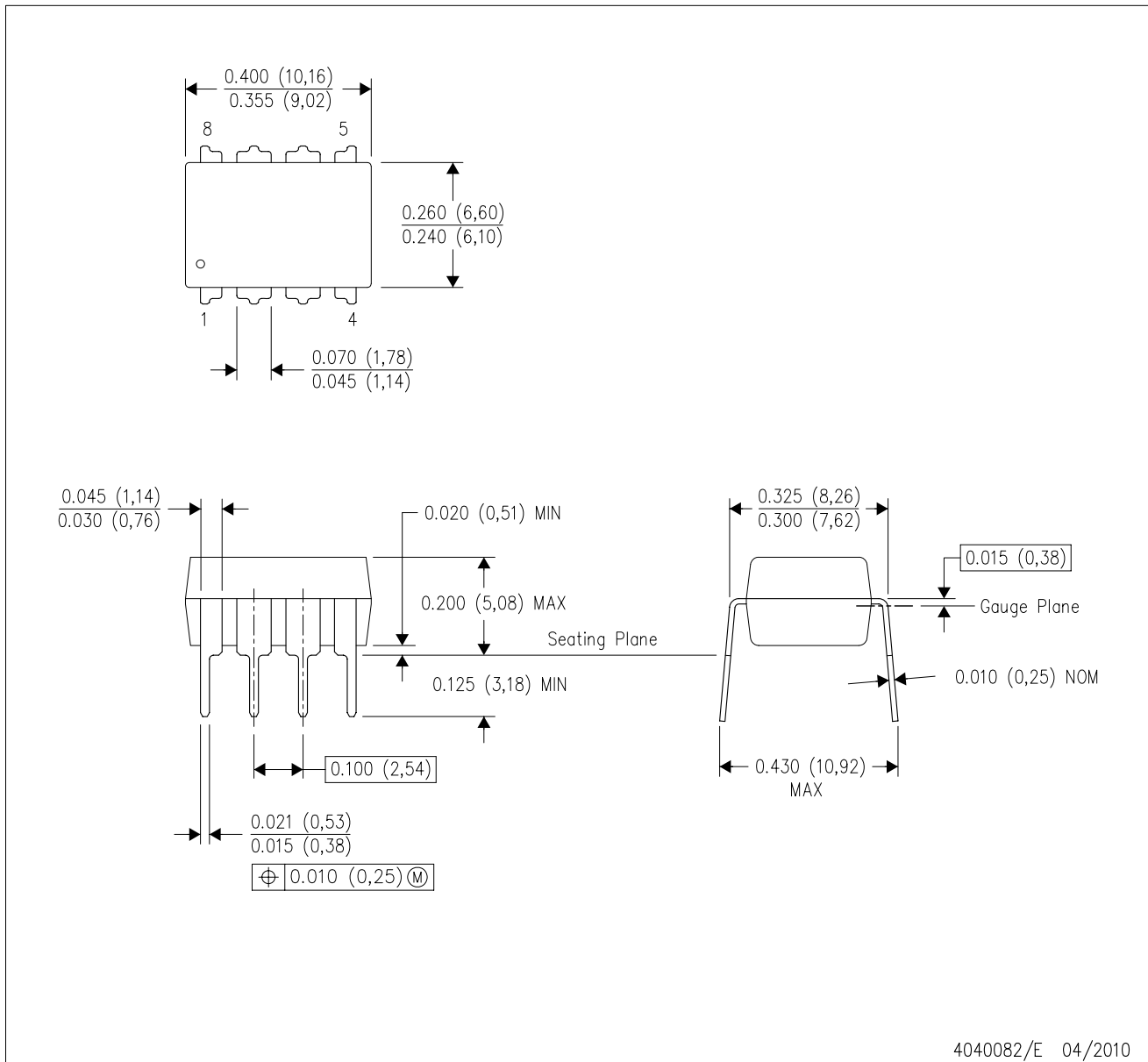
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC555CMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC555CMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC555CMMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC555CMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC555CMX	SOIC	D	8	2500	367.0	367.0	35.0
LMC555CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC555CTP/NOPB	DSBGA	YPB	8	250	210.0	185.0	35.0
LMC555CTPX/NOPB	DSBGA	YPB	8	3000	210.0	185.0	35.0

P (R-PDIP-T8)

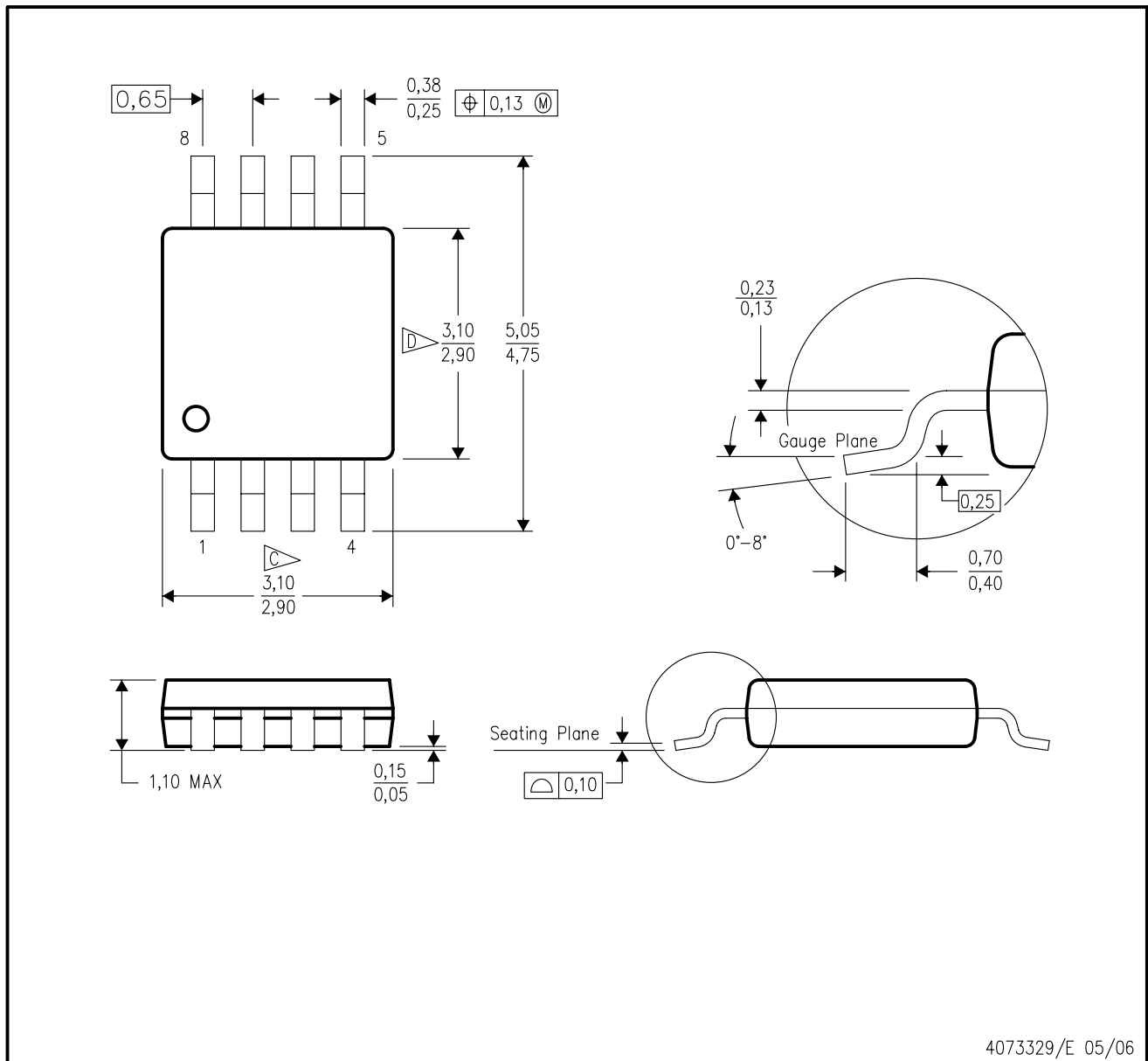
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

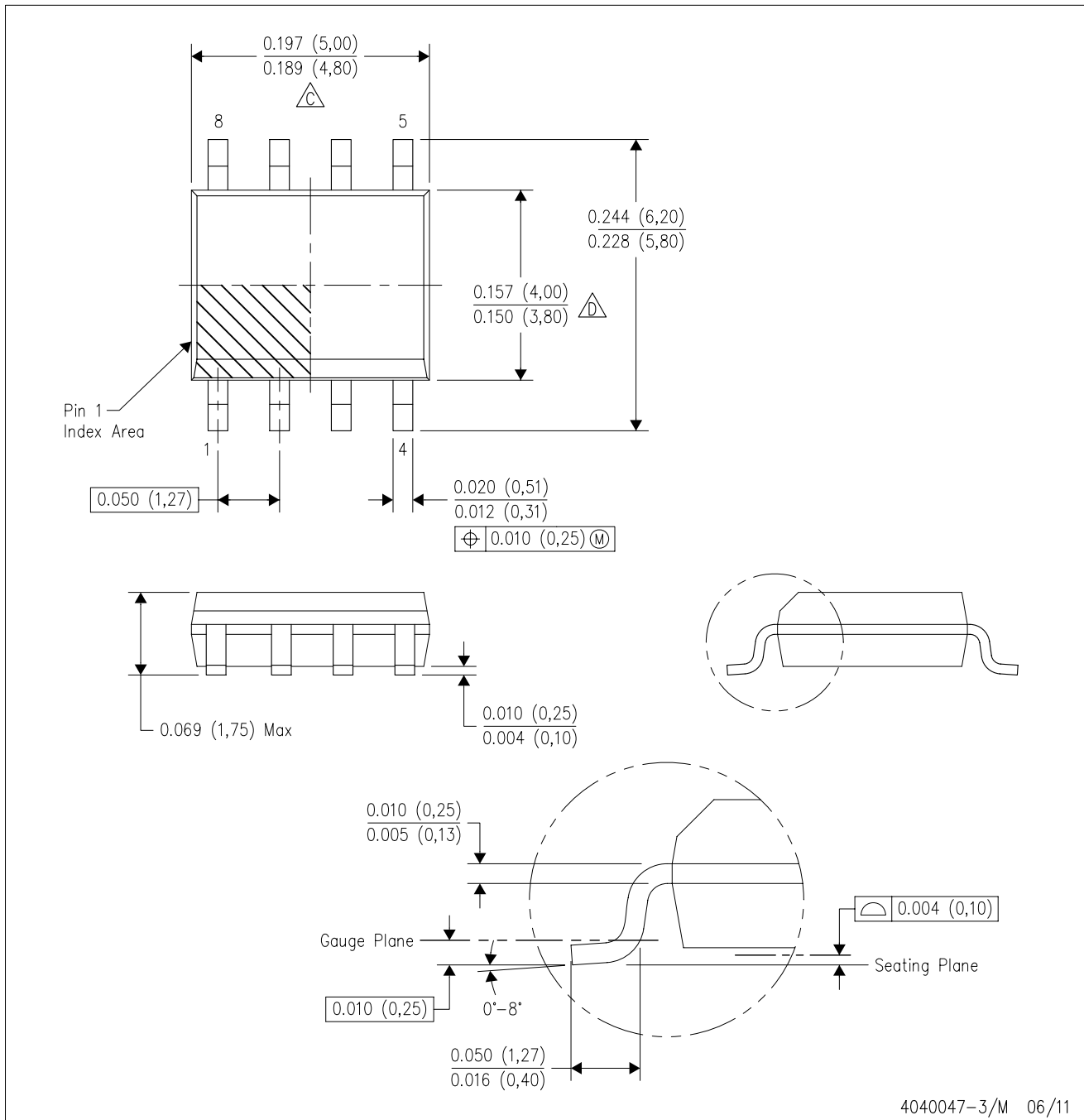


4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

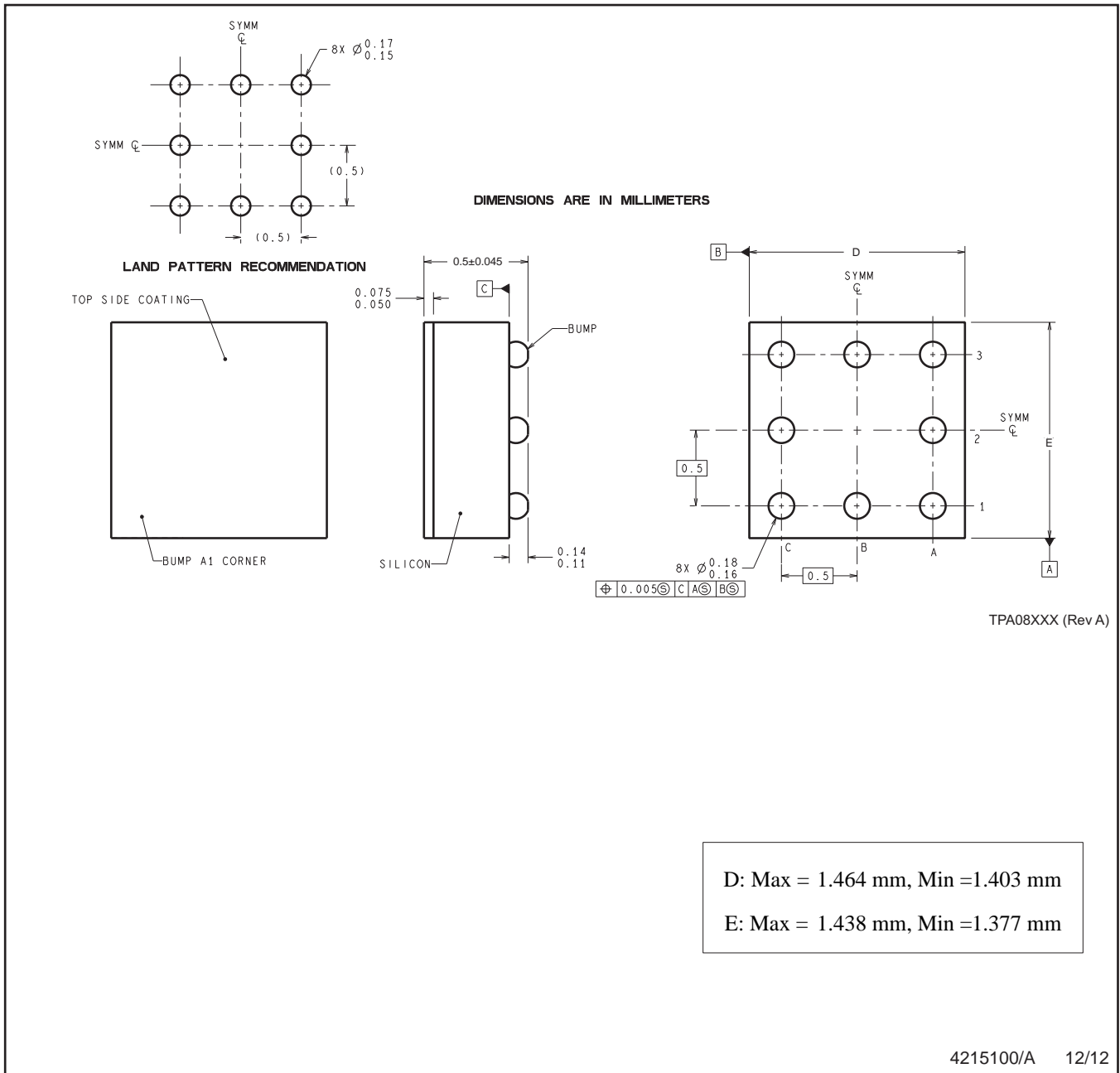
D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

YPB0008



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
 B. This drawing is subject to change without notice.

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