

LMC6082 Precision CMOS Dual Operational Amplifier

Check for Samples: [LMC6082](#)

FEATURES

- (Typical Unless Otherwise Stated)
- **Low Offset Voltage:** 150 μ V
- **Operates from 4.5V to 15V Single Supply**
- **Ultra Low Input Bias Current:** 10 fA
- **Output Swing to Within 20 mV of Supply Rail, 100k Load**
- **Input Common-Mode Range Includes V^-**
- **High Voltage Gain:** 130 dB
- **Improved Latchup Immunity**

APPLICATIONS

- Instrumentation Amplifier
- Photodiode and Infrared Detector Preamplifier
- Transducer Amplifiers
- Medical Instrumentation
- D/A Converter
- Charge Amplifier for Piezoelectric Transducers

Connection Diagram

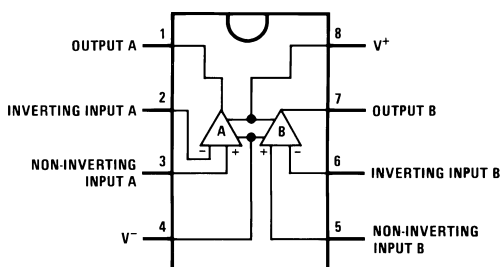


Figure 1. 8-Pin PDIP/SOIC Top View

DESCRIPTION

The LMC6082 is a precision dual low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6082 ideally suited for precision circuit applications.

Other applications using the LMC6082 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with TI's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6062 precision dual micropower operational amplifier.

PATENT PENDING

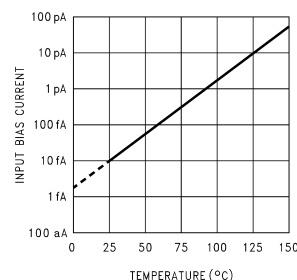


Figure 2. Input Bias Current vs Temperature



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

| | |
|---|---|
| Differential Input Voltage | ±Supply Voltage |
| Voltage at Input/Output Pin | (V ⁺) +0.3V, (V ⁻) -0.3V |
| Supply Voltage (V ⁺ - V ⁻) | 16V |
| Output Short Circuit to V ⁺ | See ⁽³⁾ |
| Output Short Circuit to V ⁻ | See ⁽⁴⁾ |
| Lead Temperature (Soldering, 10 Sec.) | 260°C |
| Storage Temp. Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| ESD Tolerance ⁽⁵⁾ | 2 kV |
| Current at Input Pin | ±10 mA |
| Current at Output Pin | ±30 mA |
| Current at Power Supply Pin | 40 mA |
| Power Dissipation | See ⁽⁶⁾ |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Do not connect output to V⁺, when V⁺ is greater than 13V or reliability will be adversely affected.
- (4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
- (5) Human body model, 1.5 kΩ in series with 100 pF.
- (6) The maximum power dissipation is a function of T_{J(Max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(Max)} - T_A) / θ_{JA}.

Operating Ratings ⁽¹⁾

| | | |
|--|---------------------|---------------------------------|
| Temperature Range | LMC6082AM | -55°C ≤ T _J ≤ +125°C |
| | LMC6082AI, LMC6082I | -40°C ≤ T _J ≤ +85°C |
| Supply Voltage | | 4.5V ≤ V ⁺ ≤ 15.5V |
| Thermal Resistance (θ _{JA}) ⁽²⁾ | 8-Pin PDIP | 115°C/W |
| | 8-Pin SOIC | 193°C/W |
| Power Dissipation | | See ⁽³⁾ |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
- (2) All numbers apply for packages soldered directly into a PC board.
- (3) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with P_D = (T_J - T_A) / θ_{JA}. All numbers apply for packages soldered directly into a PC board.

DC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_j = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ ⁽¹⁾ | LMC6082AM Limit ⁽²⁾ | LMC6082AI Limit ⁽²⁾ | LMC6082I Limit ⁽²⁾ | Units | |
|--------------------------|--|---|--------------------|--|--|--|------------------------------|-------------|
| V_{OS} | Input Offset Voltage | | 150 | 350 1000 | 350 800 | 800 1300 | μV Max | |
| TCV_{OS} | Input Offset Voltage Average Drift | | 1.0 | | | | $\mu\text{V}/^\circ\text{C}$ | |
| I_B | Input Bias Current | | 0.010 | 100 | 4 | 4 | pA Max | |
| I_{OS} | Input Offset Current | | 0.005 | 100 | 2 | 2 | pA Max | |
| R_{IN} | Input Resistance | | >10 | | | | Tera Ω | |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{\text{CM}} \leq 12.0\text{V}$ $V^+ = 15\text{V}$ | 85 | 75 72 | 75 72 | 66 63 | dB Min | |
| +PSRR | Positive Power Supply Rejection Ratio | $5\text{V} \leq V^+ \leq 15\text{V}$ $V_O = 2.5\text{V}$ | 85 | 75 72 | 75 72 | 66 63 | dB Min | |
| -PSRR | Negative Power Supply Rejection Ratio | $0\text{V} \leq V^- \leq -10\text{V}$ | 94 | 84 81 | 84 81 | 74 71 | dB Min | |
| V_{CM} | Input Common-Mode Voltage Range | $V^+ = 5\text{V}$ and 15V for $\text{CMRR} \geq 60\text{ dB}$ | -0.4 | -0.1 0 | -0.1 0 | -0.1 0 | V Max | |
| | | | $V^+ - 1.9$ | $V^+ - 2.3$ $V^+ - 2.6$ | $V^+ - 2.3$ $V^+ - 2.5$ | $V^+ - 2.3$ $V^+ - 2.5$ | V Min | |
| A_V | Large Signal Voltage Gain | $R_L = 2\text{ k}\Omega$ ⁽³⁾ | Sourcing | 1400 300 | 400 300 | 400 200 | V/mV Min | |
| | | | Sinking | 350 70 | 180 100 | 90 60 | V/mV Min | |
| | | $R_L = 600\Omega$ ⁽³⁾ | Sourcing | 1200 150 | 400 150 | 400 80 | 200 Min | V/mV Min |
| | | | Sinking | 150 35 | 100 50 | 100 35 | 70 Min | V/mV Min |

(1) Typical values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3) $V^+ = 15\text{V}$, $V_{\text{CM}} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

DC Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ ⁽¹⁾ | LMC6082AM Limit ⁽²⁾ | LMC6082AI Limit ⁽²⁾ | LMC6082I Limit ⁽²⁾ | Units | | |
|--------|----------------|--|---|-----------------------------------|-----------------------------------|----------------------------------|-----------------------|-----------------|-----------|
| V_O | Output Swing | $V^+ = 5\text{V}$ $R_L = 2\text{ k}\Omega$ to 2.5V | 4.87 | 4.80 4.70 | 4.80 4.73 | 4.75 4.67 | V Min | | |
| | | | 0.10 | 0.13 0.19 | 0.13 0.17 | 0.20 0.24 | V Max | | |
| | | | $V^+ = 5\text{V}$ $R_L = 600\Omega$ to 2.5V | 4.61 | 4.50 4.24 | 4.50 4.31 | 4.40 4.21 | V Min | |
| | | | | 0.30 | 0.40 0.63 | 0.40 0.50 | 0.50 0.63 | V Max | |
| | | | $V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$ to 7.5V | 14.63 | 14.50 14.30 | 14.50 14.34 | 14.37 14.25 | V Min | |
| | | | | 0.26 | 0.35 0.48 | 0.35 0.45 | 0.44 0.56 | V Max | |
| | | $V^+ = 15\text{V}$ $R_L = 600\Omega$ to 7.5V | 13.90 | 13.35 12.80 | 13.35 12.86 | 12.92 12.44 | V Min | | |
| | | | 0.79 | 1.16 1.42 | 1.16 1.32 | 1.33 1.58 | V Max | | |
| | | I_O | Output Current $V^+ = 5\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 22 | 16 8 | 16 10 | 13 8 | mA Min |
| | | | | | 21 | 16 11 | 16 13 | 13 10 | mA Min |
| | | | | Sinking, $V_O = 5\text{V}$ | 30 | 28 18 | 28 22 | 23 18 | mA Min |
| | | | | | 34 | 28 19 | 28 22 | 23 18 | mA Min |
| I_S | Supply Current | Both Amplifiers $V^+ = +5\text{V}$, $V_O = 1.5\text{V}$ | 0.9 | 1.5 1.8 | 1.5 1.8 | 1.5 1.8 | mA Max | | |
| | | | 1.1 | 1.7 2 | 1.7 2 | 1.7 2 | mA Max | | |
| | | Both Amplifiers $V^+ = +15\text{V}$, $V_O = 7.5\text{V}$ | 0.9 | 1.5 1.8 | 1.5 1.8 | 1.5 1.8 | mA Max | | |
| | | | 1.1 | 1.7 2 | 1.7 2 | 1.7 2 | mA Max | | |

(4) Do not connect output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

AC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$, **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ ⁽¹⁾ | LMC6082AM Limit ⁽²⁾ | LMC6082AI Limit ⁽²⁾ | LMC6082I Limit ⁽²⁾ | Units |
|----------|------------------------------|--------------------|--------------------|-----------------------------------|-----------------------------------|----------------------------------|------------------------------|
| SR | Slew Rate | See ⁽³⁾ | 1.5 | 0.8 0.5 | 0.8 0.6 | 0.8 0.6 | V/ μs Min |
| | | | GBW | Gain-Bandwidth Product | 1.3 | | |
| ϕ_m | Phase Margin | | 50 | | | | Deg |
| | Amp-to-Amp Isolation | See ⁽⁴⁾ | 140 | | | | dB |
| e_n | Input-Referred Voltage Noise | $F = 1\text{ kHz}$ | 22 | | | | $\text{nV}/\sqrt{\text{Hz}}$ |

(1) Typical values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3) $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

(4) Input referred $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 7.5V . Each amp excited in turn with 1 kHz to produce $V_O = 12\text{ V}_{PP}$.

AC Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$, **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ ⁽¹⁾ | LMC6082AM Limit⁽²⁾ | LMC6082AI Limit⁽²⁾ | LMC6082I Limit⁽²⁾ | Units |
|--------|------------------------------|---|--------------------|--|--|---|------------------------------|
| i_n | Input-Referred Current Noise | $F = 1\text{ kHz}$ | 0.0002 | | | | $\text{pA}/\sqrt{\text{Hz}}$ |
| T.H.D. | Total Harmonic Distortion | $F = 10\text{ kHz}$, $A_V = -10$ $R_L = 2\text{ k}\Omega$, $V_O = 8\text{ V}_{PP}$ $\pm 5\text{V}$ Supply | 0.01 | | | | % |

Typical Performance Characteristics

$V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified

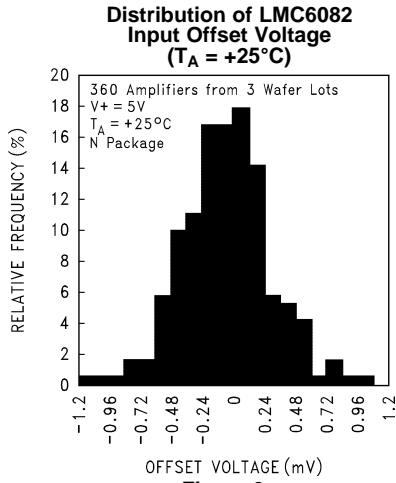


Figure 3.

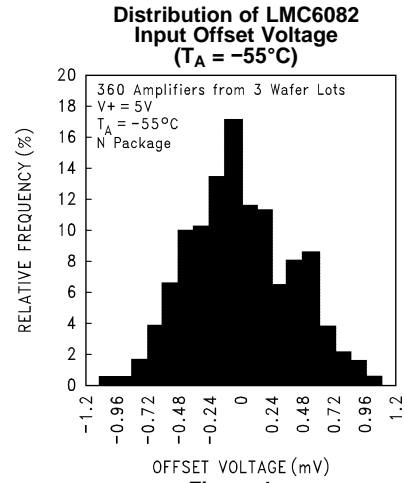


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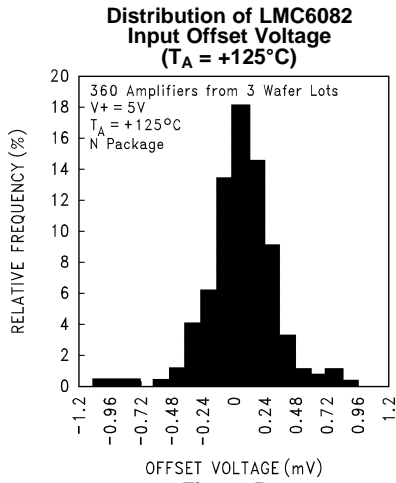


Figure 5.

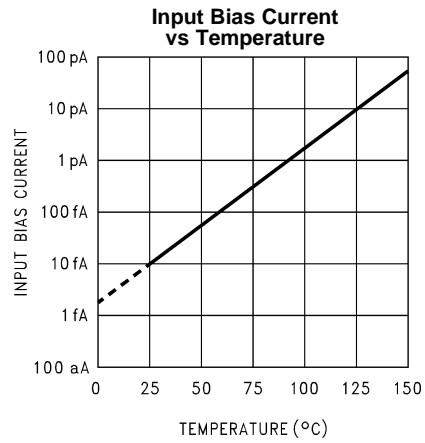


Figure 6.

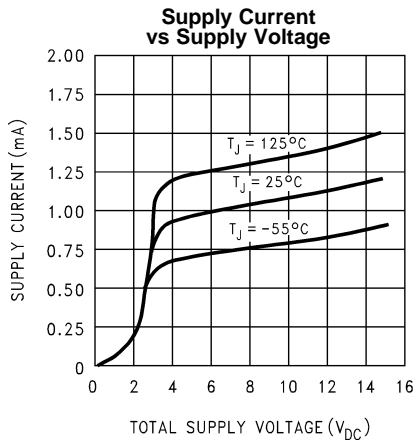


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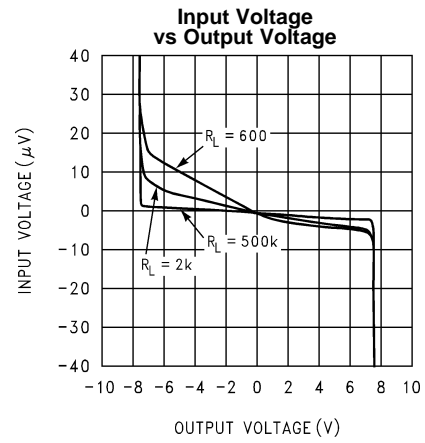


Figure 8.

Typical Performance Characteristics (continued)

$V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified

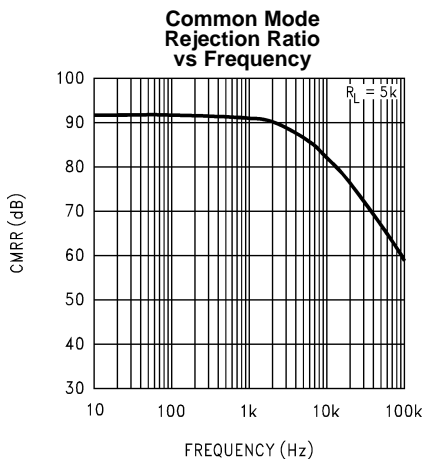


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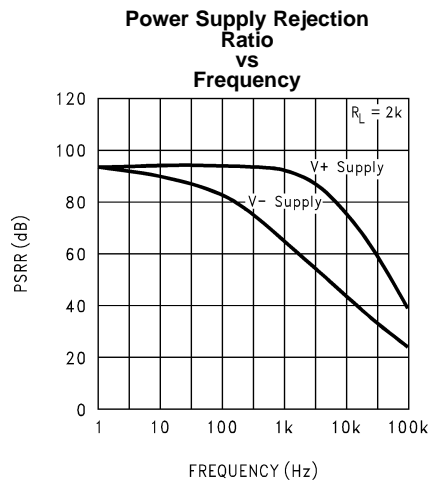


Figure 10.

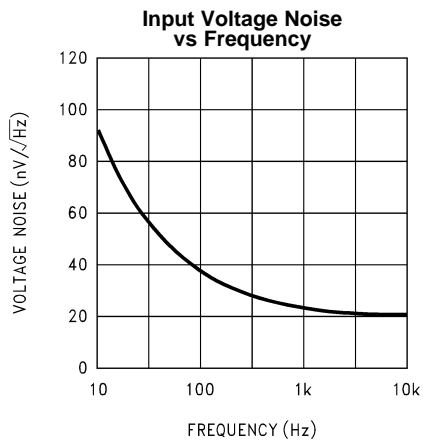


Figure 11.

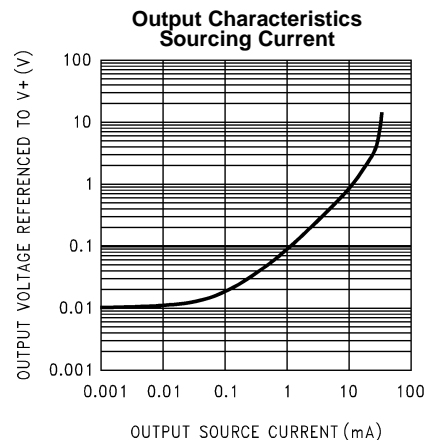


Figure 12.

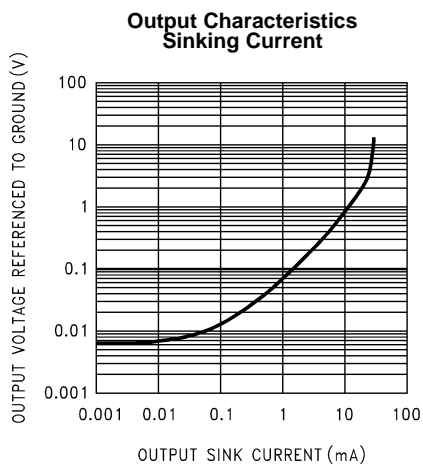


Figure 13.

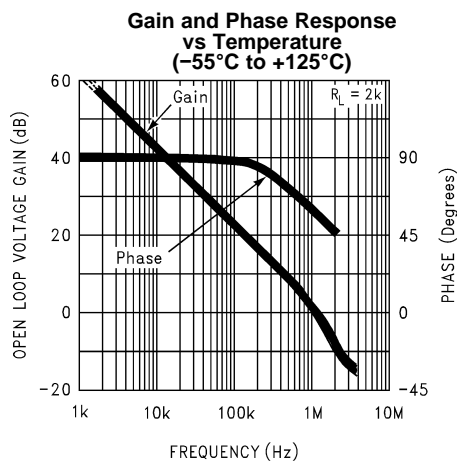
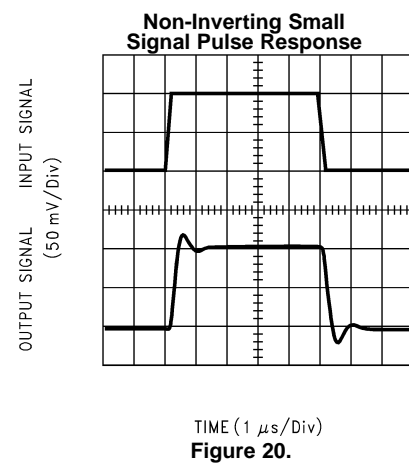
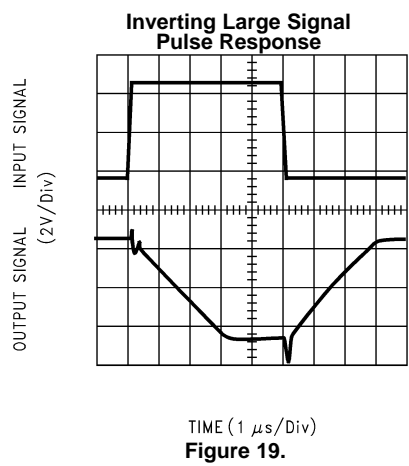
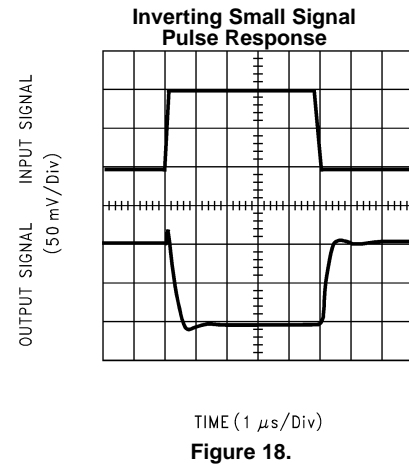
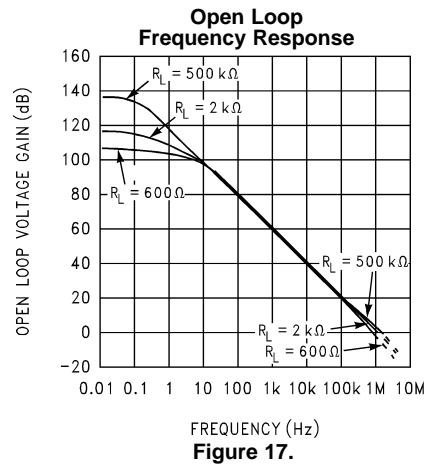
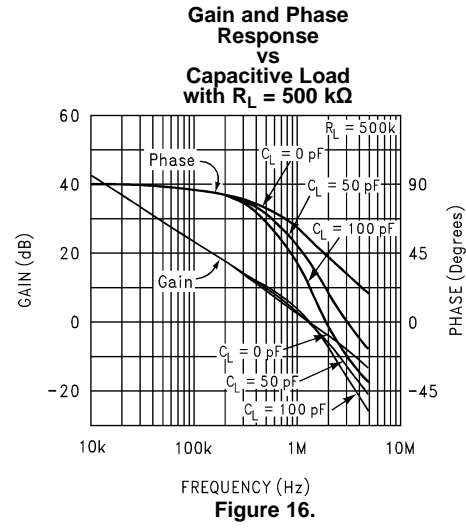
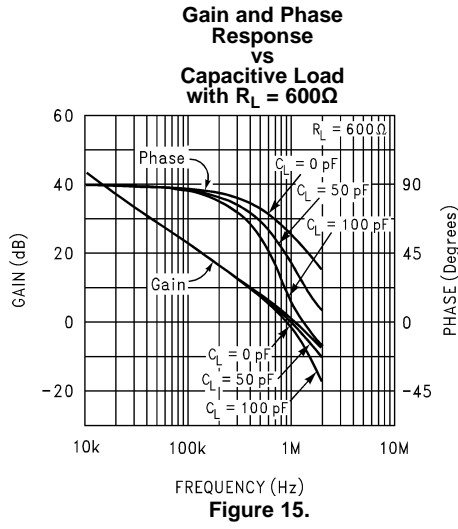


Figure 14.

Typical Performance Characteristics (continued)

$V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified



Typical Performance Characteristics (continued)

$V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified

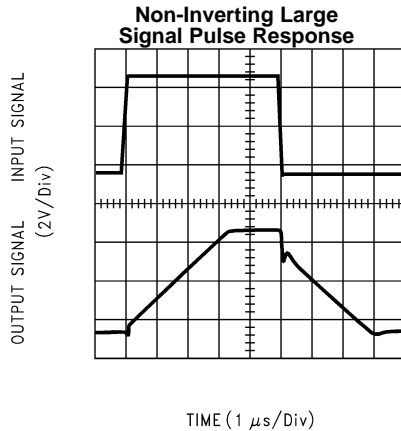


Figure 21.

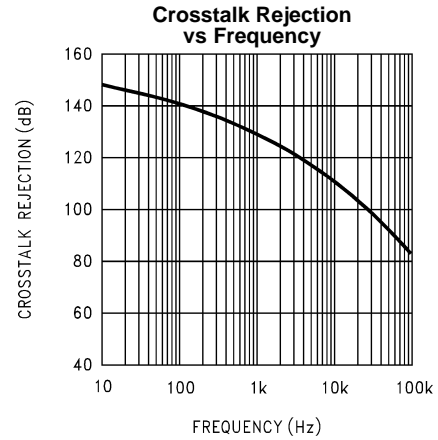


Figure 22.

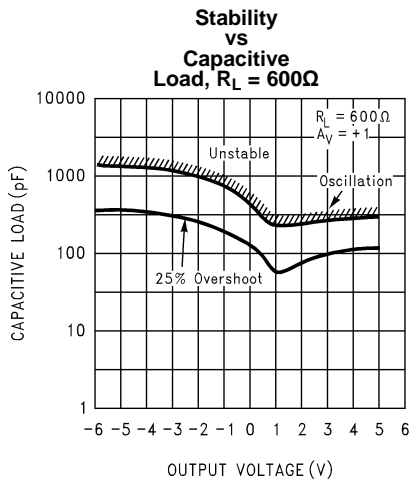


Figure 23.

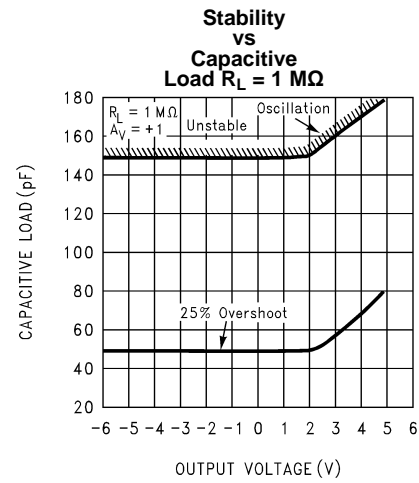


Figure 24.

APPLICATIONS HINTS

AMPLIFIER TOPOLOGY

The LMC6082 incorporates a novel op-amp design topology that enables it to maintain rail to rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6082 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6082.

Although the LMC6082 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6082 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See [Printed-Circuit-Board Layout for High Impedance Work](#))

The effect of input capacitance can be compensated for by adding a capacitor, C_f , around the feedback resistors (as in [Figure 25](#)) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_f \quad (2)$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

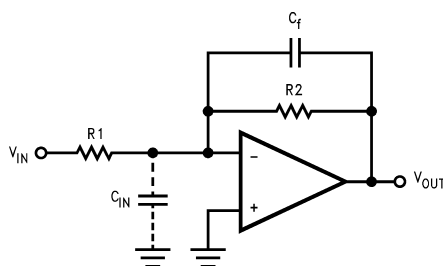


Figure 25. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see [typical curves](#)).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in [Figure 26](#).

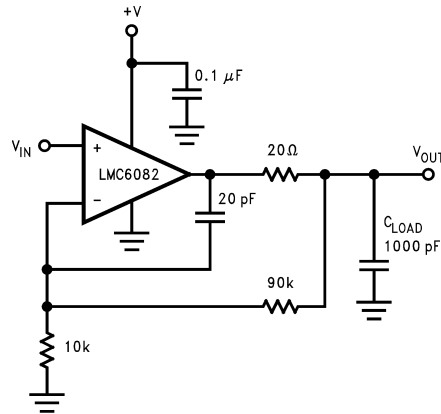


Figure 26. LMC6082 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of [Figure 26](#), R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V⁺ [Figure 27](#). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see [Electrical Characteristics](#)).

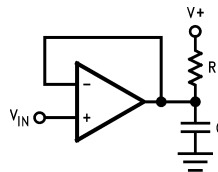


Figure 27. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6082, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6082's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in [Figure 28](#). To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6082's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See [Figure 29](#) for typical connections of guard rings for standard op-amp configurations.

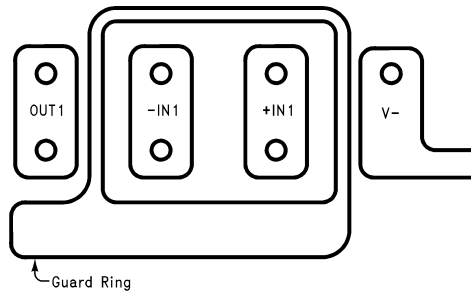


Figure 28. Example of Guard Ring in P.C. Board Layout

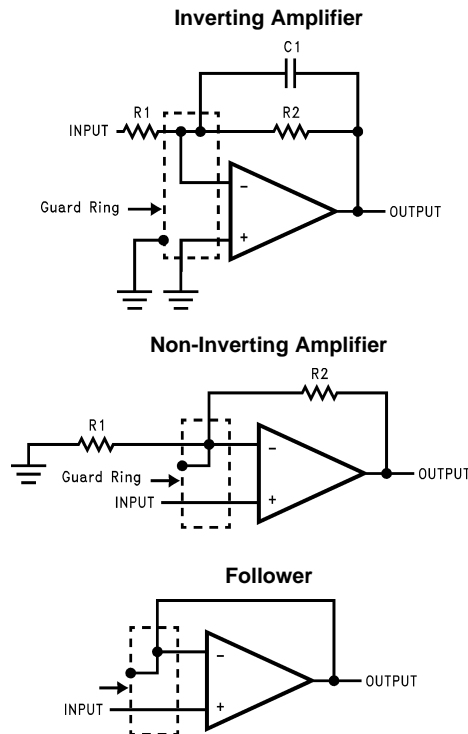
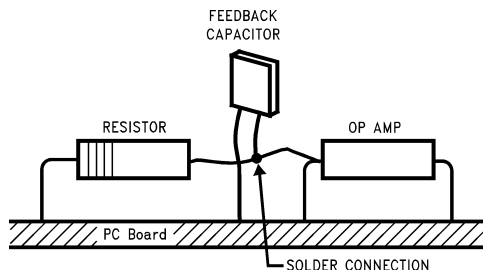


Figure 29. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See [Figure 30](#).

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6062 and LMC6082 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

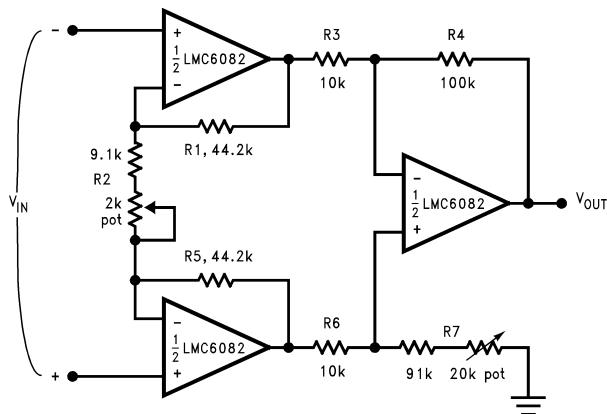
Figure 30. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0 V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6082 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 31 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 1000$, excellent CMRR with 1 k Ω imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 $\mu V/^\circ C$. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3} \quad \therefore A_V \approx 100 \text{ for circuit shown } (R_2 = 9.822k).$$

Figure 31. Instrumentation Amplifier

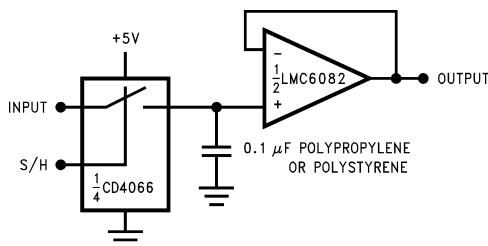


Figure 32. Low-Leakage Sample and Hold

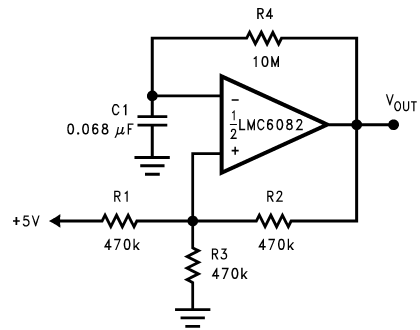


Figure 33. 1 Hz Square Wave Oscillator

REVISION HISTORY

| Changes from Revision C (March 2013) to Revision D | Page |
|--|--------------------------|
| <hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format | <hr/> 14 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| LMC6082AIM | ACTIVE | SOIC | D | 8 | 95 | TBD | Call TI | Call TI | -40 to 85 | LMC6082AIM | Samples |
| LMC6082AIM/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LMC6082AIM | Samples |
| LMC6082AIMX | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | -40 to 85 | LMC6082AIM | Samples |
| LMC6082AIMX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LMC6082AIM | Samples |
| LMC6082AIN | ACTIVE | PDIP | P | 8 | 40 | TBD | Call TI | Call TI | -40 to 85 | LMC6082AIN | Samples |
| LMC6082AIN/NOPB | ACTIVE | PDIP | P | 8 | 40 | Green (RoHS & no Sb/Br) | SN | Level-1-NA-UNLIM | -40 to 85 | LMC6082AIN | Samples |
| LMC6082IM | ACTIVE | SOIC | D | 8 | 95 | TBD | Call TI | Call TI | -40 to 85 | LMC6082IM | Samples |
| LMC6082IM/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LMC6082IM | Samples |
| LMC6082IMX | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | -40 to 85 | LMC6082IM | Samples |
| LMC6082IMX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LMC6082IM | Samples |
| LMC6082IN | ACTIVE | PDIP | P | 8 | 40 | TBD | Call TI | Call TI | -40 to 85 | LMC6082IN | Samples |
| LMC6082IN/NOPB | ACTIVE | PDIP | P | 8 | 40 | Green (RoHS & no Sb/Br) | SN | Level-1-NA-UNLIM | -40 to 85 | LMC6082IN | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMC6082AIMX | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMC6082AIMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMC6082IMX | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMC6082IMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |

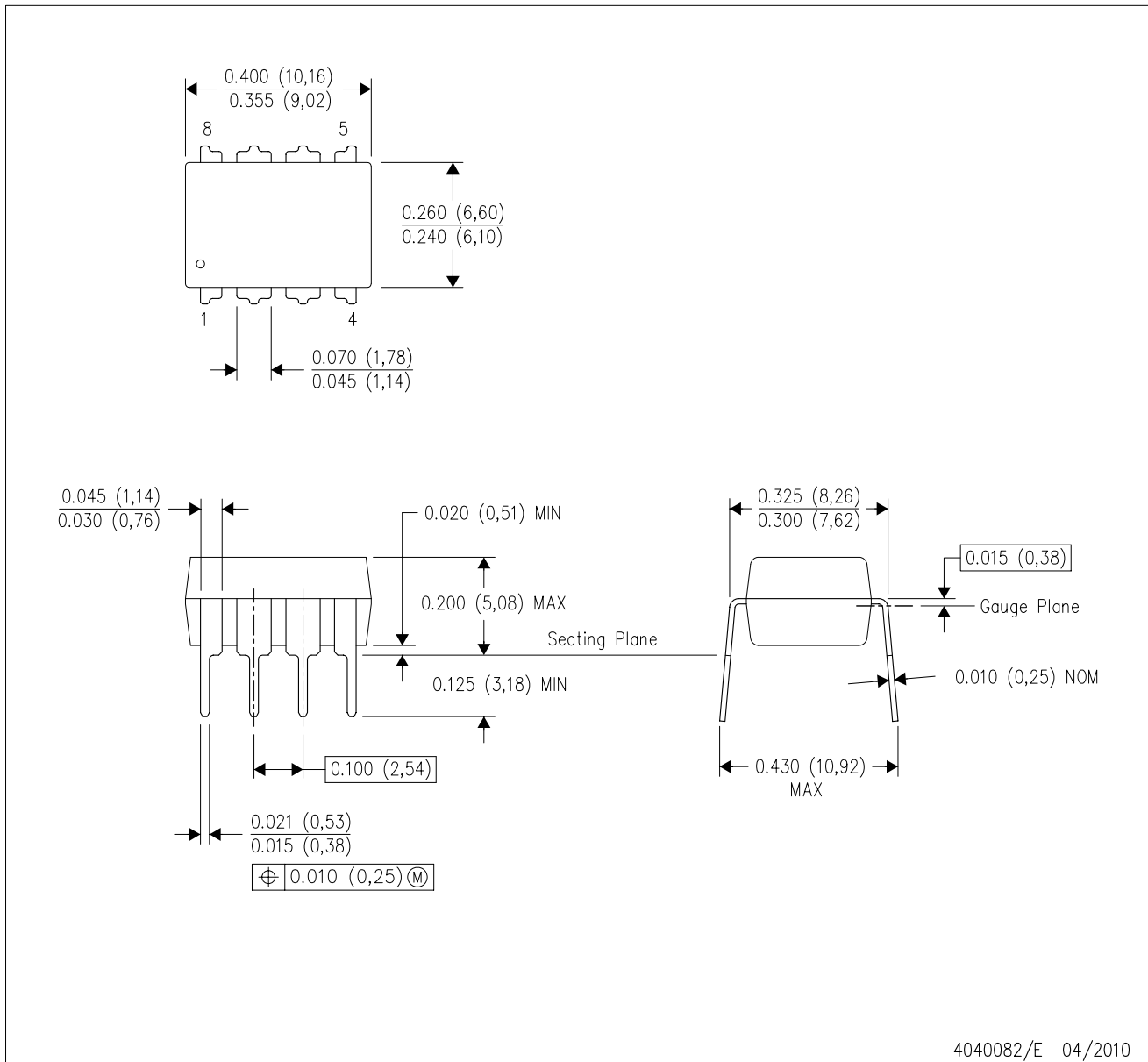
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMC6082AIMX | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMC6082AIMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMC6082IMX | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMC6082IMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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