LMC660 CMOS Quad Operational Amplifier

Check for Samples: LMC660

FEATURES

- **Rail-to-Rail Output Swing**
- **Specified for 2 kΩ and 600Ω Loads**
- **High Voltage Gain: 126 dB**
- **Low Input Offset Voltage: 3 mV**
- **Low Offset Voltage Drift: 1.3 μV/°C**
- **Ultra Low Input Bias Current: 2 fA**
- **Input Common-Mode Range Includes V^-**
- **Operating Range from +5V to +15.5V Supply**
- **I_{SS} = 375 μA/Amplifier; Independent of V^+**
- **Low Distortion: 0.01% at 10 kHz**
- **Slew Rate: 1.1 V/μs**

APPLICATIONS

- **High-Impedance Buffer or Preamplifier**
- **Precision Current-to-Voltage Converter**
- **Long-Term Integrator**
- **Sample-and-Hold Circuit**
- **Peak Detector**
- **Medical Instrumentation**
- **Industrial Controls**
- **Automotive Sensors**

DESCRIPTION

The LMC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It operates from +5V to +15.5V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with TI's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC662 datasheet for a dual CMOS operational amplifier with these same features.

Connection Diagrams

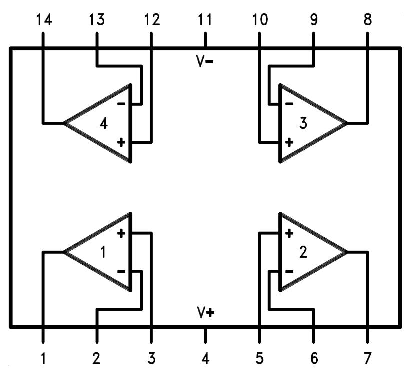


Figure 1. 14-Pin SOIC/PDIP

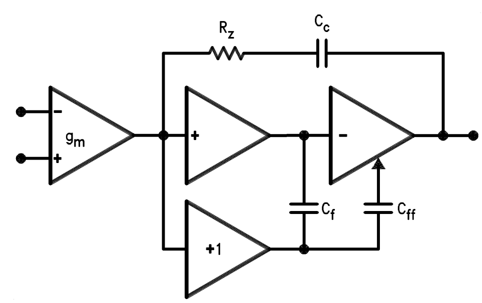


Figure 2. LMC660 Circuit Topology (Each Amplifier)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Differential Input Voltage	±Supply Voltage
Supply Voltage	16V
Output Short Circuit to V^+	See(2)
Output Short Circuit to V^-	See(3)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Voltage at Input/Output Pins	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Power Dissipation	See(4)
Junction Temperature	150°C
ESD tolerance(5)	1000V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.
(3) Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$.
(5) Human Body Model is 1.5 kΩ in series with 100 pF.

Operating Ratings

Temperature Range	
LMC660AI	$-40°C \le T_J \le +85°C$
LMC660C	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	See(1)
Thermal Resistance (θ_{JA})(2)	
14-Pin SOIC	115°C/W
14-Pin PDIP	85°C/W

(1) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.
(2) All numbers apply for packages soldered directly into a PC board.

DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1MΩ unless otherwise specified.

Parameter	Test Conditions	Typ(1)	LMC660AI Limit(1)	LMC660C Limit(1)	Units
Input Offset Voltage		1	3 **3.3**	6 **6.3**	mV max
Input Offset Voltage Average Drift		1.3			μV/°C
Input Bias Current		0.002	 **4**	 **2**	pA max
Input Offset Current		0.001	 **2**	 **1**	pA max
Input Resistance		>1			TeraΩ
Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 12.0V V^+ = 15V	83	70 **68**	63 **62**	dB min
Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V V_O = 2.5V	83	70 **68**	63 **62**	dB min
Negative Power Supply Rejection Ratio	0V ≤ V^- ≤ −10V	94	84 **83**	74 **73**	dB min
Input Common-Mode Voltage Range	V^+ = 5V & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	−0.1 **0**	V max
		V^+ − 1.9	V^+ − 2.3 **V^+ − 2.5**	V^+ − 2.3 **V^+ − 2.4**	V min
Large Signal Voltage Gain	R_L = 2 kΩ(2) Sourcing	2000	440 **400**	300 **200**	V/mV min
	Sinking	500	180 **120**	90 **80**	V/mV min
	R_L = 600Ω(2) Sourcing	1000	220 **200**	150 **100**	V/mV min
	Sinking	250	100 **60**	50 **40**	V/mV min
Output Swing	V^+ = 5V R_L = 2 kΩ to V^+/2	4.87	4.82 **4.79**	4.78 **4.76**	V min
		0.10	0.15 **0.17**	0.19 **0.21**	V max
	V^+ = 5V R_L = 600Ω to V^+/2	4.61	4.41 **4.31**	4.27 **4.21**	V min
		0.30	0.50 **0.56**	0.63 **0.69**	V max
	V^+ = 15V R_L = 2 kΩ to V^+/2	14.63	14.50 **14.44**	14.37 **14.32**	V min
		0.26	0.35 **0.40**	0.44 **0.48**	V max
	V^+ = 15V R_L = 600Ω to V^+/2	13.90	13.35 **13.15**	12.92 **12.76**	V min
		0.79	1.16 **1.32**	1.45 **1.58**	V max

(1) Typical values represent the most likely parametric norm. Limits are specified by testing or correlation.
(2) V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1MΩ unless otherwise specified.

Parameter	Test Conditions	Typ (1)	LMC660AI Limit (1)	LMC660C Limit (1)	Units
Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16	13	mA
			14	**11**	min
	Sinking, V_O = 5V	21	16	13	mA
			14	**11**	min
Output Current V^+ = 15V	Sourcing, V_O = 0V	40	28	23	mA
			25	**21**	min
	Sinking, V_O = 13V (3)	39	28	23	mA
			24	**20**	min
Supply Current	All Four Amplifiers	1.5	2.2	2.7	mA
	V_O = 1.5V		**2.6**	**2.9**	max

(3) Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1MΩ unless otherwise specified.

Parameter	Test Conditions	Typ (1)	LMC660AI Limit (1)	LMC660C Limit (1)	Units
Slew Rate	See (2)	1.1	0.8	0.8	V/μs
			0.6	**0.7**	min
Gain-Bandwidth Product		1.4			MHz
Phase Margin		50			Deg
Gain Margin		17			dB
Amp-to-Amp Isolation	See (3)	130			dB
Input Referred Voltage Noise	F = 1 kHz	22			nV/√Hz
Input Referred Current Noise	f = 1 kHz	0.0002			pA//√Hz
Total Harmonic Distortion	f = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} V^+ = 15V	0.01			%

(1) Typical values represent the most likely parametric norm. Limits are specified by testing or correlation.
(2) V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.
(3) Input referred. V^+ = 15V and R_L = 10 kΩ connected to V^+/2. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

Typical Performance Characteristics

V_S = ±7.5V, T_A = 25°C unless otherwise specified.

Supply Current vs. Supply Voltage

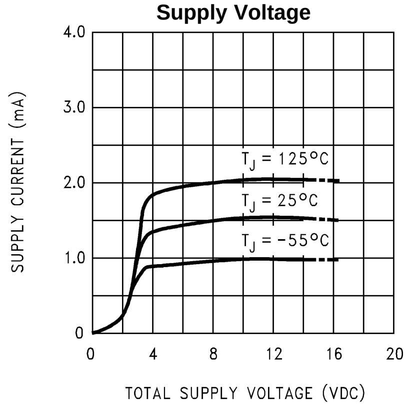


Figure 3.

Offset Voltage

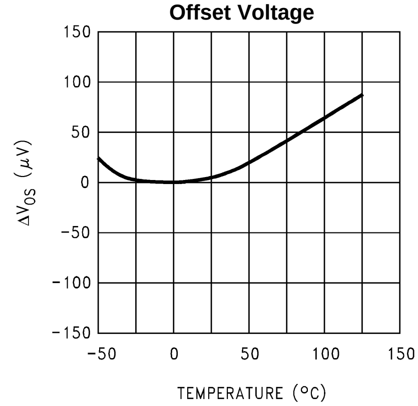


Figure 4.

Input Bias Current

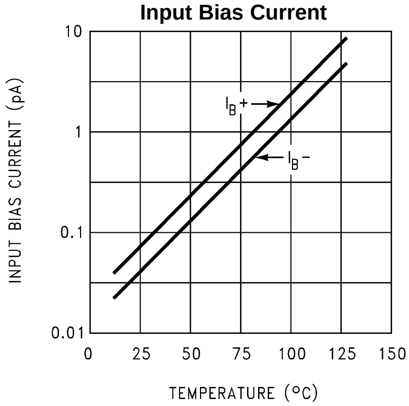


Figure 5.

Output Characteristics Current Sinking

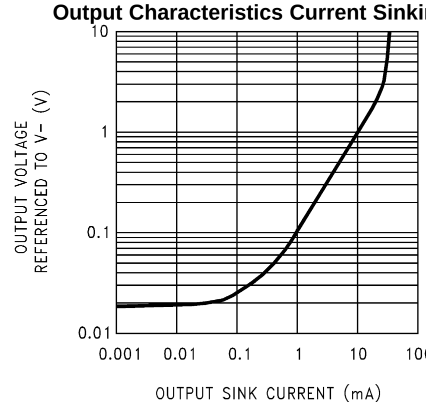


Figure 6.

Output Characteristics Current Sourcing

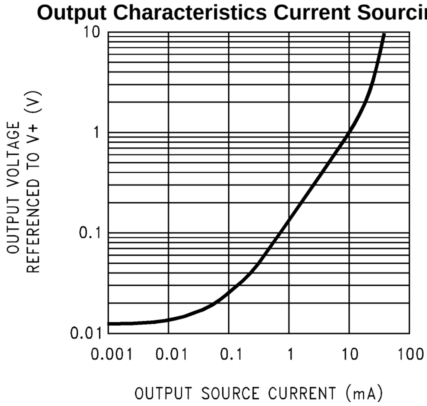


Figure 7.

Input Voltage Noise vs. Frequency

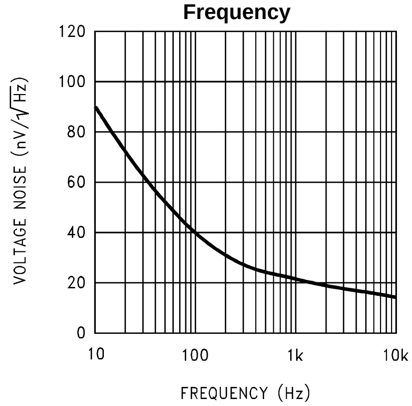


Figure 8.

Typical Performance Characteristics (continued)

V_S = ±7.5V, T_A = 25°C unless otherwise specified.

CMRR vs. Frequency

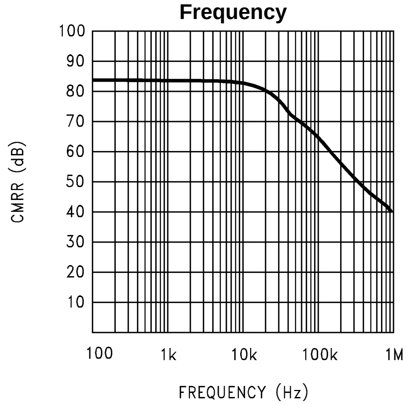


Figure 9.

Open-Loop Frequency Response

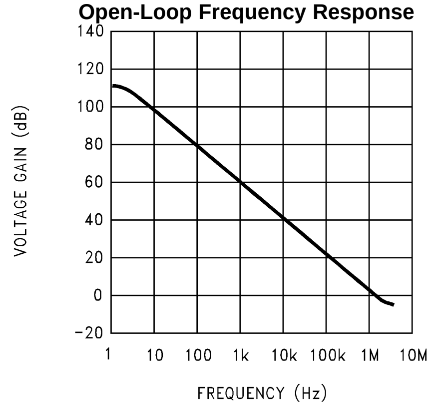


Figure 10.

Frequency Response vs. Capacitive Load

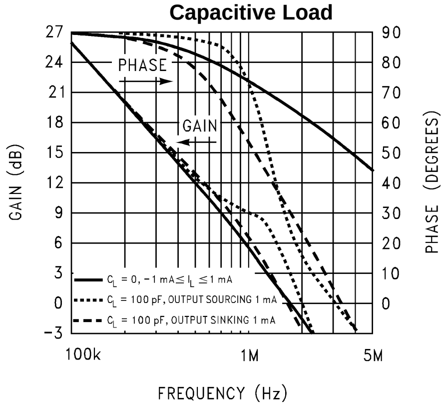


Figure 11.

Non-Inverting Large Signal Pulse Response

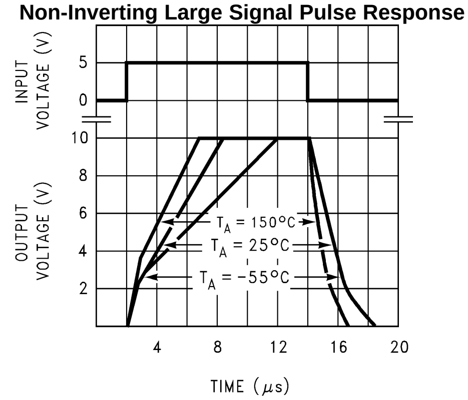


Figure 12.

Stability vs. Capacitive Load

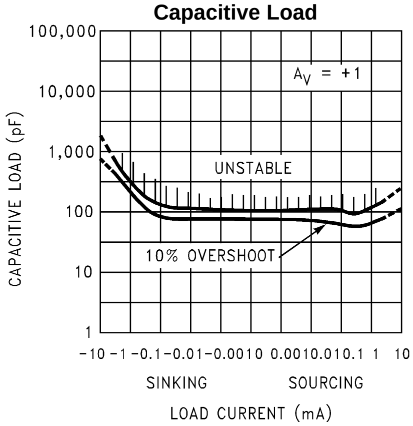


Figure 13.

Stability vs. Capacitive Load

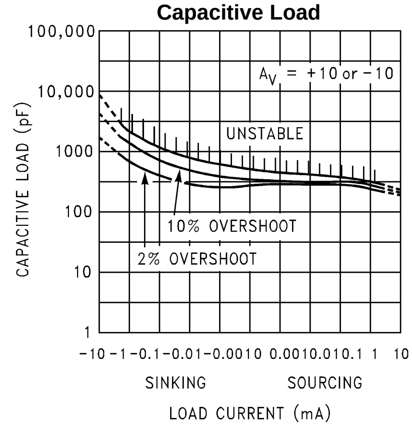


Figure 14.

APPLICATION INFORMATION

AMPLIFIER TOPOLOGY

The topology chosen for the LMC660, shown in Figure 15, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

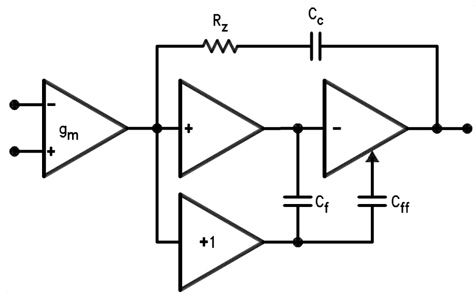


Figure 15. LMC660 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in DC Electrical Characteristics. Avoid resistive loads of less than 500Ω, as they may cause instability.

COMPENSATING INPUT CAPACITANCE

The high input resistance of the LMC660 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier circuit, Figure 16 the frequency of this pole is:

$$fp = \frac{1}{2\pi C_S R_P} \quad (1)$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the “ideal” closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the “ideal” −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability a feedback capacitor will probably be needed if:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S} \quad (2)$$

where:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \quad (3)$$

is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \quad (4)$$

regardless of whether the amplifier is being used in inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S}, \quad (5)$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)} \quad (6)$$

If

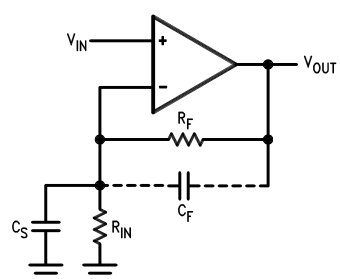
$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S} \quad (7)$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}} \quad (8)$$

Note that these capacitor values are usually significant smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F} \quad (9)$$



C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistors.

Figure 16. General Operational Amplifier Circuit

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the values of C_F should be checked on the actual circuit, starting with the computed value.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC660 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in Figure 17, the addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

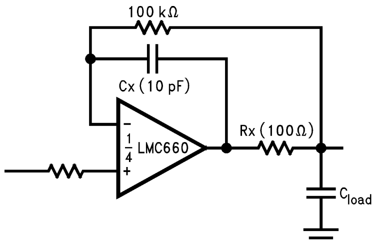


Figure 17. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 18). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see DC Electrical Characteristics).

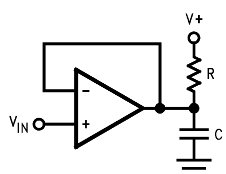


Figure 18. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC662, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC660's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op amp's inputs. See Figure 19. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12}Ω, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11}Ω would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figure 20*a*, Figure 20*b*, and Figure 20*c* for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 20*d*.

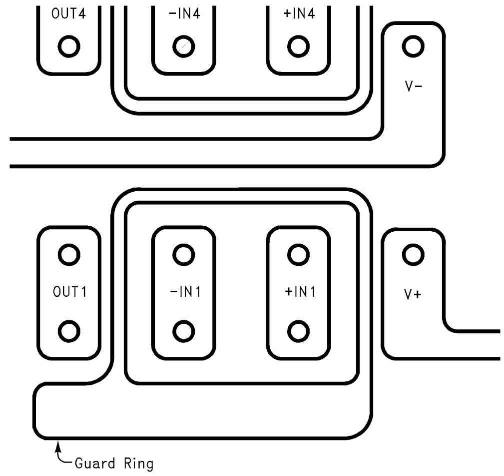


Figure 19. Example, using the LMC660, of Guard Ring in P.C. Board Layout

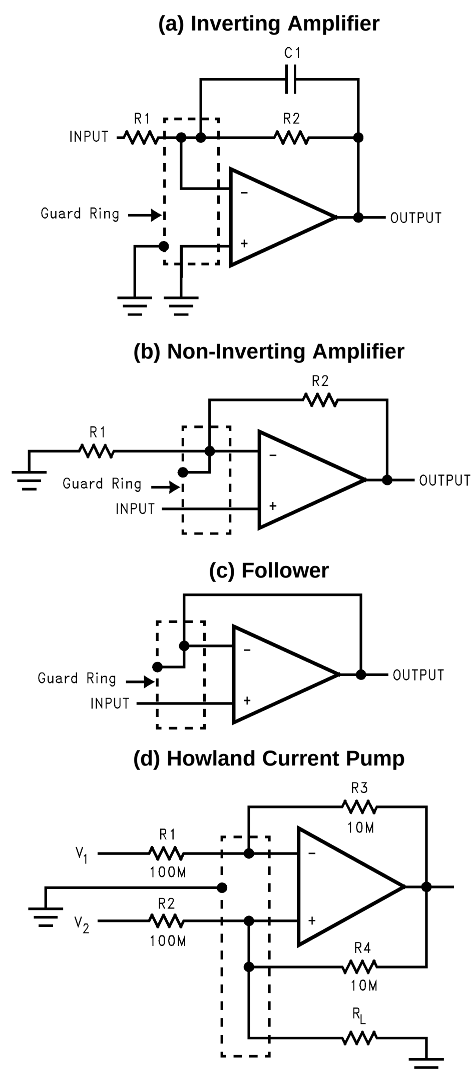
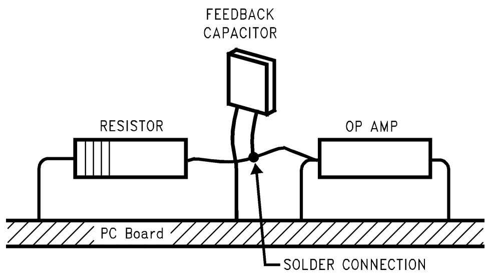


Figure 20. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 21.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

Figure 21. Air Wiring

BIAS CURRENT TESTING

The test method of Figure 21 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then:

$$I_b^- = \frac{dV_{OUT}}{dt} \times C2. \quad (10)$$

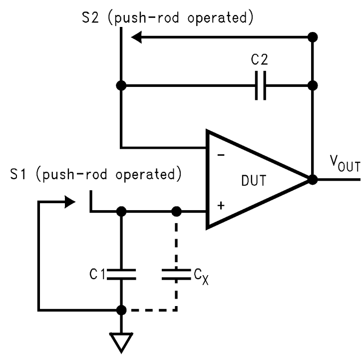


Figure 22. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_b−, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted):

$$I_b^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x) \quad (11)$$

where C_x is the stray capacitance at the + input.

TYPICAL SINGLE-SUPPLY APPLICATIONS

(V^+ = 5.0 VDC)

Additional single-supply applications ideas can be found in the LM324 datasheet. The LMC660 is pin-for-pin compatible with the LM324 and offers greater bandwidth and input resistance over the LM324. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC660 is smaller than that of the LM324.

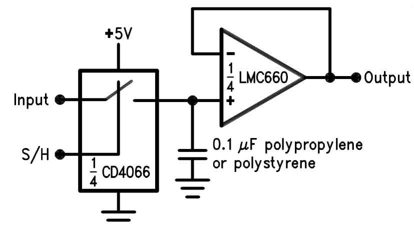


Figure 23. Low-Leakage Sample-and-Hold

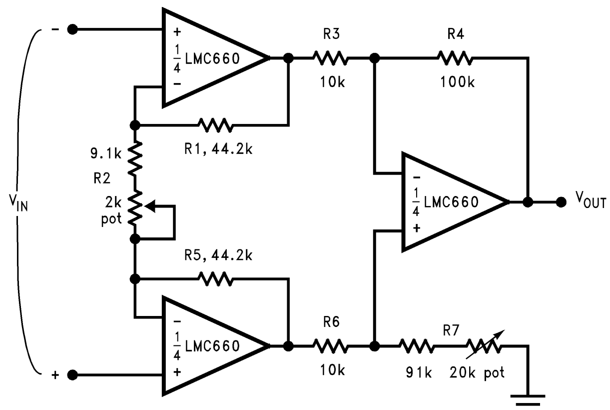


Figure 24. Instrumentation Amplifier

If R1 = R5, R3 = R6, and R4 = R7; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3} \tag{12}$$

$\therefore A_V \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affect CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

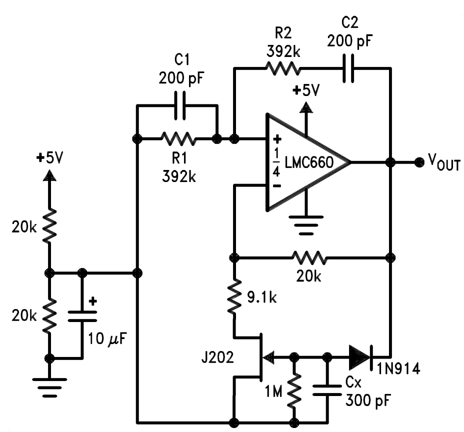


Figure 25. Sine-Wave Oscillator

Oscillator frequency is determined by R1, R2, C1, and C2:

TYPICAL SINGLE-SUPPLY APPLICATIONS (continued)

(V^+ = 5.0 VDC)

fosc = 1/2πRC, where R = R1 = R2 and
C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V.

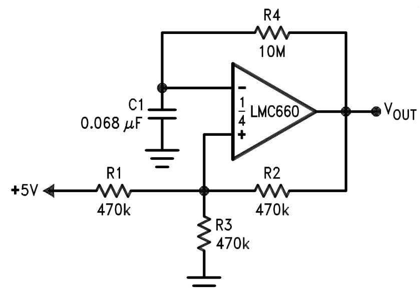


Figure 26. 1 Hz Square-Wave Oscillator

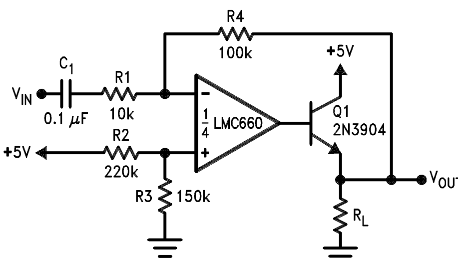


Figure 27. Power Amplifier

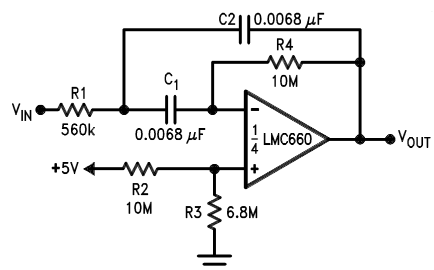


Figure 28. 10 Hz Bandpass Filter

f_O = 10 Hz
Q = 2.1
Gain = −8.8

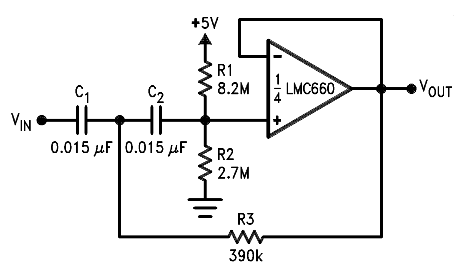


Figure 29. 10 Hz High-Pass Filter

f_c = 10 Hz
d = 0.895
Gain = 1
2 dB passband ripple

TYPICAL SINGLE-SUPPLY APPLICATIONS (continued)

(V^+ = 5.0 VDC)

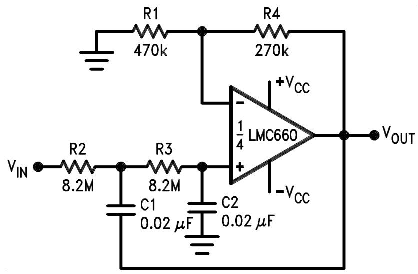


Figure 30. 1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)

f_c = 1 Hz
d = 1.414
Gain = 1.57

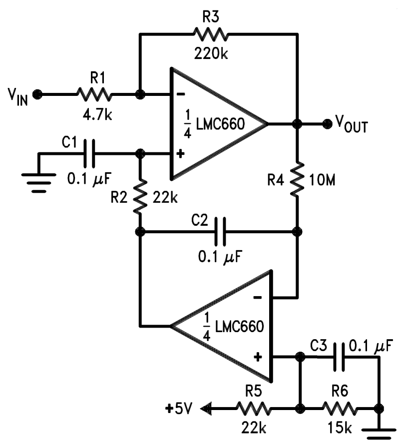


Figure 31. High Gain Amplifier with Offset Voltage Reduction

Gain = −46.8
Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMC660AIM	ACTIVE	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LMC660AIM	Samples
LMC660AIM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC660AIM	Samples
LMC660AIMX	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LMC660AIM	Samples
LMC660AIMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC660AIM	Samples
LMC660AIN	ACTIVE	PDIP	NFF	14	25	TBD	Call TI	Call TI	-40 to 85	LMC660AIN	Samples
LMC660AIN/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LMC660AIN	Samples
LMC660CM	ACTIVE	SOIC	D	14	55	TBD	Call TI	Call TI	0 to 70	LMC660CM	Samples
LMC660CM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LMC660CM	Samples
LMC660CMX	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	0 to 70	LMC660CM	Samples
LMC660CMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LMC660CM	Samples
LMC660CN	ACTIVE	PDIP	NFF	14	25	TBD	Call TI	Call TI	0 to 70	LMC660CN	Samples
LMC660CN/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LMC660CN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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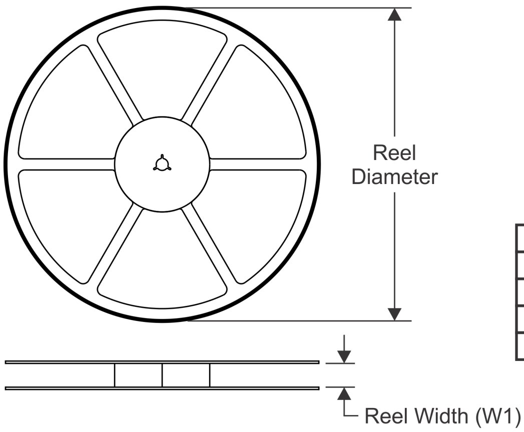
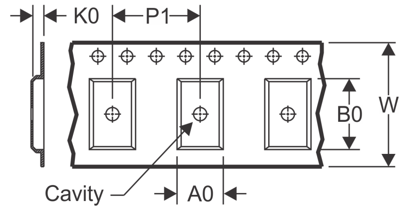
TAPE AND REEL INFORMATION

REEL DIMENSIONS

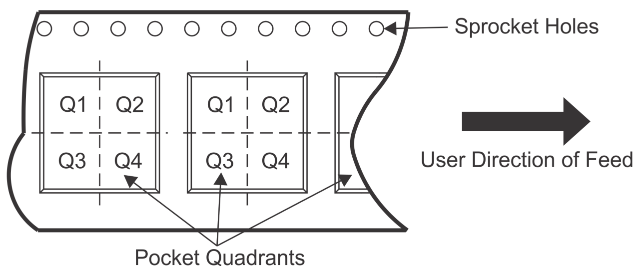


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

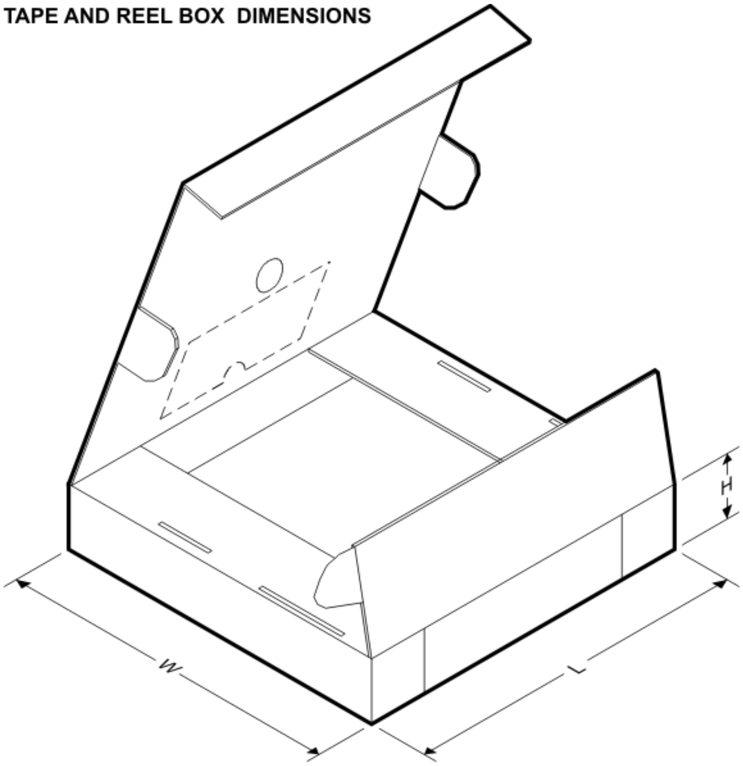
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC660AIMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC660AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC660CMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC660CMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

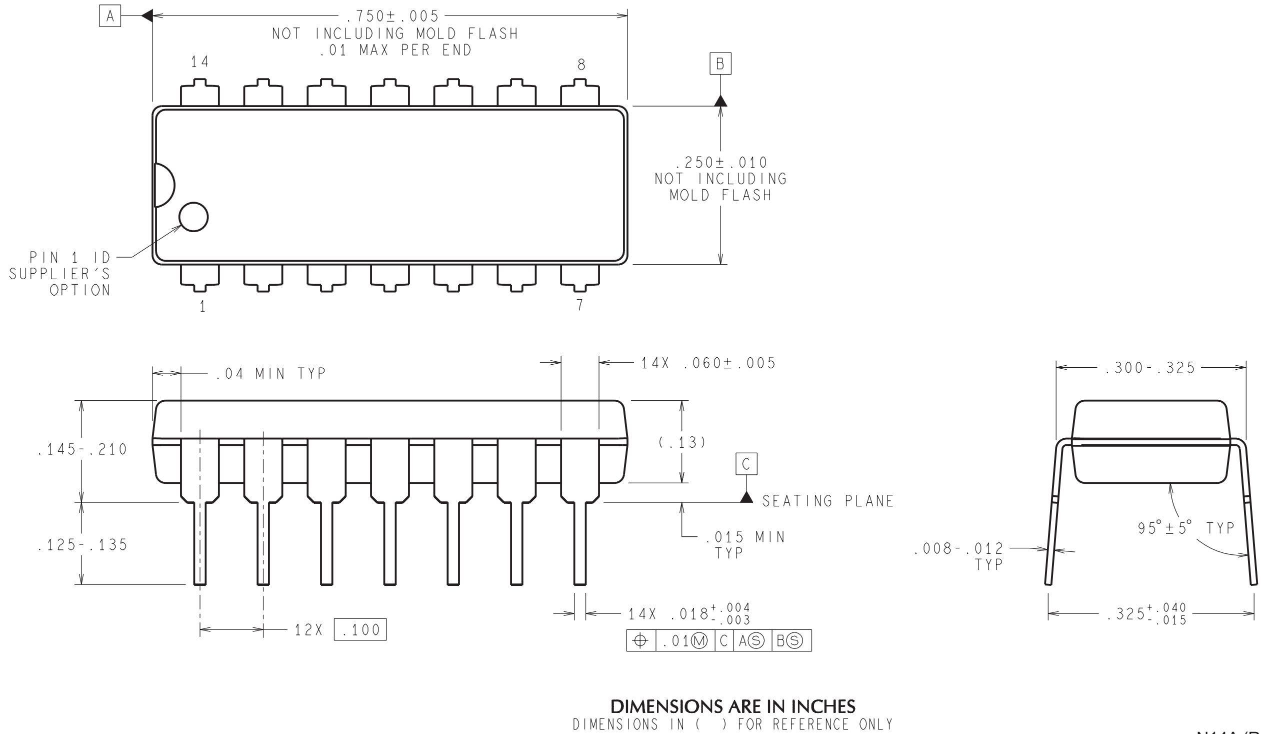
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

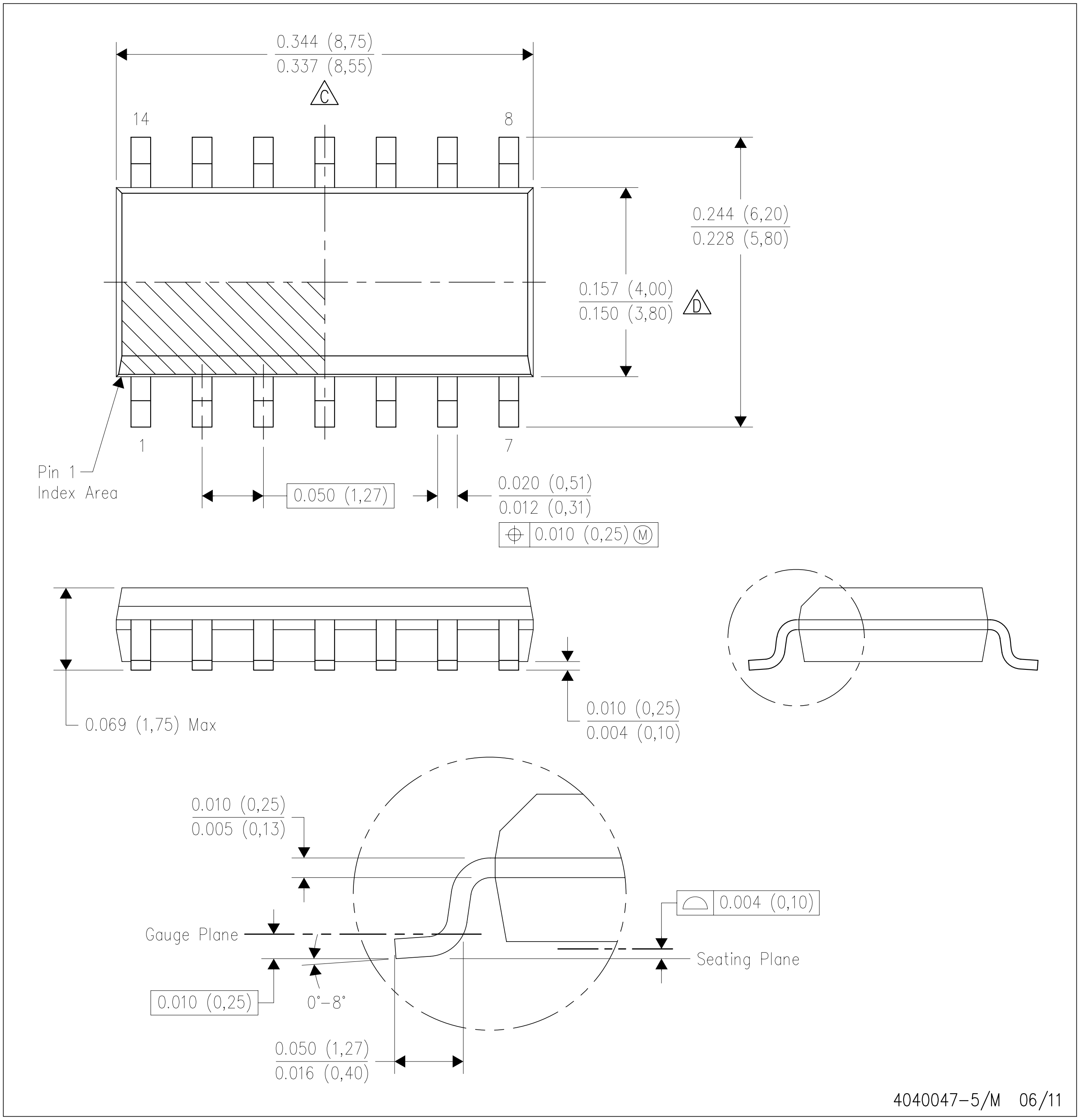
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC660AIMX	SOIC	D	14	2500	367.0	367.0	35.0
LMC660AIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMC660CMX	SOIC	D	14	2500	367.0	367.0	35.0
LMC660CMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

NFF0014A



N14A (Rev G)

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

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