LMH6657/LMH6658 270MHz Single Supply, Single & Dual Amplifiers

Check for Samples: LMH6657, LMH6658

FEATURES

V_S = 5V, T_A = 25°C, R_L = 100Ω (Typical Values Unless Specified)

- **−3dB BW (A_V = +1) 270MHz**
- **Supply Voltage Range 3V to 12V**
- **Slew Rate, (V_S = ±5V) 700V/µs**
- **Supply Current 6.2mA/amp**
- **Output Current +80/−90mA**
- **Input Common Mode volt. 0.5V Beyond V^-, 1.7V from V^+**
- **Output Voltage Swing (R_L = 2kΩ) 0.8V from Rails**
- **Input Voltage Noise 11nV/$\sqrt{Hz}$**
- **Input Current Noise 2.1pA$\sqrt{Hz}$/**
- **DG Error 0.03%**
- **DP Error 0.10°**
- **THD (5MHz) −55dBc**
- **Settling Time (0.1%) 37ns**
- **Fully Characterized for 5V, and ±5V**
- **Output Overdrive Recovery 18ns**
- **Output Short Circuit Protected(1)**
- **No Output Phase Reversal with CMVR Exceeded**

APPLICATIONS

- **CD/DVD ROM**
- **ADC Buffer Amp**
- **Portable Video**
- **Current Sense Buffer**
- **Portable Communications**

(1) Short Circuit Test is a momentary test. See Note 7 under Absolute Maximum Ratings.

DESCRIPTION

The LMH6657/6658 are low-cost operational amplifiers that operate from a single supply with input voltage range extending below the V^-. Based on easy to use voltage feedback topology and boasting fast slew rate (700V/µs) and high speed (140MHz GBWP), the LMH6657 (Single) and LMH6658 (dual) can be used in high speed large signal applications. These applications include instrumentation, communication devices, set-top boxes, etc.

With a -3dB BW of 100MHz (A_V = +2) and DG & DP of 0.03% & 0.10° respectively, the LMH6657/6658 are well suited for video applications. The output stage can typically supply 80mA into the load with a swing of about 1V from either rail.

For Industrial applications, the LMH6657/6658 are excellent cost-saving choices. Input referred voltage noise is low and the input voltage can extend below V^- to ease amplification of low level signals that could be at or near the system ground. With low distortion and fast settling, LMH6657/6658 can provide buffering for A/D and D/A applications.

The LMH6657/6658 versatility and ease of use is extended even further by offering these high slew rate , high speed Op Amps in miniature packages such as SOT-23-5, SC70, SOIC-8, and VSSOP-8. Refer to the Ordering Information section for packaging options available for each device.

Connection Diagram

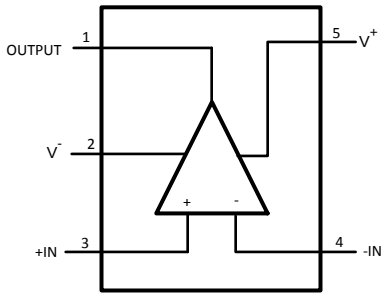


Figure 1. SOT-23-5/SC70-5 (LMH6657)
Top View

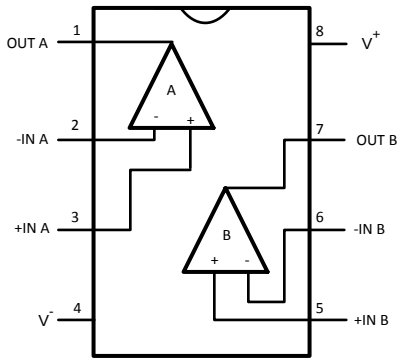


Figure 2. SOIC-8/VSSOP-8 (LMH6658)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance	Human Body Model	2KV(3)
	Machine Model	200V(4)
V_{IN} Differential		±2.5V
Output Short Circuit Duration		See(5)(6)
Input Current		±10mA
Supply Voltage (V^+ - V^-)		12.6V
Voltage at Input/Output pins		V^+ +0.8V, V^- −0.8V
Soldering Information	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C
Storage Temperature Range		−65°C to +150°C
Junction Temperature(7)		+150°C

(1) Absolute maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF.
(4) Machine Model, 0Ω in series with 200pF.
(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(6) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(7) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings(1)

Supply Voltage (V^+ – V^-)		3V to 12V
Operating Temperature Range(2)		−40°C to +85°C
Package Thermal Resistance (θ_{JA})(2)	SC70	478°C/W
	SOT-23–5	265°C/W
	VSSOP-8	235°C/W
	SOIC-8	190°C/W

(1) Absolute maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_L = 100Ω (or as specified) tied to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
GB	Gain Bandwidth Product	V_{OUT} < 200mV$_{PP}$		140		MHz
SSBW	−3dB BW	A_V = +1, V_{OUT} = 200mV$_{PP}$	220	270		MHz
		A_V = +2 or −1, V_{OUT} = 200mV$_{PP}$		100		
GFP	Frequency Response Peaking	A_V = +2, V_{OUT} = 200mV$_{PP}$, DC to 100MHz		1.5		dB
GFR	Frequency Response Rolloff	A_V = +2, V_{OUT} = 200mV$_{PP}$, DC to 100MHz		0.5		dB
$LPD_{1°}$	1° Linear Phase Deviation	A_V = +2, V_{OUT} = 200mV$_{PP}$, ±1°		30		MHz
$GF_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, ±0.1dB, V_{OUT} = 200mV$_{PP}$		13		MHz
PBW	Full Power Bandwidth	−1dB, V_{OUT} = 3V$_{PP}$, A_V = −1		55		MHz
DG	Differential Gain	NTSC, V_{CM} = 2V, R_L = 150Ω to $V^+/2$, Pos. Video Only		0.03		%
DP	Differential Phase	NTSC, V_{CM} = 2V, R_L=150Ω to $V^+/2$ Pos. Video Only		0.1		deg
Time Domain Response						
t_r	Rise and Fall Time	A_V = +2, V_{OUT} = 500mV$_{PP}$		3.3		ns
		A_V = −1, V_{OUT} = 500mV$_{PP}$		3.4		
OS	Overshoot, Undershoot	A_V = +2, V_{OUT} = 500mV$_{PP}$		18		%
t_s	Settling Time	V_O = 2V$_{PP}$, ±0.1%, R_L = 500Ω to $V^+/2$, A_V = −1		37		ns
SR	Slew Rate (3)	A_V = −1, V_O = 3V$_{PP}$ (4)		470		V/µs
		A_V = +2, V_O = 3V$_{PP}$ (4)		420		
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	f = 5MHz, V_O = 2V$_{PP}$, A_V = -1		−70		dBc
HD3	3rd Harmonic Distortion	f = 5MHz, V_O = 2V$_{PP}$, A_V = -1		−57		dBc
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V$_{PP}$, A_V = -1		−55.5		dBc
V_n	Input-Referred Voltage Noise	f = 100KHz		11		nV/√Hz
		f = 1KHz		19		
I_n	Input-Referred Current Noise	f = 100KHz		2.1		pA/√Hz
		f = 1KHz		7.5		
XTLKA	Cross-Talk Rejection (LMH6658)	f = 5MHz, R_L (SND) = 100Ω RCV: R_F = R_G = 1k		69		dB
Static, DC Performance						
A_{VOL}	Large Signal Voltage Gain	V_O = 1.25V to 3.75V, R_L = 2k to $V^+/2$	85	95		dB
		V_O = 1.5V to 3.5V, R_L = 150Ω to $V^+/2$	75	85		
		V_O = 2V to 3V, R_L = 50Ω to $V^+/2$	70	80		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB	−0.2 **−0.1**	−0.5		V
			3.0 **2.8**	3.3		
V_{OS}	Input Offset Voltage			±1.1	±5 **±7**	mV

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the "worst case" of the rising and falling slew rates.
(4) Output Swing not limited by Slew Rate limit.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L = 100Ω (or as specified) tied to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
TC V_{OS}	Input Offset Voltage Average Drift	See (5)		±2		µV/C
I_B	Input Bias Current	See (6)		−5	−20 **−30**	µA
TC $_{IB}$	Input Bias Current Average Drift	See (5)		0.01		nA/°C
I_{OS}	Input Offset Current			50	300 **500**	nA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.0V	72	82		dB
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 4.5V to 5.5V, V_{CM} = 1V	72	82		dB
I_S	Supply Current (per channel)	No load		6.2	8.5 **10**	mA
Miscellaneous Performance						
V_{OH}	Output Swing High	R_L = 2k to V^+/2	4.10 **3.8**	4.25		V
		R_L = 150Ω to V^+/2	4.00 **3.70**	4.19		
		R_L = 75Ω to V^+/2	3.85 **3.50**	4.15		
V_{OL}	Output Swing Low	R_L = 2k to V^+/2	900 **1100**	800		mV
		R_L = 150Ω to V^+/2	970 **1200**	870		
		R_L = 75Ω to V^+/2	990 **1250**	885		
I_{OUT}	Output Current	V_{OUT} = 1V from either rail	±40	+85, −105		mA
I_{SC}	Output Short CircuitCurrent (7)	Sourcing to V^+/2	100 **80**	155		mA
		Sinking to V^+/2	100 **80**	220		
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			1.8		pF
R_{OUT}	Output Impedance	f = 1MHz, A_V = +1		0.06		Ω

(5) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(6) Positive current corresponds to current flowing into the device.
(7) Short circuit test is a momentary test. See Note 6 under Absolute Maximum Ratings.

±5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = V_O, and R_L = 100Ω (or as specified) tied to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
GB	Gain Bandwidth Product	V_{OUT} < 200mV_{PP}		140		MHz
SSBW	−3dB BW	A_V = +1, V_{OUT} = 200mV_{PP}	220	270		MHz
		A_V = +2 or −1, V_{OUT} = 200mV_{PP}		100		
GFP	Frequency Response Peaking	A_V = +2, V_{OUT} = 200mV_{PP}, DC to 100MHz		1.0		dB
GFR	Frequency Response Rolloff	A_V = +2, V_{OUT} = 200mV_{PP}, DC to 100MHz		0.9		dB
$LPD_{1°}$	1° Linear Phase Deviation	A_V = +2, V_{OUT} = 200mV_{PP}, ±1°		30		MHz

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = V_O, and R_L = 100Ω (or as specified) tied to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
$GF_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, ±0.1dB, V_{OUT} = 200mV_{PP}		20		MHz
PBW	Full Power Bandwidth	−1dB, V_{OUT} = 8V_{PP}, A_V = −1		30		MHz
DG	Differential Gain	NTSC, R_L = 150Ω, Pos. or Neg. Video		0.03		%
DP	Differential Phase	NTSC,R_L = 150Ω, Pos. or Neg. Video		0.1		deg
Time Domain Response						
t_r	Rise and Fall Time	A_V = +2, V_{OUT} = 500mV_{PP}		3.3		ns
		A_V = −1, V_{OUT} = 500mV_{PP}		3.3		
OS	Overshoot, Undershoot	A_V = +2, V_{OUT} = 500mV_{PP}		16		%
t_s	Settling Time	V_O = 5V_{PP}, ±0.1%, R_L =500Ω, A_V = −1		35		ns
SR	Slew Rate(3)	A_V = −1, V_O = 8V_{PP}		700		V/µs
		A_V = +2, V_O = 8V_{PP}		500		
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A_V = -1		−70		dBc
HD3	3rd Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A_V = -1		−57		dBc
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A_V = -1		−55.5		dBc
V_n	Input-Referred Voltage Noise	f = 100KHz		11		nV/√Hz
		f = 1KHz		19		
I_n	Input-Referred Current Noise	f = 100KHz		2.1		pA/√Hz
		f = 1KHz		7.5		
XTLKA	Cross-Talk Rejection (LMH6658)	f = 5MHz, R_L (SND) = 100Ω RCV: R_F = R_G = 1k		69		dB
Static, DC Performance						
A_{VOL}	Large Signal Voltage Gain	V_O = −3.75V to 3.75V, R_L = 2k	87	100		dB
		V_O = −3.5V to 3.5V, R_L = 150Ω	80	90		
		V_O = −3V to 3V, R_L = 50Ω	75	85		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB	−5.2 **−5.1**	−5.5		V
			3.0 **2.8**	3.3		
V_{OS}	Input Offset Voltage			±1.0	±5 **±7**	mV
TC V_{OS}	Input Offset Voltage Average Drift	See(4)		±2		µV/C
I_B	Input Bias Current	See(5)		−5	−20 **−30**	µA
TC_{IB}	Input Bias Current Average Drift	See(4)		0.01		nA/°C
I_{OS}	Input Offset Current			50	300 **500**	nA
CMRR	Common ModeRejection Ratio	V_{CM} Stepped from −5V to 3.0V	75	84		dB
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 4.5V to 5.5V, V_{CM} = −4V	75	82		dB
−PSRR	Negative Power Supply Rejection Ratio	V^- = −4.5V to −5.5V	78	85		dB
I_S	Supply Current (per channel)	No load		6.5	9.0 **11**	mA
Miscellaneous Performance						

(3) Slew rate is the "worst case" of the rising and falling slew rates.
(4) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = V_O, and R_L = 100Ω (or as specified) tied to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[1]	Typ[2]	Max[1]	Units
V_{OH}	Output Swing High	R_L = 2k	4.10 **3.80**	4.25		V
		R_L = 150Ω	4.00 **3.70**	4.20		
		R_L = 75Ω	3.85 **3.50**	4.18		
V_{OL}	Output Swing Low	R_L = 2k	−4.05 **−3.80**	−4.19		V
		R_L = 150Ω	−3.90 **−3.65**	−4.05		
		R_L = 75Ω	−3.80 **−3.50**	−4.00		
I_{OUT}	Output Current	V_{OUT} = 1V from either rail	±45	+100, −110		mA
I_{SC}	Output Short Circuit Current[6]	Sourcing to Ground	120 **100**	180		mA
		Sinking to Ground	120 **100**	230		
R_{IN}	Common Mode Input Resistance			4		MΩ
C_{IN}	Common Mode Input Capacitance			1.8		pF
R_{OUT}	Output Impedance	f = 1MHz, A_V = +1		0.06		Ω

(6) Short circuit test is a momentary test. See Note 6 under Absolute Maximum Ratings.

Typical Performance Characteristics

Non-Inverting Frequency Response, Gain

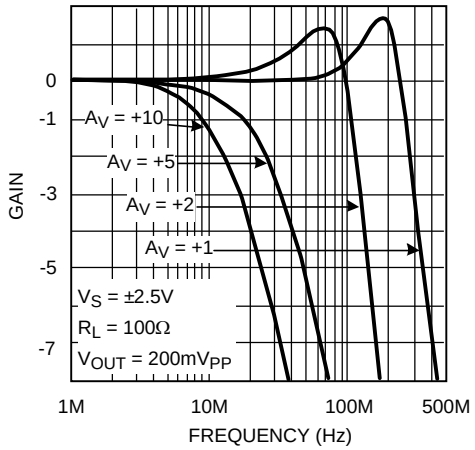


Figure 3.

Inverting Frequency Response, Gain

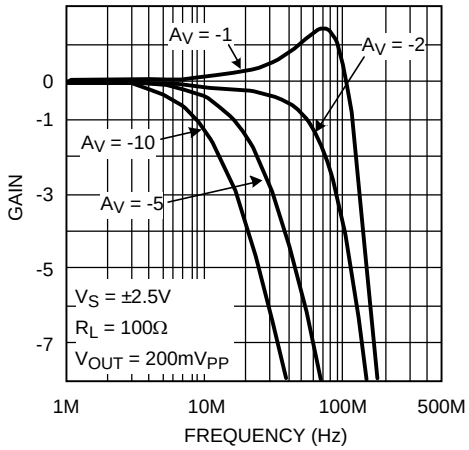


Figure 4.

Non-Inverting Frequency Response, Phase

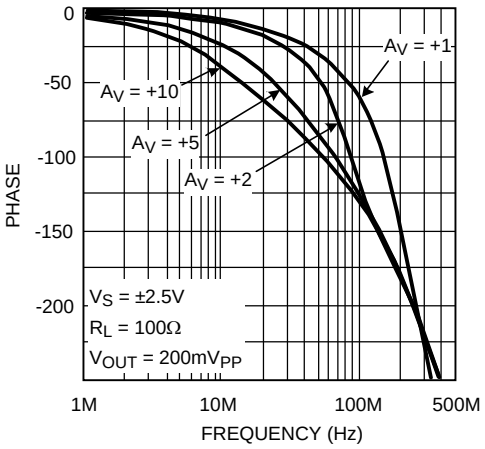


Figure 5.

Inverting Frequency Response, Phase

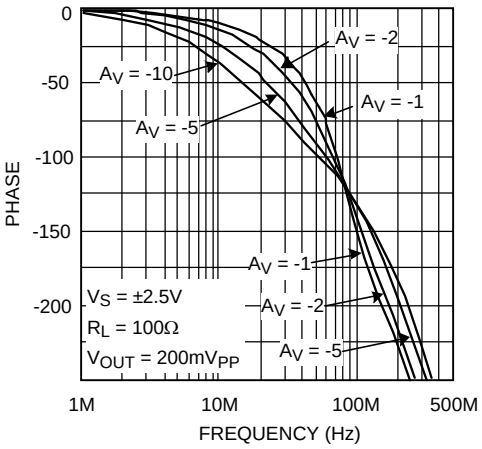


Figure 6.

Open Loop Gain/Phase vs. Frequency

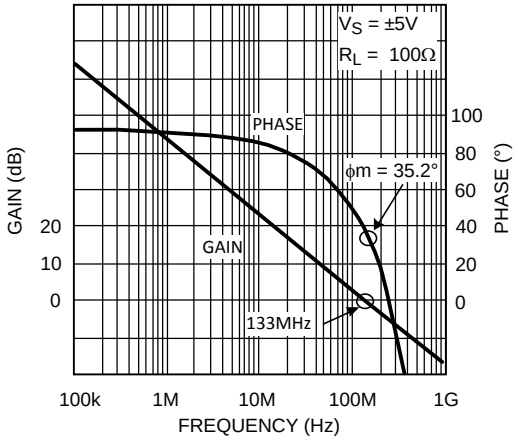


Figure 7.

Unity Gain Frequency vs. V_{CM}

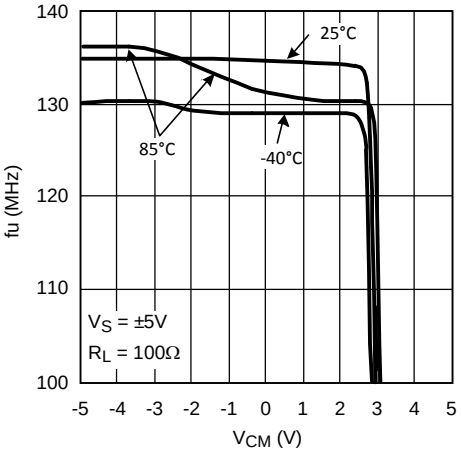


Figure 8.

Typical Performance Characteristics (continued)

Phase Margin vs. V_{CM}

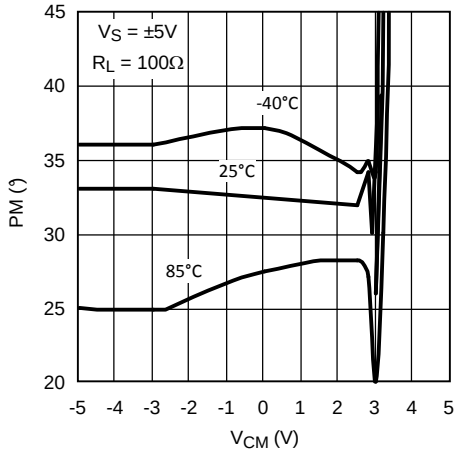


Figure 9.

Output vs. Input

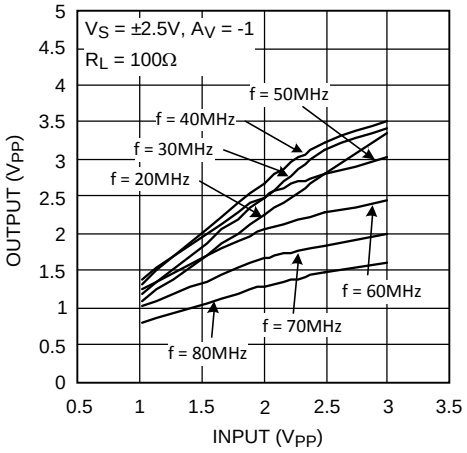


Figure 10.

Output vs. Input

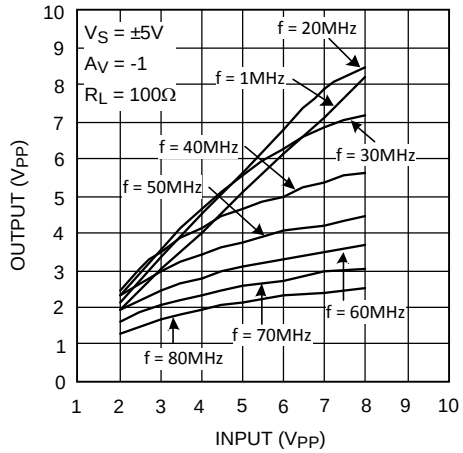


Figure 11.

CMRR vs. Frequency

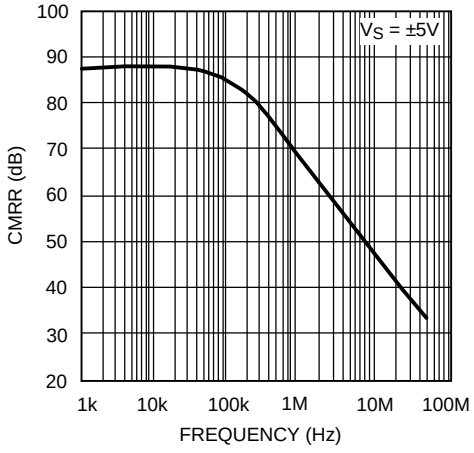


Figure 12.

PSRR vs. Frequency

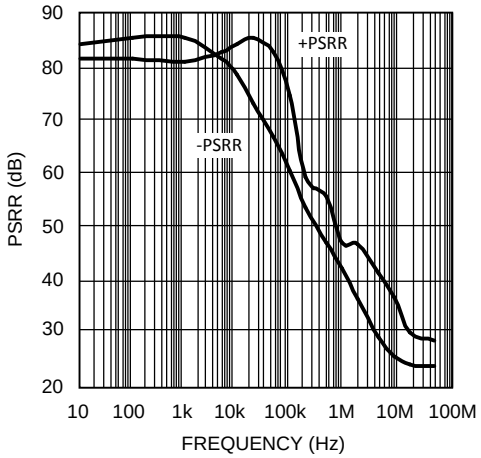


Figure 13.

DG/DP vs. IRE

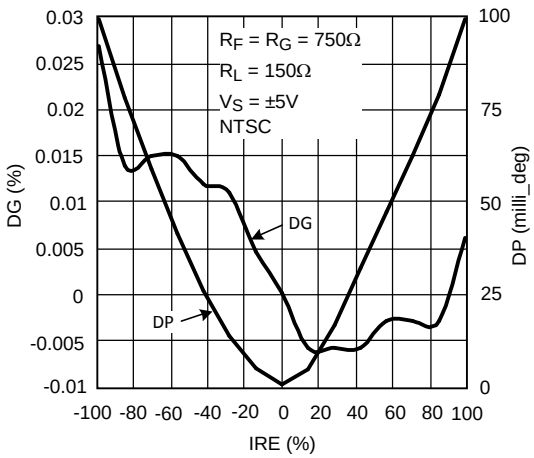


Figure 14.

Typical Performance Characteristics (continued)

Noise vs. Frequency

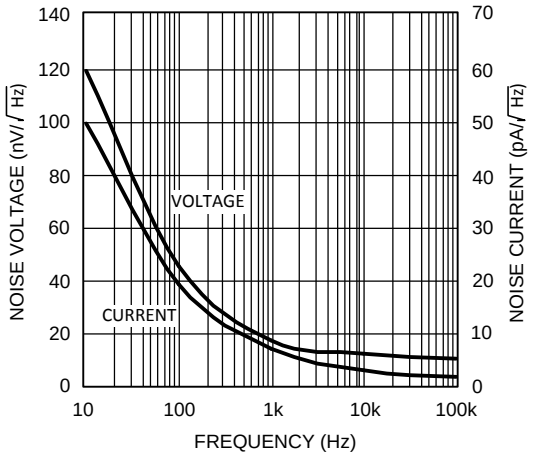


Figure 15.

Crosstalk Rejection vs. Frequency

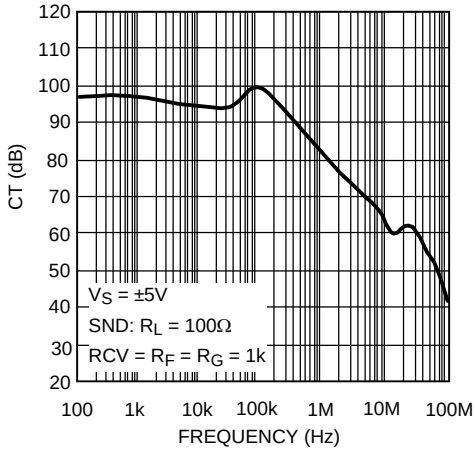


Figure 16.

Output Impedance vs. Frequency

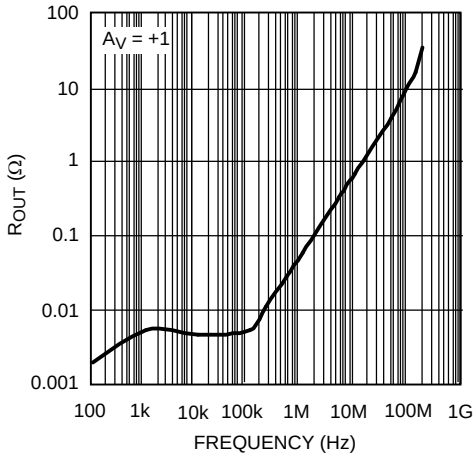


Figure 17.

HD vs. V_{OUT}

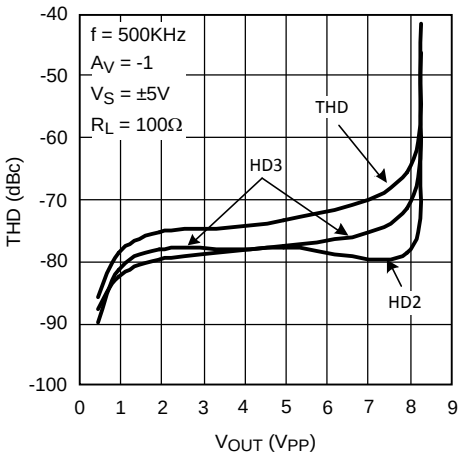


Figure 18.

HD vs. V_{OUT}

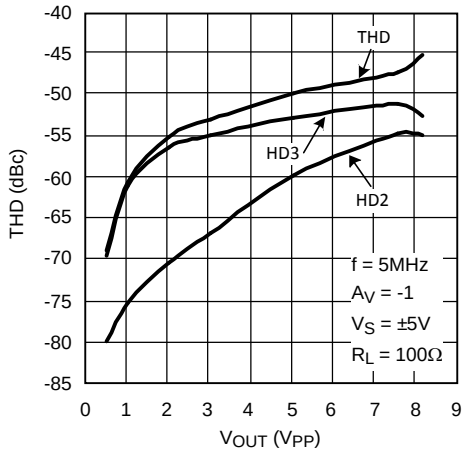


Figure 19.

THD vs. V_{OUT}

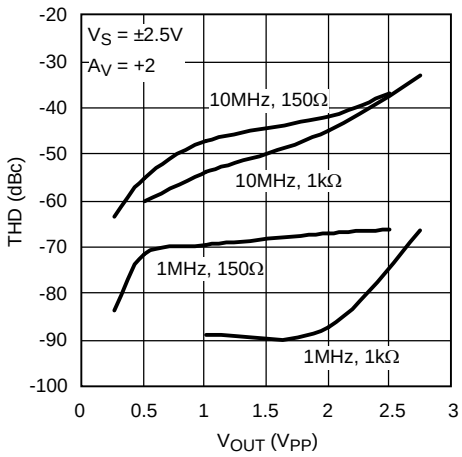


Figure 20.

Typical Performance Characteristics (continued)

HD vs. Frequency

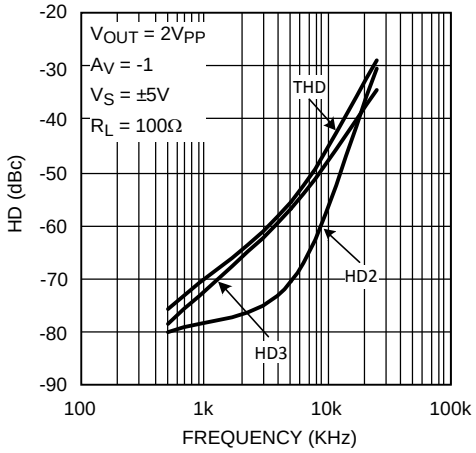


Figure 21.

HD vs. Frequency

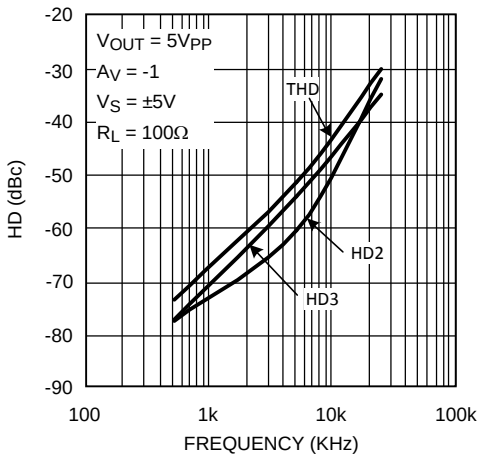


Figure 22.

V_{OUT} vs. I_{SOURCE}

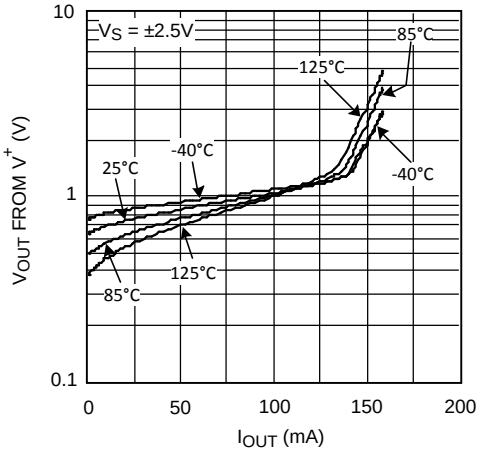


Figure 23.

V_{OUT} vs. I_{SINK}

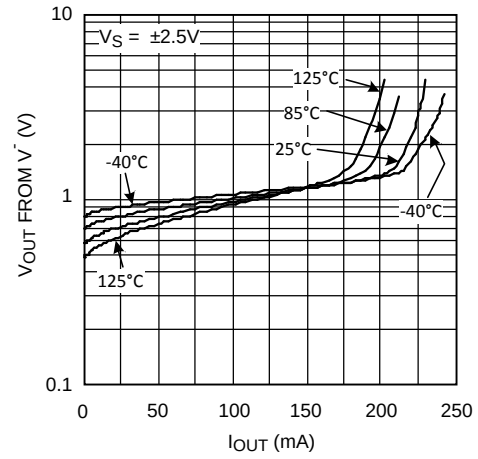


Figure 24.

V_{OUT} vs. I_{SOURCE}

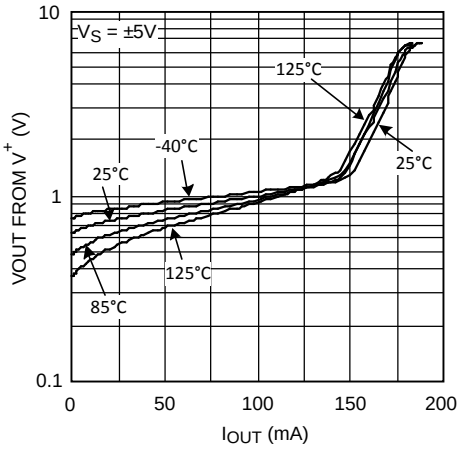


Figure 25.

V_{OUT} vs. I_{SINK}

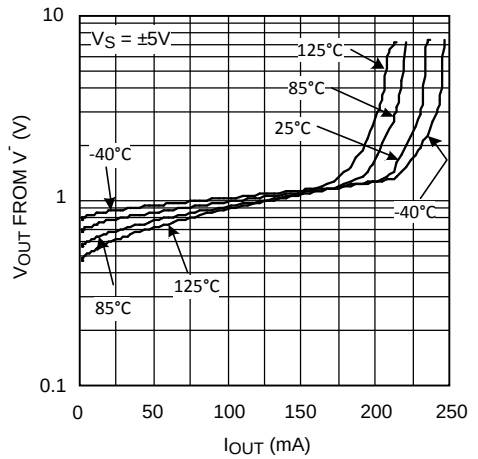


Figure 26.

Typical Performance Characteristics (continued)

Short Circuit Current

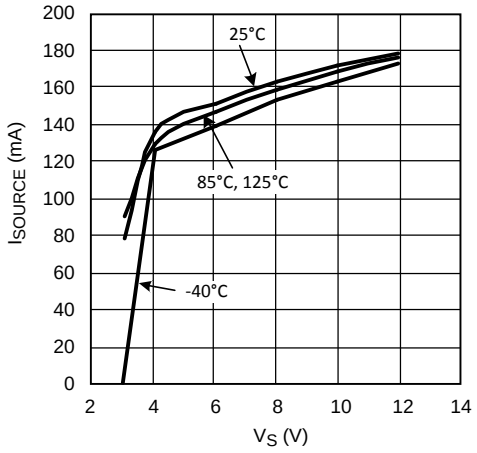


Figure 27.

Short Circuit Current

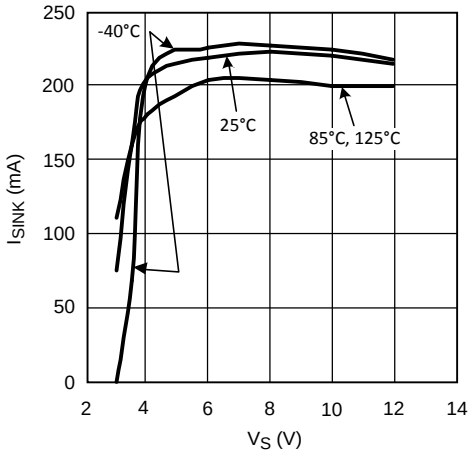


Figure 28.

Settling Time vs. Output Step Amplitude

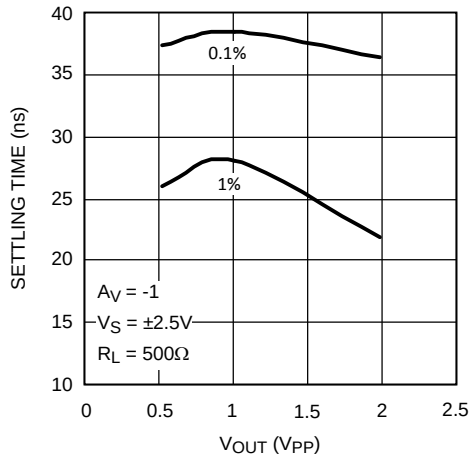


Figure 29.

Settling Time vs. Output Step Amplitude

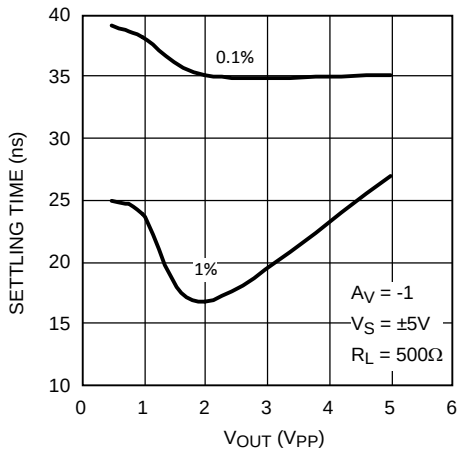


Figure 30.

0.1% Settling Time vs. Cap Load

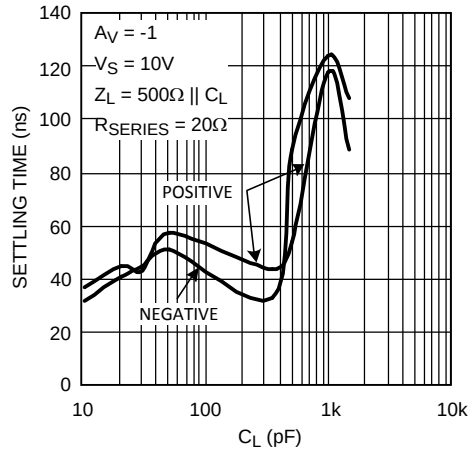


Figure 31.

ΔV_{OS} vs. V_{OUT}

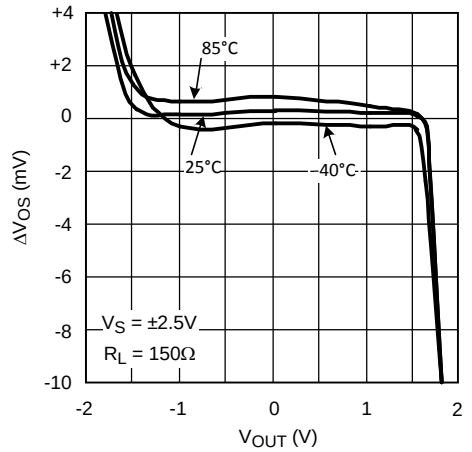


Figure 32.

Typical Performance Characteristics (continued)

ΔV_{OS} vs. V_{OUT}

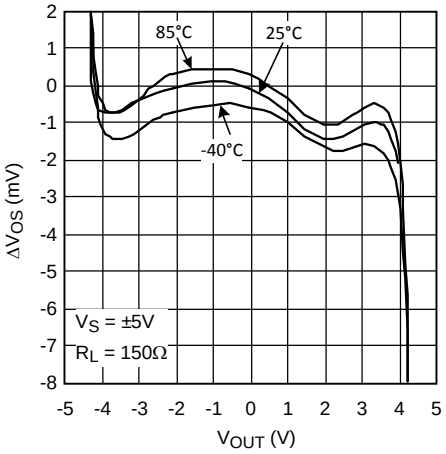


Figure 33.

I_S /Amp vs. V_S

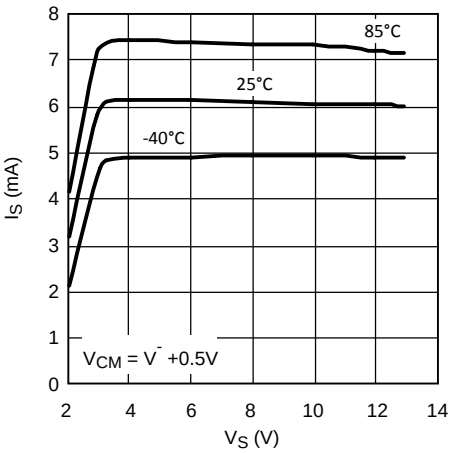


Figure 34.

I_S/Amp vs. V_{CM}

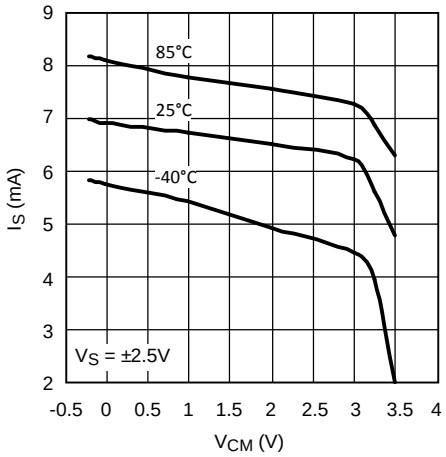


Figure 35.

I_S/Amp vs. V_{CM}

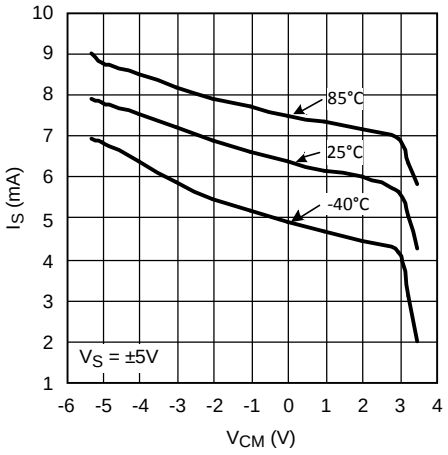


Figure 36.

V_{OS} vs. V_S (for 3 Representative Units)

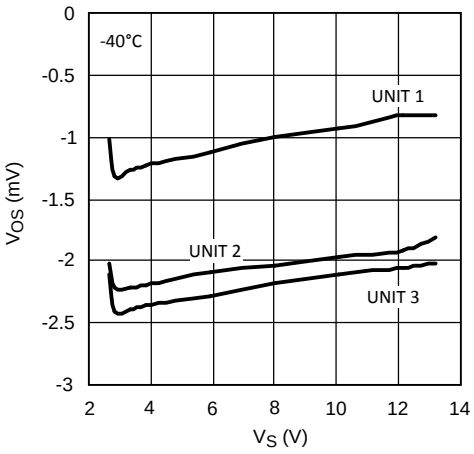


Figure 37.

V_{OS} vs. V_S (for 3 Representative Units)

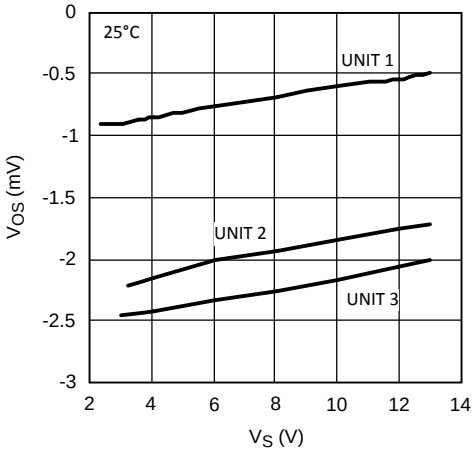


Figure 38.

Typical Performance Characteristics (continued)

V_{OS} vs. V_S (for 3 Representative Units)

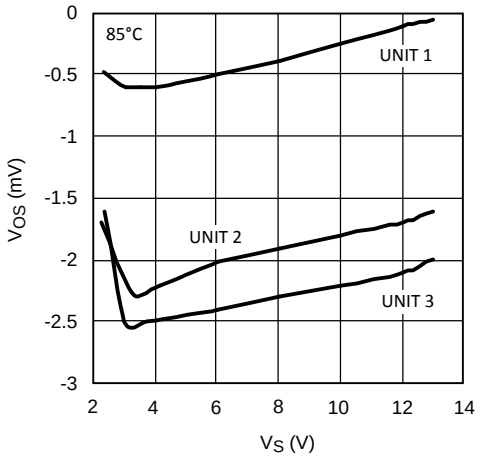


Figure 39.

V_{OS} vs. V_{CM} (A Typical Unit)

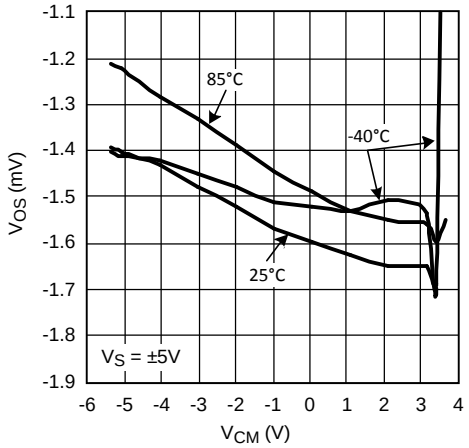


Figure 40.

$|I_B|$ vs. V_S

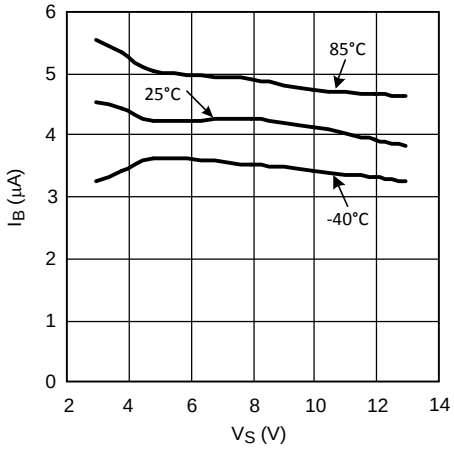


Figure 41.

I_{OS} vs. V_S

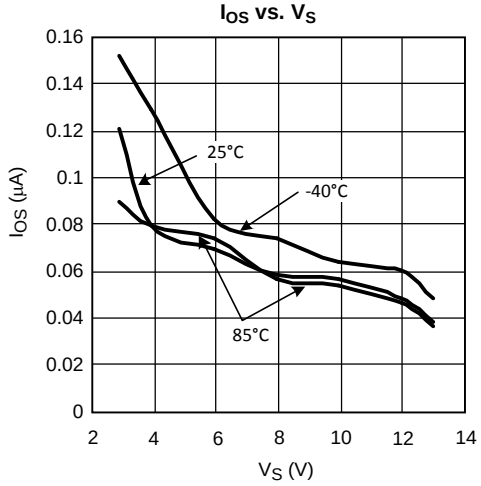


Figure 42.

Small Signal Step Response

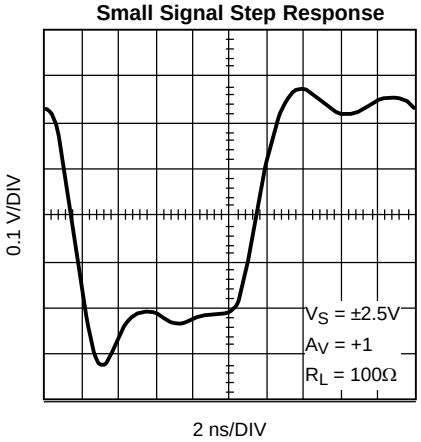


Figure 43.

Small Signal Step Response

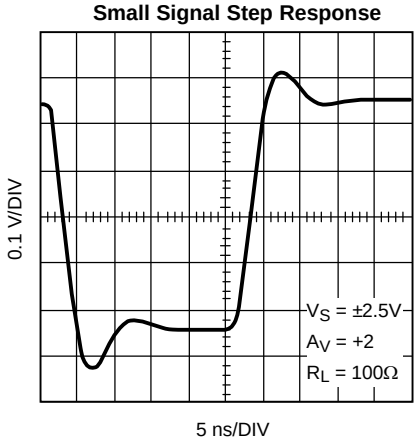


Figure 44.

Typical Performance Characteristics (continued)

Small Signal Step Response

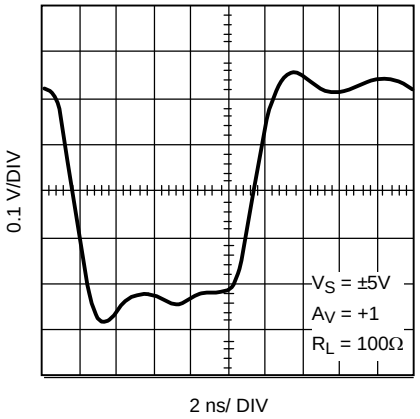


Figure 45.

Small Signal Step Response

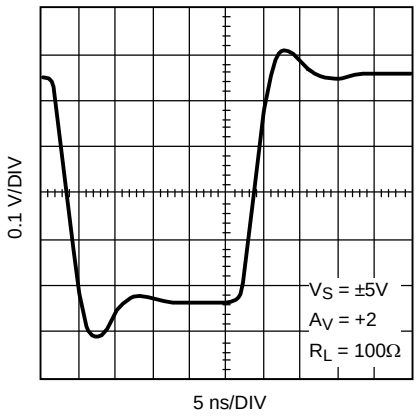


Figure 46.

Large Signal Step Response

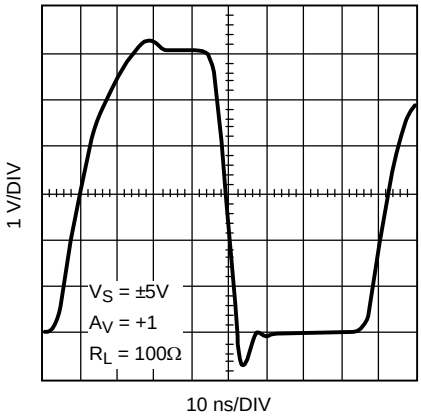


Figure 47.

Large Signal Step Response

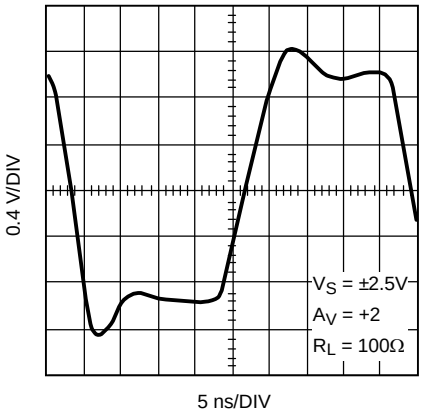


Figure 48.

Large Signal Step Response

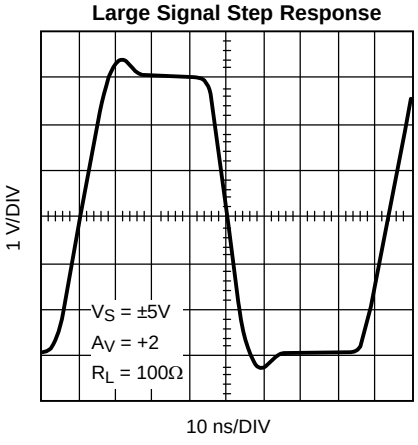


Figure 49.

APPLICATION SECTION

LARGE SIGNAL BEHAVIOR

The LMH6657/6658 is specially designed to handle large output swings, such as those encountered in video waveforms, without being slew rate limited. With 5V supply, the LMH6657/6658 slew rate limit is larger than that might be necessary to make full allowable output swing excursions. Therefore, the large signal frequency response is dominated by the small signal characteristics, rather than the conventional limitation imposed by slew rate limit.

The LMH6657/6658 input stage is designed to provide excess overdrive when needed. This occurs when fast input signal excursions cannot be followed by the output stage. In these situations, the device encounters larger input signals than would be encountered under normal closed loop conditions. The LMH6657/6658 input stage is designed to take advantage of this "input overdrive" condition. The larger the amount of this overdrive, the greater is the speed with which the output voltage can change. Here is a plot of how the output slew rate limitation varies with respect to the amount of overdrive imposed on the input:

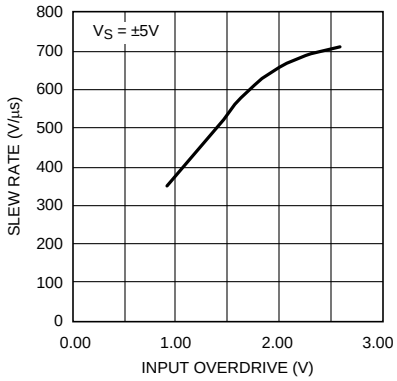


Figure 50. Plot Showing the Relationship Between Slew Rate and Input Overdrive

To relate the explanation above to a practical example, consider the following application example. Consider the case of a closed loop amplifier with a gain of −1 amplifying a sinusoidal waveform. From the plot of Output vs. Input (Typical Performance Characteristics section), with a 30MHz signal and $7V_{PP}$ input signal, it can be seen that the output will be limited to a swing of $6.9V_{PP}$. From the frequency Response plot it can be seen that the inverting gain of −1 has a −32° output phase shift at this frequency. It can be shown that this setup will result in about $1.9V_{PP}$ differential input voltage corresponding to 650V/µs of slew rate from Figure 50, above ($SR = V_O(pp)*\pi*f = 650V/\mu s$). Note that the amount of overdrive appearing on the input for a given sinusoidal test waveform is affected by the following:

- Output swing
- Gain setting
- Input/output phase relationship for the given test frequency
- Amplifier configuration (inverting or non-inverting)

Due to the higher frequency phase shift between input and output, there is no closed form solution to input overdrive for a given input. Therefore, Figure 50 is not very useful by itself in determining the output swing.

The following plots aid in predicting the output transition time based on the amount of swing required for a given gain setting.

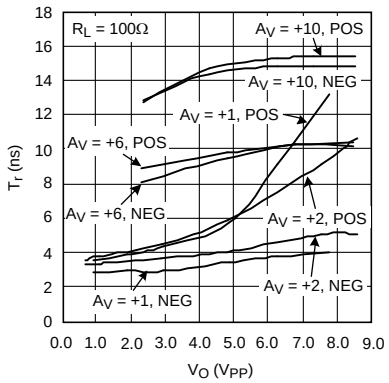


Figure 51. Output 20%-80% Transition vs. Output Voltage Swing (Non-Inverting Gain)

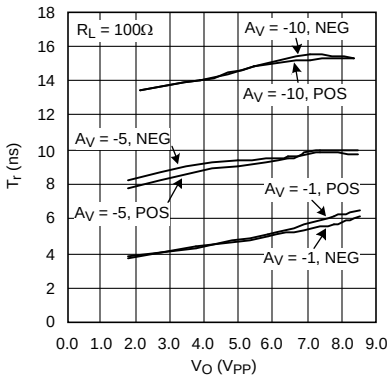


Figure 52. Output 20%-80% Transition vs. Output Voltage Swing (Inverting Gain)

Beyond a gain of 5 or so, the LMH6657/6658 output transition would be limited by bandwidth. For example, with a gain of 5, the −3dB BW would be around 30MHz corresponding to a rise time of about 12ns (10% - 90%). Assuming a near linear transition, the 20%-80% transition time would be around 9ns which matches the measured results as shown in Figure 51.

When the output is heavily loaded, output swing may be limited by current capability of the device. Refer to Output Current Capability section, below, for more details.

Output Characteristics

OUTPUT CURRENT CAPABILITY

The LMH6657/6658 output swing for a given load can be determined by referring to the Output Voltage vs. Output Current plots (Typical Performance Characteristics section). Characteristic Tables show the output current when the output is 1V from either rail. The plots and table values can be used to predict closed loop continuous value of current for a given load. If left unchecked, the output current capability of the LMH6657/6658 could easily result in junction temperature exceeding the maximum allowed value specified under Absolute Maximum Ratings. Proper heat sinking or other precautions are required if conditions as such, exist.

Under transient conditions, such as when the input voltage makes a large transition and the output has not had time to reach its final value, the device can deliver output currents in excess of the typical plots mentioned above. Plots shown in Figure 53 and 54 below depict how the output current capability improves under higher input overdrive voltages:

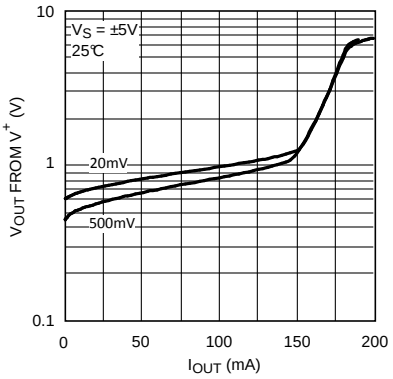


Figure 53. V_{OUT} vs. I_{SOURCE} (for Various Overdrive)

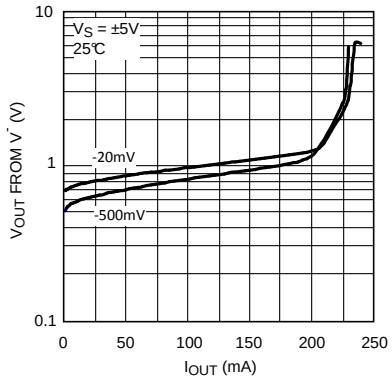


Figure 54. V_{OUT} vs. I_{SINK} (for Various Overdrive)

The LMH6657/6658 output stage is designed to swing within approximately one diode drop of each supply voltage by utilizing specially designed high speed output clamps. This allows adequate output voltage swing even with 5V supplies and yet avoids some of the issues associated with rail-to-rail output operational amplifiers. Some of these issues are:

- Supply current increases when output reaches saturation at or near the supply rails
- Prolonged recovery when output approaches the rails

The LMH6657/6658 output is exceedingly well-behaved when it comes to recovering from an overload condition. As can be seen from Figure 55 below, the LMH6657/6658 will typically recover from an output overload condition in about 18ns, regardless of the duration of the overload.

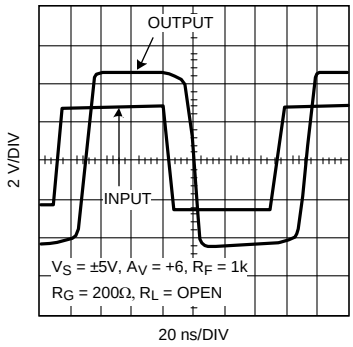


Figure 55.

OUTPUT PHASE REVERSAL

This is a problem with some operational amplifiers. This effect is caused by phase reversal in the input stage due to saturation of one or more of the transistors when the inputs exceed the normal expected range of voltages. Some applications, such as servo control loops among others, are sensitive to this kind of behavior and would need special safeguards to ensure proper functioning. The LMH6657/6658 is immune to output phase reversal with input overload. With inputs exceeded, the LMH6657/6658 output will stay at the clamped voltage from the supply rail. Exceeding the input supply voltages beyond the Absolute Maximum Ratings of the device could however damage or otherwise adversely effect the reliability or life of the device.

DRIVING CAPACITIVE LOADS

The LMH6657/6658 can drive moderate values of capacitance by utilizing a series isolation resistor between the output and the capacitive load. Typical Performance Characteristics section shows the settling time behavior for various capacitive loads and 20Ω of isolation resistance. Capacitive load tolerance will improve with higher closed loop gain values. Applications such as ADC buffers, among others, present complex and varying capacitive loads to the Op Amp; best value for this isolation resistance is often found by experimentation and actual trial and error for each application.

DISTORTION

Applications with demanding distortion performance requirements are best served with the device operating in the inverting mode. The reason for this is that in the inverting configuration, the input common mode voltage does not vary with the signal and there is no subsequent ill effects due to this shift in operating point and the possibility of additional non-linearity. Moreover, under low closed loop gain settings (most suited to low distortion), the non-inverting configuration is at a further disadvantage of having to contend with the input common voltage range. There is also a strong relationship between output loading and distortion performance (i.e. 1kΩ vs. 100Ω distortion improves by about 20dB @100KHz) especially at the lower frequency end where the distortion tends to be lower. At higher frequency, this dependence diminishes greatly such that this difference is only about 4dB at 10MHz. But, in general, lighter output load leads to reduced HD3 term and thus improves THD.

PRINTED CIRCUIT BOARD LAYOUT AND COMPONENT VALUES SECTIONS

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board PN
LMH6657MF	SOT-23-5	CLC730068
LMH6657MG	SC-70	NA
LMH6658MA	8-Pin SOIC	CLC730036
LMH6658MM	8-Pin VSSOP	CLC730123

These free evaluation boards are shipped when a device sample request is placed with Texas Instruments. Another important parameter in working with high speed/high performance amplifiers, is the component values selection. Choosing external resistors that are large in value will effect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower, will diminish this interaction to a large extent. On the other hand, choosing very low value resistors will load down nodes and will contribute to higher overall power dissipation.

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6657MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A85A	Samples
LMH6657MFX	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A85A	Samples
LMH6657MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A85A	Samples
LMH6657MG	ACTIVE	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	A76	Samples
LMH6657MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A76	Samples
LMH6657MGX	ACTIVE	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 85	A76	Samples
LMH6657MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A76	Samples
LMH6658MA	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMH66 58MA	Samples
LMH6658MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 58MA	Samples
LMH6658MAX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMH66 58MA	Samples
LMH6658MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 58MA	Samples
LMH6658MM	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	A88A	Samples
LMH6658MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A88A	Samples
LMH6658MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 85	A88A	Samples
LMH6658MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A88A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

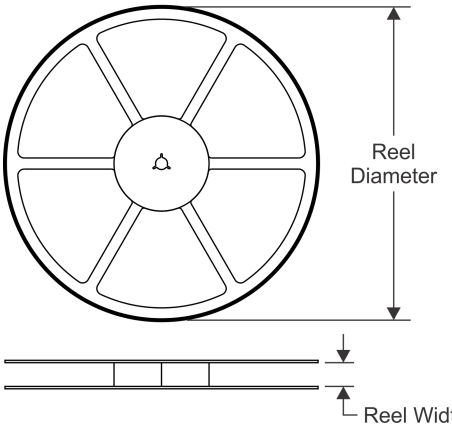
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

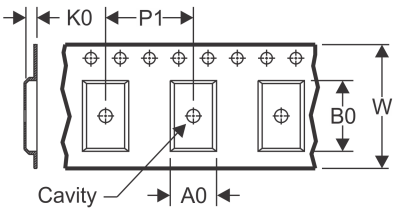
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

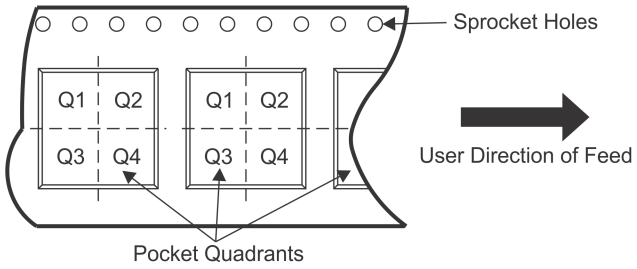


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

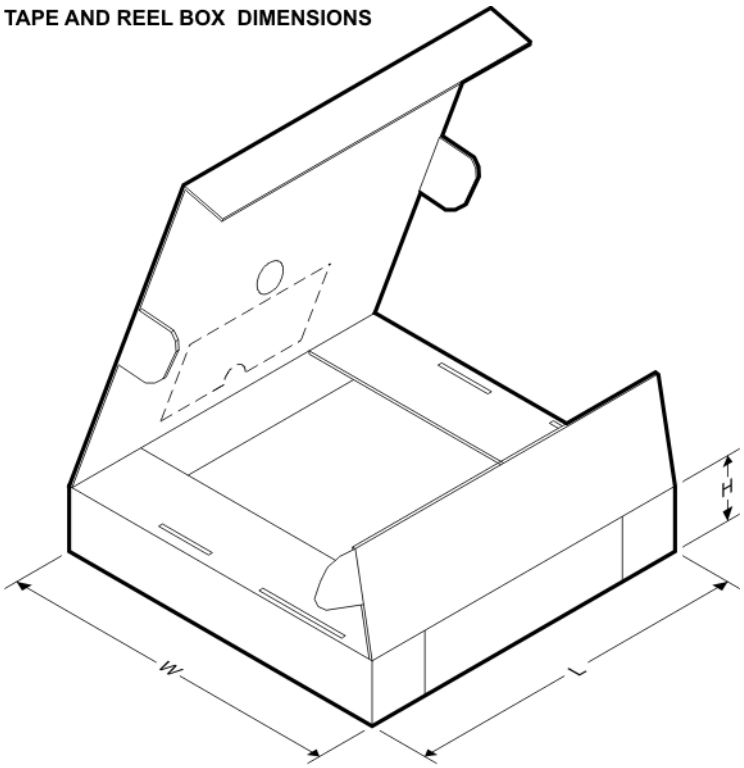
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6657MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6657MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6657MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6657MG	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMH6657MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMH6657MGX	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMH6657MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMH6658MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6658MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6658MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6658MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6658MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6658MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

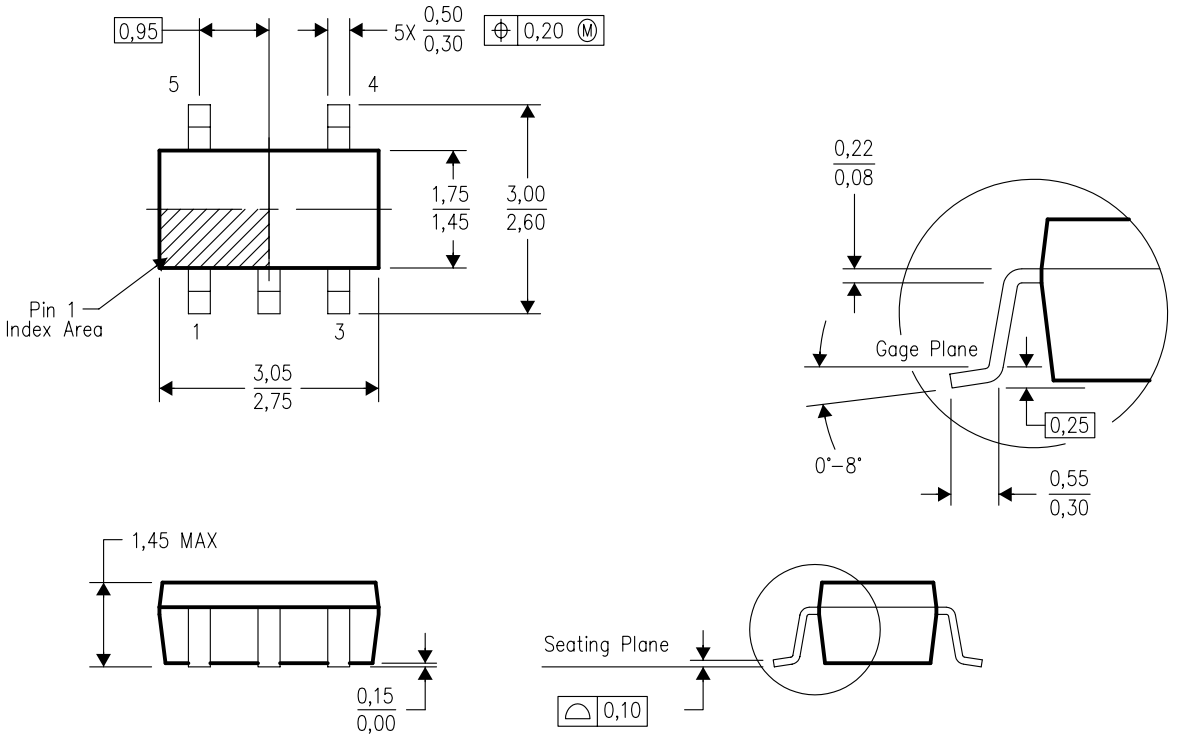
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6657MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6657MFX	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6657MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6657MG	SC70	DCK	5	1000	210.0	185.0	35.0
LMH6657MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMH6657MGX	SC70	DCK	5	3000	210.0	185.0	35.0
LMH6657MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMH6658MAX	SOIC	D	8	2500	367.0	367.0	35.0
LMH6658MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6658MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMH6658MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMH6658MMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMH6658MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

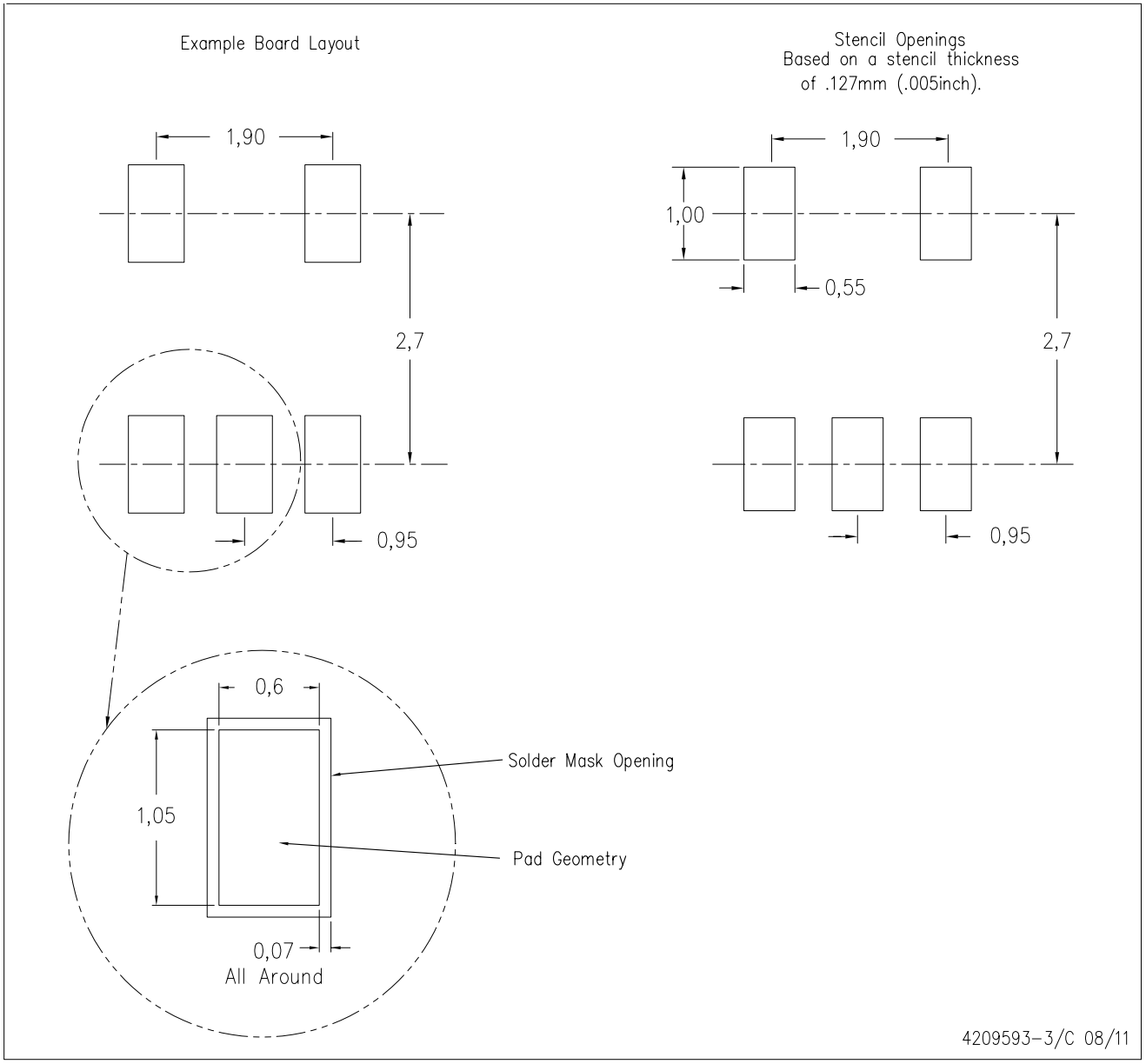
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

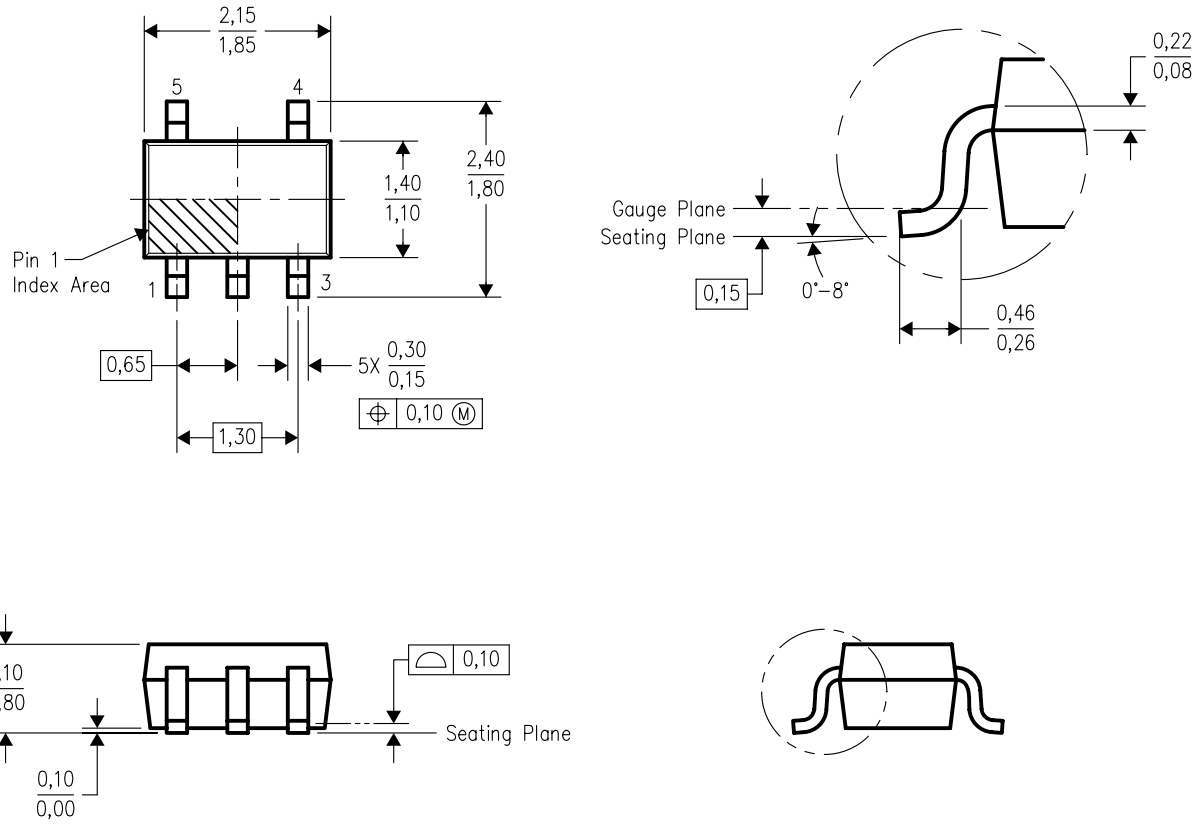
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

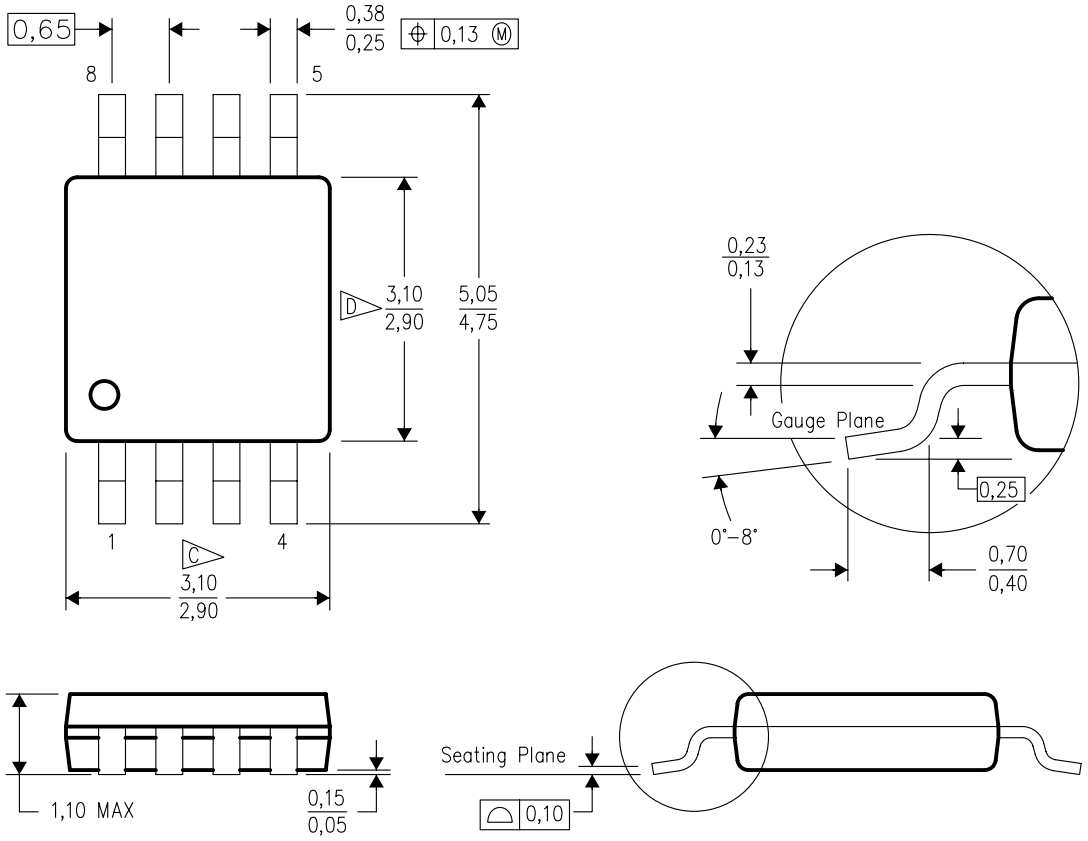
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

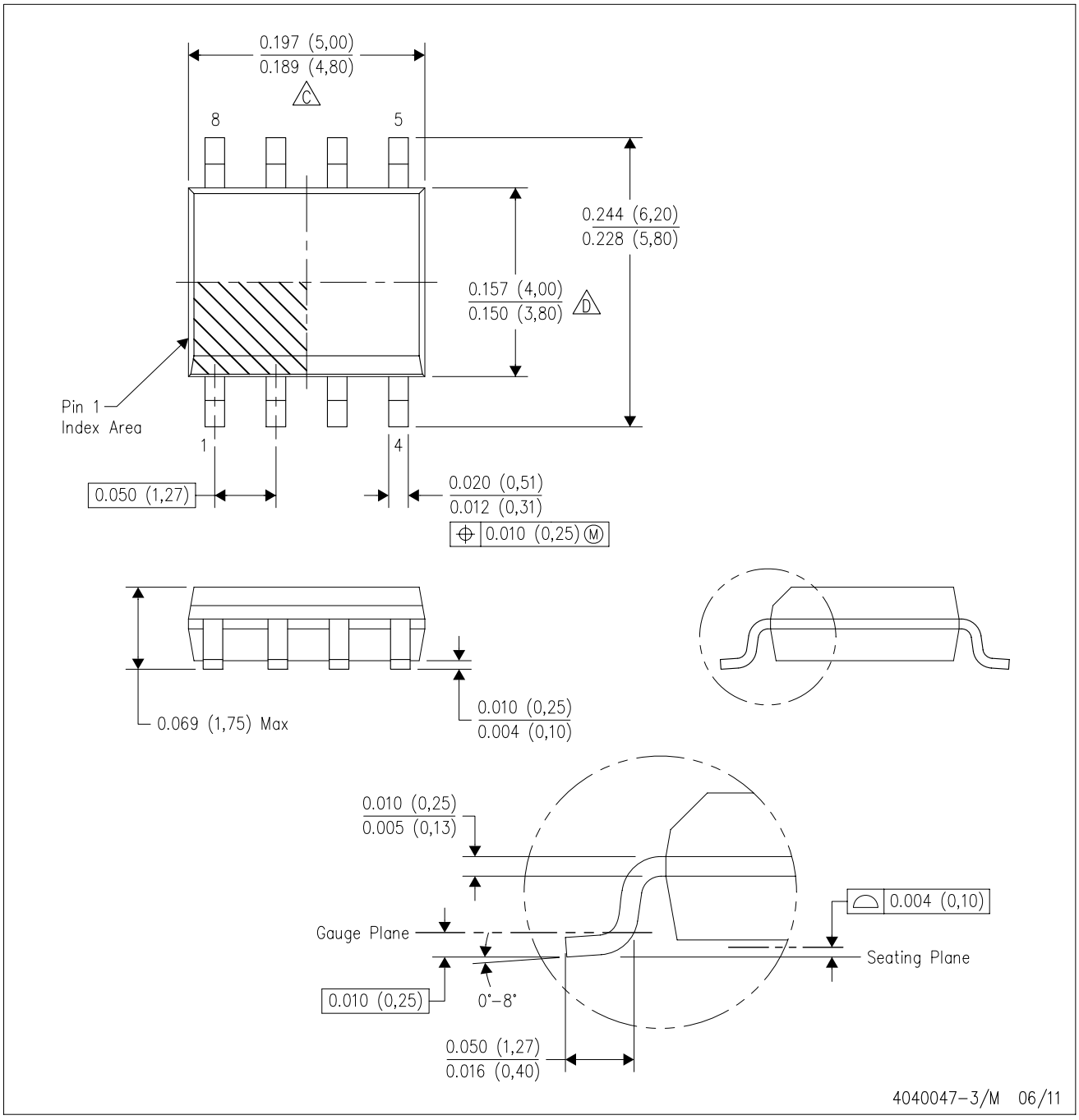
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265