

## LMV821/LMV821-Q1/LMV822/LMV822-Q1/LMV824/LMV824-Q1 Single/Dual/Quad Low Voltage, Low Power, R-to-R Output, 5 MHz Op Amps

Check for Samples: [LMV821-N](#), [LMV821-N-Q1](#), [LMV822-N](#), [LMV822-N-Q1](#), [LMV824-N](#), [LMV824-N-Q1](#)

### FEATURES

- (For Typical, 5 V Supply Values; Unless Otherwise Noted)
- LMV821-N/LMV822-N/LMV824-N are available in Automotive AEC-Q100 Grade 1 versions
- Ultra Tiny, SC70-5 Package 2.0 x 2.0 x 1.0 mm
- Guaranteed 2.5 V, 2.7 V and 5 V Performance
- Maximum VOS 3.5 mV (Guaranteed)
- VOS Temp. Drift 1  $\mu\text{V}/^\circ\text{C}$
- GBW product @ 2.7 V 5 MHz
- $I_{\text{Supply}}$  @ 2.7 V 220  $\mu\text{A}/\text{Amplifier}$
- Minimum SR 1.4 V/us (Guaranteed)
- CMRR 90 dB
- PSRR 85 dB
- $V_{\text{CM}}$  @ 5V -0.3V to 4.3V
- Rail-to-Rail (R-to-R) Output Swing
- @ 600  $\Omega$  Load 160 mV from rail
- @ 10 k $\Omega$  Load 55 mV from rail
- Stable with High Capacitive Loads (Refer to Application Section)

### APPLICATIONS

- Cordless Phones
- Cellular Phones
- Laptops
- PDAs
- PCMCIA

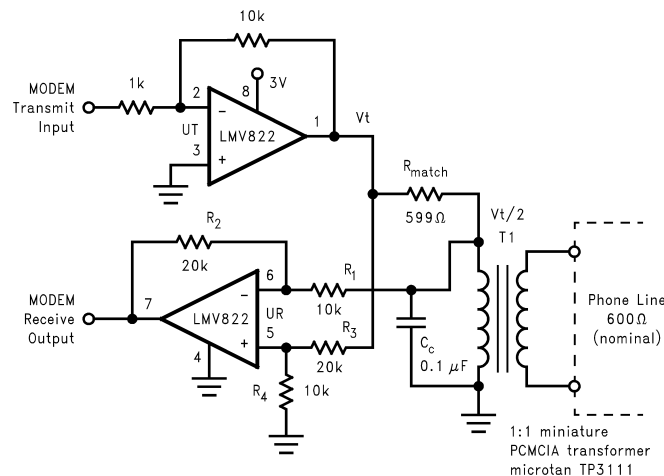
### DESCRIPTION

The LMV821/LMV822/LMV824 bring performance and economy to low voltage / low power systems. With a 5 MHz unity-gain frequency and a guaranteed 1.4 V/ $\mu\text{s}$  slew rate, the quiescent current is only 220  $\mu\text{A}/\text{amplifier}$  (2.7 V). They provide rail-to-rail (R-to-R) output swing into heavy loads (600  $\Omega$  Guarantees). The input common-mode voltage range includes ground, and the maximum input offset voltage is 3.5mV (Guaranteed). They are also capable of comfortably driving large capacitive loads (refer to the application notes section).

The LMV821 (single) is available in the ultra tiny SC70-5 package, which is about half the size of the previous title holder, the SOT23-5.

Overall, the LMV821/LMV822/LMV824 (Single/Dual/Quad) are low voltage, low power, performance op amps, that can be designed into a wide range of applications, at an economical price.

### Telephone-line Transceiver for a PCMCIA Modem Card



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)</sup>

ESD Tolerance <sup>(3)</sup>	
Machine Model	100V
Human Body Model	
LMV822/824	2000V
LMV821	1500V
Differential Input Voltage	± Supply Voltage
Supply Voltage (V <sup>+</sup> –V <sup>-</sup> )	5.5V
Output Short Circuit to V <sup>+</sup> <sup>(4)</sup>	
Output Short Circuit to V <sup>-</sup> <sup>(4)</sup>	
Soldering Information	
Infrared or Convection (20 sec)	235°C
Storage Temperature Range	-65°C to 150°C
Junction Temperature <sup>(5)</sup>	150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Human body model, 1.5 kΩ in series with 100 pF. Machine model, 200Ω in series with 100 pF.
- (4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.
- (5) The maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub>–T<sub>A</sub>)/θ<sub>JA</sub>. All numbers apply for packages soldered directly into a PC board.

### Operating Ratings<sup>(1)</sup>

Supply Voltage	2.5V to 5.5V
Temperature Range	
LMV821, LMV822, LMV824	-40°C ≤T <sub>J</sub> ≤85°C
Thermal Resistance (θ <sub>JA</sub> )	
Ultra Tiny SC70-5 Package, 5-Pin Surface Mount	440 °C/W
Tiny SOT23-5 Package, 5-Pin Surface Mount	265 °C/W
SOIC Package, 8-Pin Surface Mount	190 °C/W
VSSOP Package, 8-Pin Mini Surface Mount	235 °C/W
SOIC Package, 14-Pin Surface Mount	145 °C/W
TSSOP Package, 14-Pin	155 °C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

## 2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.0\text{V}$ ,  $V_O = 1.35\text{V}$  and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (1)	LMV821/822/824 Limit (2)	Units	
$V_{\text{OS}}$	Input Offset Voltage		1	3.5	mV	
				<b>4</b>	max	
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Average Drift		1		$\mu\text{V}/^\circ\text{C}$	
$I_B$	Input Bias Current		30	90	nA	
				<b>140</b>	max	
$I_{\text{OS}}$	Input Offset Current		0.5	30	nA	
				<b>50</b>	max	
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 1.7\text{V}$	85	70	dB	
				<b>68</b>	min	
+PSRR	Positive Power Supply Rejection Ratio	$1.7\text{V} \leq V^+ \leq 4\text{V}$ , $V^- = 1\text{V}$ , $V_O = 0\text{V}$ , $V_{\text{CM}} = 0\text{V}$	85	75	dB	
-PSRR	Negative Power Supply Rejection Ratio	$-1.0\text{V} \leq V^- \leq -3.3\text{V}$ , $V^+ = 1.7\text{V}$ , $V_O = 0\text{V}$ , $V_{\text{CM}} = 0\text{V}$	85	73	dB	
				<b>70</b>	min	
$V_{\text{CM}}$	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{dB}$	-0.3	-0.2	V	
					max	
			2.0	1.9	V	
$A_V$	Large Signal Voltage Gain	Sourcing, $R_L = 600\Omega$ to $1.35\text{V}$ , $V_O = 1.35\text{V}$ to $2.2\text{V}$	100	90	dB	
				<b>85</b>	min	
			Sinking, $R_L = 600\Omega$ to $1.35\text{V}$ , $V_O = 1.35\text{V}$ to $0.5\text{V}$	90	85	dB
				<b>80</b>	min	
			Sourcing, $R_L = 2\text{k}\Omega$ to $1.35\text{V}$ , $V_O = 1.35\text{V}$ to $2.2\text{V}$	100	95	dB
	<b>90</b>	min				
$V_O$	Output Swing	$V^+ = 2.7\text{V}$ , $R_L = 600\Omega$ to $1.35\text{V}$	2.58	2.50	V	
				<b>2.40</b>	min	
			0.13	0.20	V	
				<b>0.30</b>	max	
			$V^+ = 2.7\text{V}$ , $R_L = 2\text{k}\Omega$ to $1.35\text{V}$	2.66	2.60	V
	<b>2.50</b>	min				
$I_O$	Output Current	Sourcing, $V_O = 0\text{V}$	16	12	mA	
					min	
			Sinking, $V_O = 2.7\text{V}$	26	12	mA
$I_S$	Supply Current	LMV821 (Single)	0.22	0.3	mA	
				<b>0.5</b>	max	
		LMV822 (Dual)	0.45	0.6	mA	
				<b>0.8</b>	max	
		LMV824 (Quad)	0.72	1.0	mA	
	<b>1.2</b>	max				

(1) Typical Values represent the most likely parametric norm.

(2) All limits are guaranteed by testing or statistical analysis.

## 2.5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.0\text{V}$ ,  $V_O = 1.25\text{V}$  and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (1)	LMV821/822/824 Limit (2)	Units
$V_{\text{OS}}$	Input Offset Voltage		1	3.5	mV
				<b>4</b>	max
$V_O$	Output Swing	$V^+ = 2.5\text{V}$ , $R_L = 600\Omega$ to $1.25\text{V}$	2.37	2.30	V
				<b>2.20</b>	min
			0.13	0.20	V
		$V^+ = 2.5\text{V}$ , $R_L = 2\text{k}\Omega$ to $1.25\text{V}$	2.46	2.40	V
				<b>2.30</b>	min
			0.08	0.12	V
			<b>0.20</b>	max	

- (1) Typical Values represent the most likely parametric norm.  
(2) All limits are guaranteed by testing or statistical analysis.

## 2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.0\text{V}$ ,  $V_O = 1.35\text{V}$  and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMV821/822/824 Limit (2)	Units
SR	Slew Rate	(3)	1.5		V/ $\mu\text{s}$
GBW	Gain-Bandwidth Product		5		MHz
$\Phi_m$	Phase Margin		61		Deg.
$G_m$	Gain Margin		10		dB
	Amp-to-Amp Isolation	(4)	135		dB
$e_n$	Input-Related Voltage Noise	$f = 1\text{kHz}$ , $V_{\text{CM}} = 1\text{V}$	28		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$f = 1\text{kHz}$	0.1		pA/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{kHz}$ , $A_V = -2$ , $R_L = 10\text{k}\Omega$ , $V_O = 4.1\text{V}_{\text{PP}}$	0.01		%

- (1) Typical Values represent the most likely parametric norm.  
(2) All limits are guaranteed by testing or statistical analysis.  
(3)  $V^+ = 5\text{V}$ . Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.  
(4) Input referred,  $V^+ = 5\text{V}$  and  $R_L = 100\text{k}\Omega$  connected to 2.5V. Each amp excited in turn with 1 kHz to produce  $V_O = 3\text{V}_{\text{PP}}$ .

## 5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 2.0\text{V}$ ,  $V_O = 2.5\text{V}$  and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (1)	LMV821/822/824 Limit (2)	Units
$V_{\text{OS}}$	Input Offset Voltage		1	3.5	mV
				<b>4.0</b>	max
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Average Drift		1		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current		40	100	nA
				<b>150</b>	max
$I_{\text{OS}}$	Input Offset Current		0.5	30	nA
				<b>50</b>	max

- (1) Typical Values represent the most likely parametric norm.  
(2) All limits are guaranteed by testing or statistical analysis.

**5V DC Electrical Characteristics (continued)**

 Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 2.0\text{V}$ ,  $V_O = 2.5\text{V}$  and  $R_L > 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (1)	LMV821/822/824 Limit (2)	Units		
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 4.0\text{V}$	90	72	dB		
				<b>70</b>	min		
+PSRR	Positive Power Supply Rejection Ratio	$1.7\text{V} \leq V^+ \leq 4\text{V}$ , $V^- = 1\text{V}$ , $V_O = 0\text{V}$ , $V_{\text{CM}} = 0\text{V}$	85	75	dB		
				<b>70</b>	min		
-PSRR	Negative Power Supply Rejection Ratio	$-1.0\text{V} \leq V^- \leq -3.3\text{V}$ , $V^+ = 1.7\text{V}$ , $V_O = 0\text{V}$ , $V_{\text{CM}} = 0\text{V}$	85	73	dB		
				<b>70</b>	min		
$V_{\text{CM}}$	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{dB}$	-0.3	-0.2	V		
						max	
				4.3	4.2	V	
						min	
$A_V$	Large Signal Voltage Gain	Sourcing, $R_L = 600\Omega$ to $2.5\text{V}$ , $V_O = 2.5$ to $4.5\text{V}$	105	95	dB		
				<b>90</b>	min		
				Sinking, $R_L = 600\Omega$ to $2.5\text{V}$ , $V_O = 2.5$ to $0.5\text{V}$	105	95	dB
						<b>90</b>	min
		Sourcing, $R_L = 2\text{k}\Omega$ to $2.5\text{V}$ , $V_O = 2.5$ to $4.5\text{V}$	105	95	dB		
				<b>90</b>	min		
				Sinking, $R_L = 2\text{k}\Omega$ to $2.5$ , $V_O = 2.5$ to $0.5\text{V}$	105	95	dB
						<b>90</b>	min
$V_O$	Output Swing	$V^+ = 5\text{V}$ , $R_L = 600\Omega$ to $2.5\text{V}$	4.84	4.75	V		
				<b>4.70</b>	min		
				0.17	0.250	V	
						<b>.30</b>	max
		$V^+ = 5\text{V}$ , $R_L = 2\text{k}\Omega$ to $2.5\text{V}$	4.90	4.85	V		
				<b>4.80</b>	min		
				0.10	0.15	V	
						<b>0.20</b>	max
$I_O$	Output Current	Sourcing, $V_O = 0\text{V}$	45	20	mA		
				<b>15</b>	min		
		Sinking, $V_O = 5\text{V}$	40	20	mA		
				<b>15</b>	min		
$I_S$	Supply Current	LMV821 (Single)	0.30	0.4	mA		
				<b>0.6</b>	max		
		LMV822 (Dual)	0.5	0.7	mA		
				<b>0.9</b>	max		
		LMV824 (Quad)	1.0	1.3	mA		
				<b>1.5</b>	max		

### 5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = 2\text{V}$ ,  $V_O = 2.5\text{V}$  and  $R_L > 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMV821/822/824 Limit (2)	Units
SR	Slew Rate	(3)	2.0	1.4	V/ $\mu\text{s}$ min
GBW	Gain-Bandwidth Product		5.6		MHz
$\Phi_m$	Phase Margin		67		Deg.
$G_m$	Gain Margin		15		dB
	Amp-to-Amp Isolation	(4)	135		dB
$e_n$	Input-Related Voltage Noise	$f = 1\text{ kHz}$ , $V_{CM} = 1\text{V}$	24		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$f = 1\text{ kHz}$	0.25		pA/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{ kHz}$ , $A_V = -2$ , $R_L = 10\text{ k}\Omega$ , $V_O = 4.1\text{ V}_{PP}$	0.01		%

(1) Typical Values represent the most likely parametric norm.

(2) All limits are guaranteed by testing or statistical analysis.

(3)  $V^+ = 5\text{V}$ . Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.

(4) Input referred,  $V^+ = 5\text{V}$  and  $R_L = 100\text{k}\Omega$  connected to 2.5V. Each amp excited in turn with 1 kHz to produce  $V_O = 3\text{ V}_{PP}$ .

### Typical Performance Characteristics

Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .

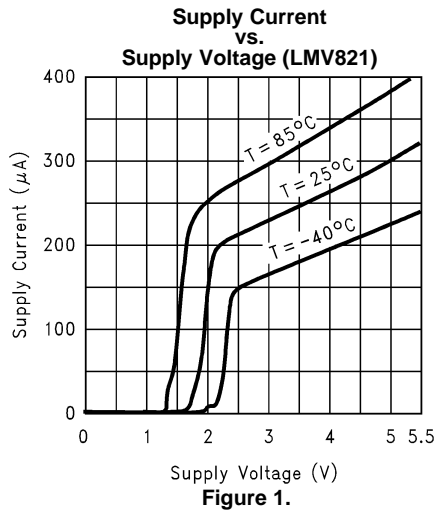


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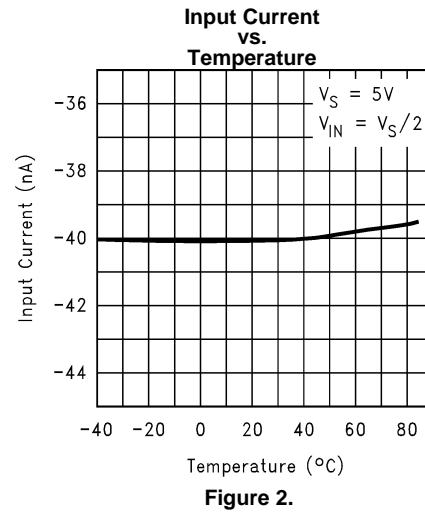


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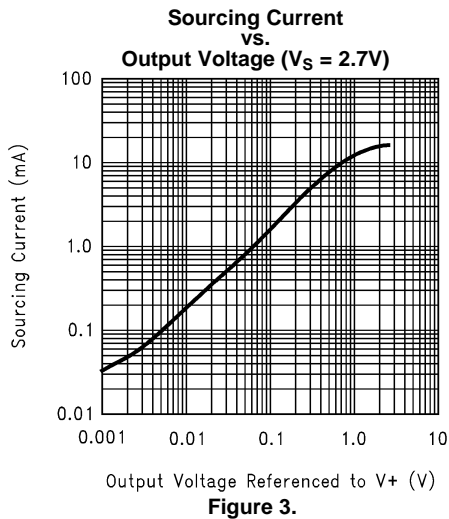


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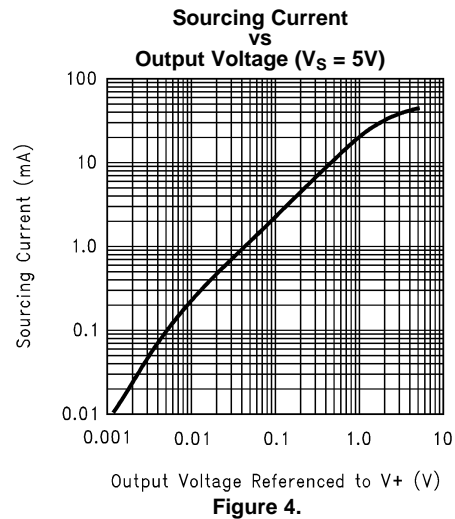


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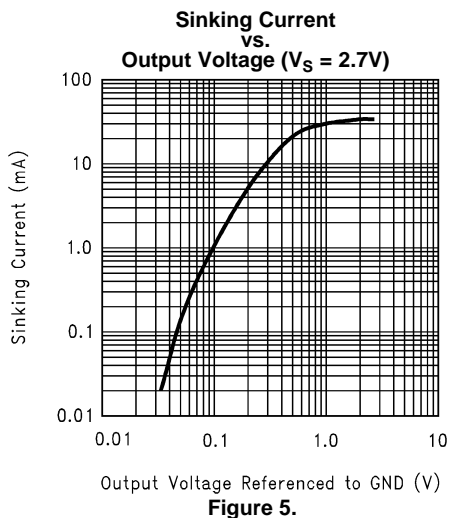


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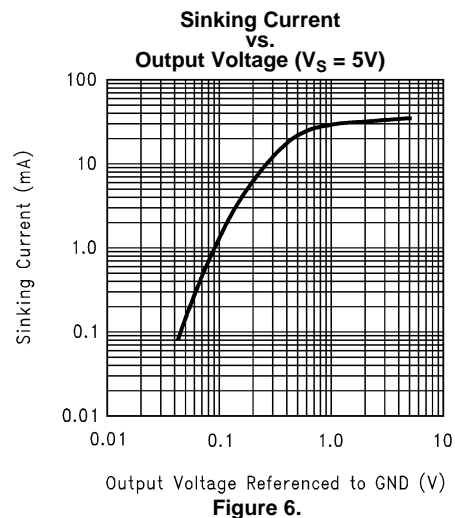


Figure 6.

Typical Performance Characteristics (continued)

Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .

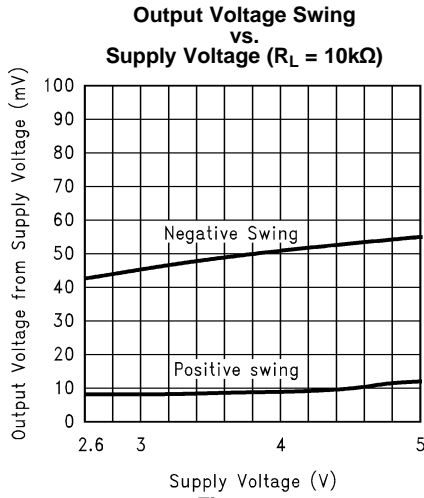


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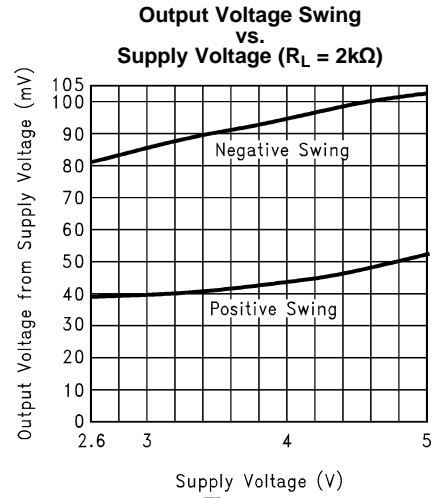


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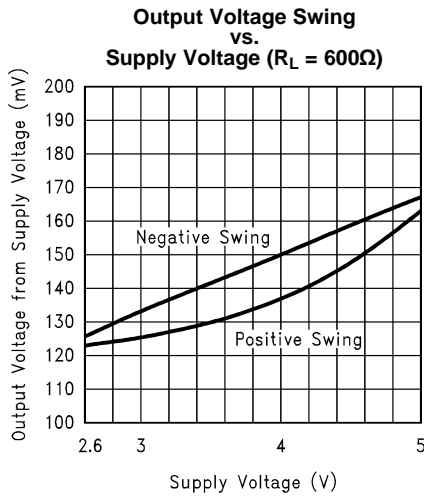


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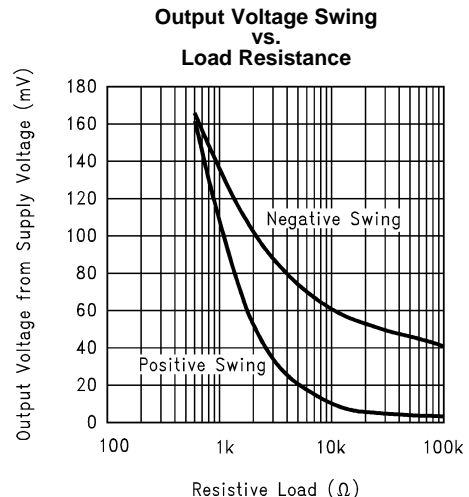


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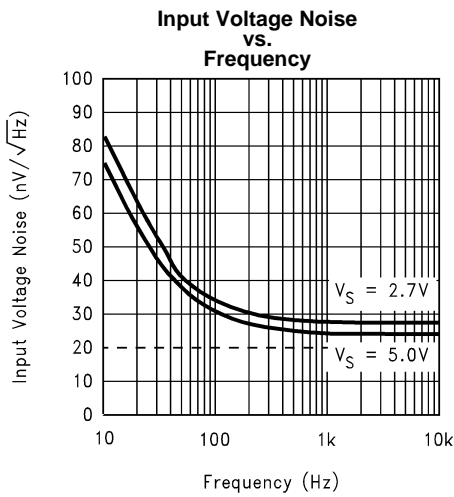


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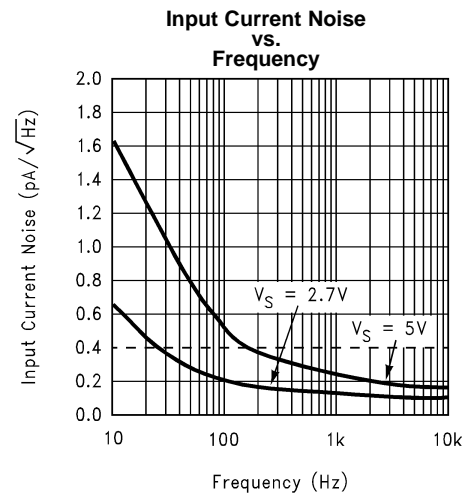


Figure 12.



Typical Performance Characteristics (continued)

Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .

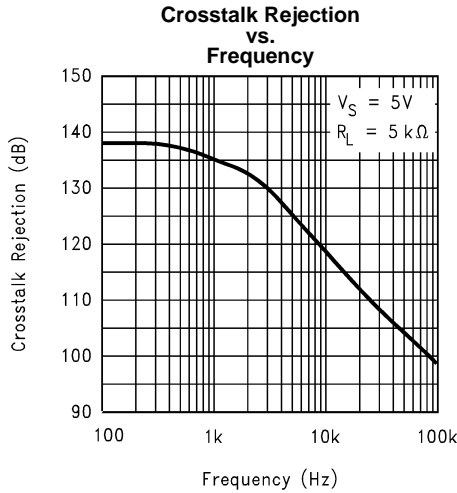


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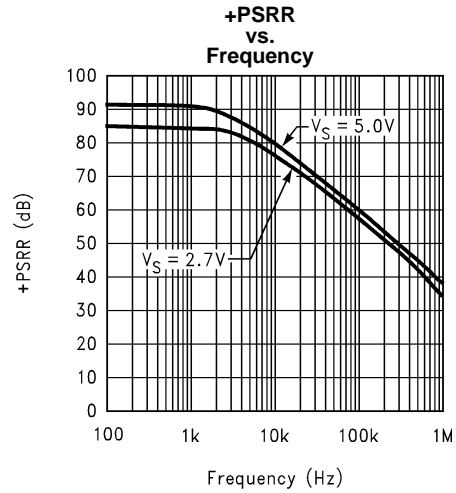


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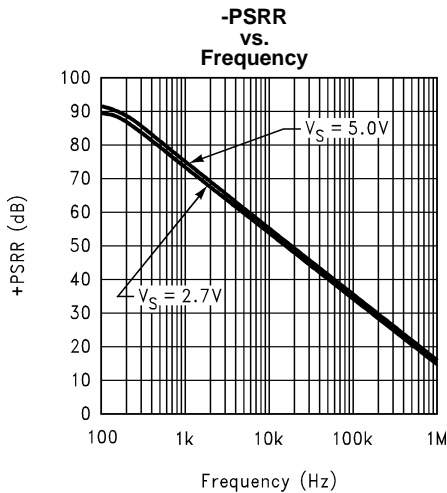


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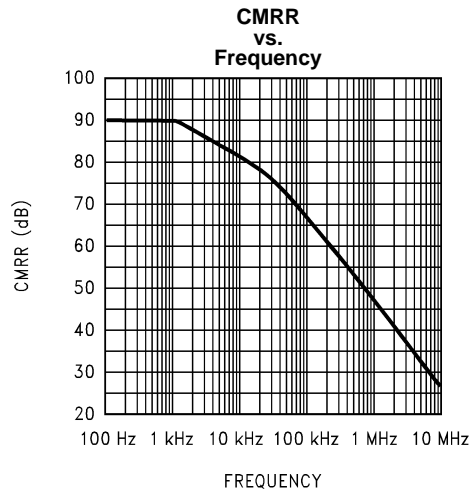


Figure 16.

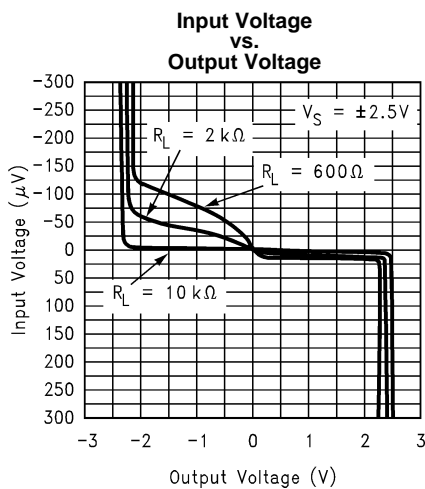


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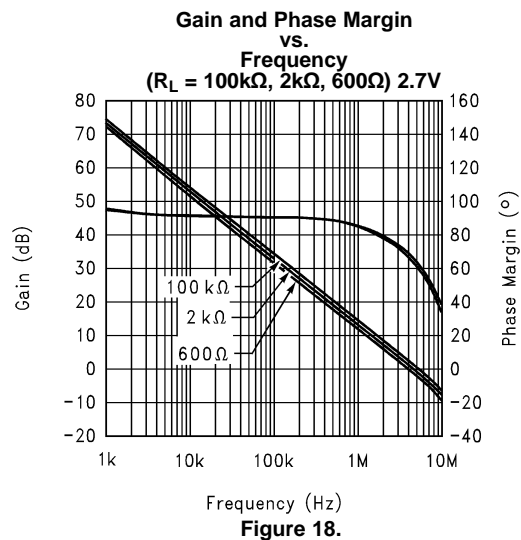
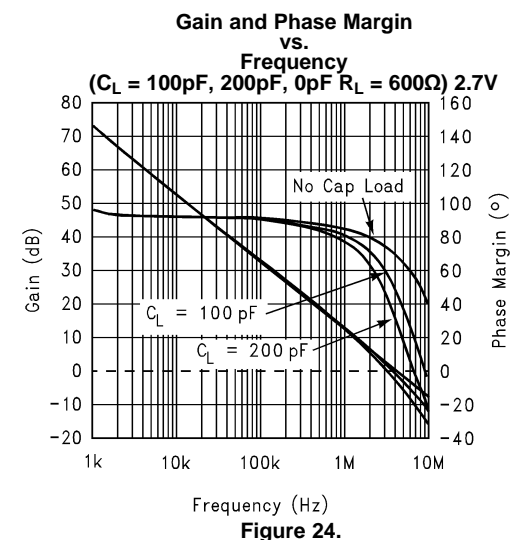
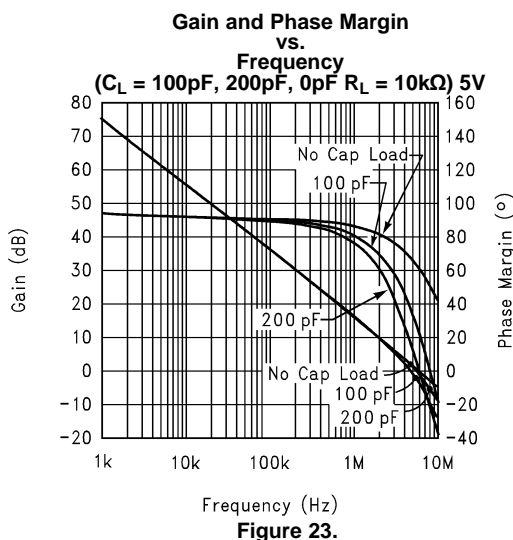
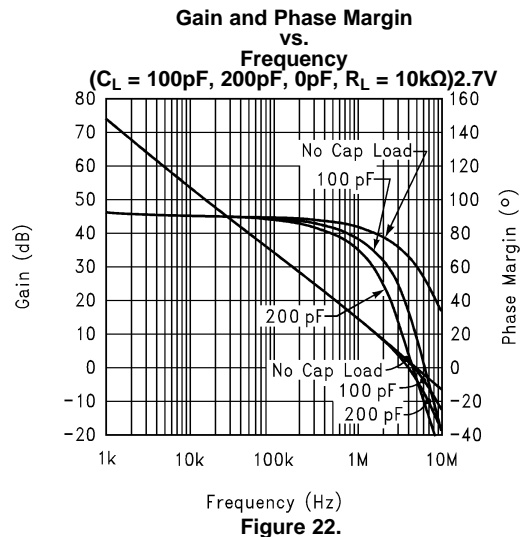
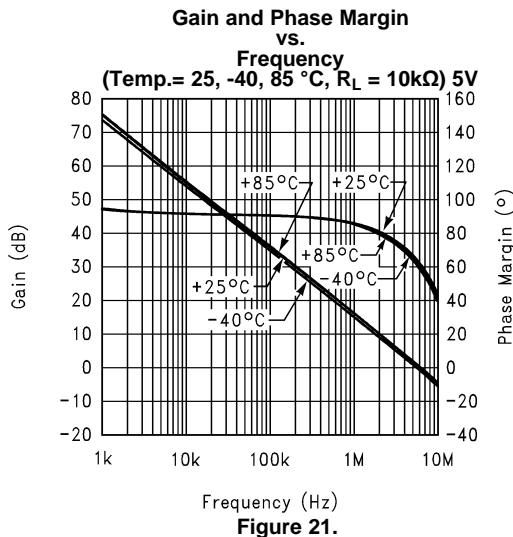
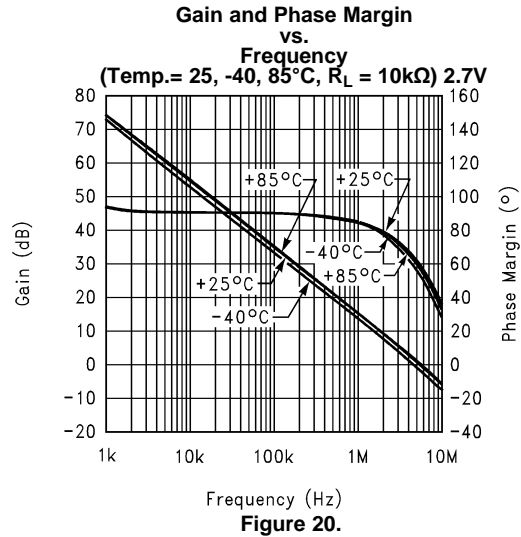
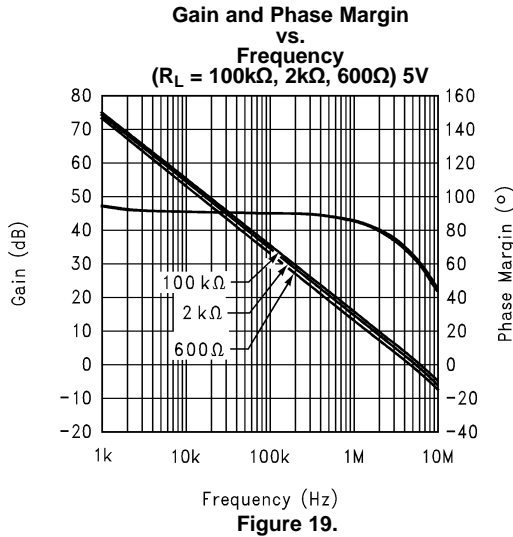


Figure 18.

Typical Performance Characteristics (continued)

Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .



Typical Performance Characteristics (continued)

Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .

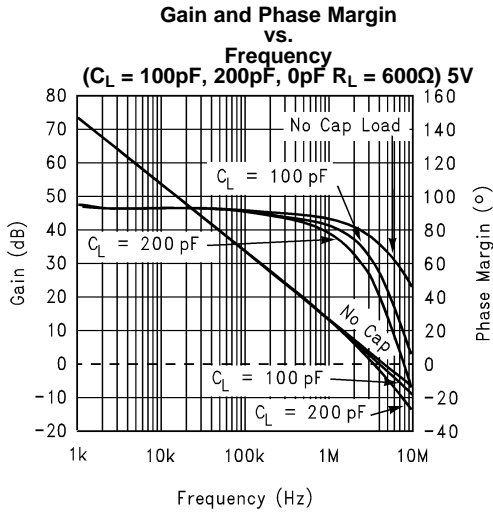


Figure 25.

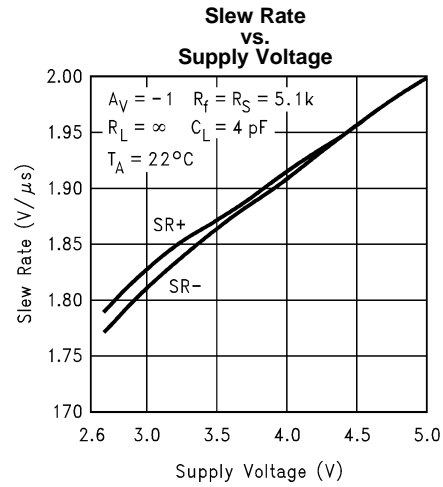


Figure 26.

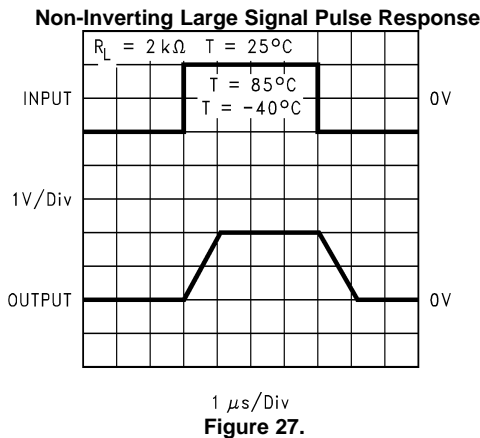


Figure 27.

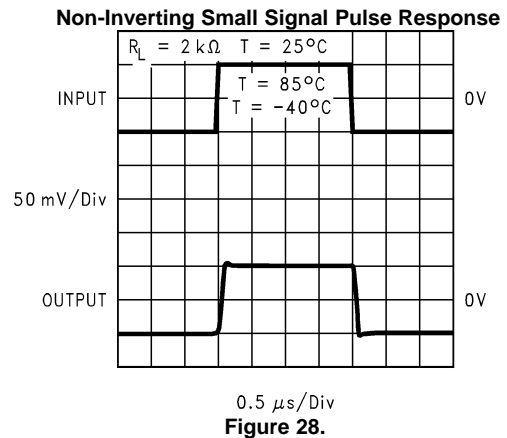


Figure 28.

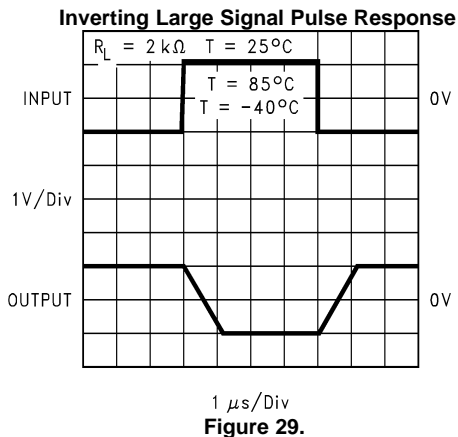


Figure 29.

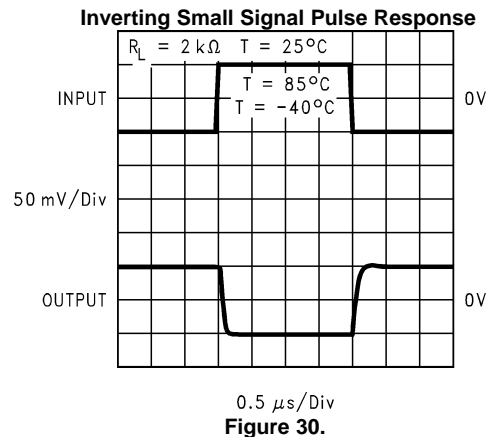
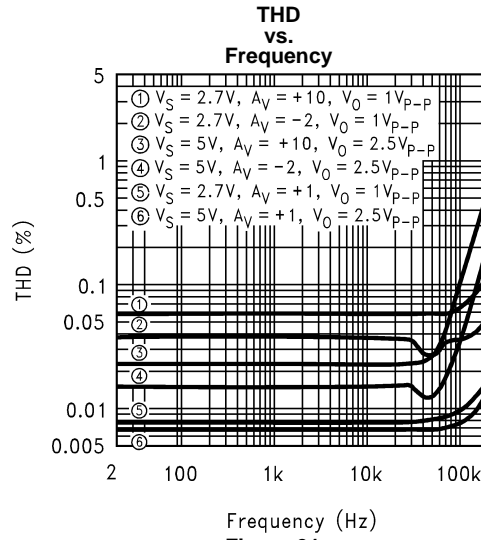


Figure 30.

**Typical Performance Characteristics (continued)**

Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .



## APPLICATION NOTE

This application note is divided into two sections: design considerations and Application Circuits.

### DESIGN CONSIDERATIONS

This section covers the following design considerations:

1. Frequency and Phase Response Considerations
2. Unity-Gain Pulse Response Considerations
3. Input Bias Current Considerations

### FREQUENCY AND PHASE RESPONSE CONSIDERATIONS

The relationship between open-loop frequency response and open-loop phase response determines the closed-loop stability performance (negative feedback). The open-loop phase response causes the feedback signal to shift towards becoming positive feedback, thus becoming unstable. The further the output phase angle is from the input phase angle, the more stable the negative feedback will operate. Phase Margin ( $\phi_m$ ) specifies this output-to-input phase relationship at the unity-gain crossover point. Zero degrees of phase-margin means that the input and output are completely in phase with each other and will sustain oscillation at the unity-gain frequency.

The AC tables show  $\phi_m$  for a no load condition. But  $\phi_m$  changes with load. The Gain and Phase margin vs Frequency plots in the curve section can be used to graphically determine the  $\phi_m$  for various loaded conditions. To do this, examine the phase angle portion of the plot, find the phase margin point at the unity-gain frequency, and determine how far this point is from zero degree of phase-margin. The larger the phase-margin, the more stable the circuit operation.

The bandwidth is also affected by load. The graphs of [Figure 32](#) and [Figure 33](#) provide a quick look at how various loads affect the  $\phi_m$  and the bandwidth of the LMV821/822/824 family. These graphs show capacitive loads reducing both  $\phi_m$  and bandwidth, while resistive loads reduce the bandwidth but increase the  $\phi_m$ . Notice how a 600 $\Omega$  resistor can be added in parallel with 220 picofarads capacitance, to increase the  $\phi_m$  20°(approx.), but at the price of about a 100 kHz of bandwidth.

Overall, the LMV821/822/824 family provides good stability for loaded condition.

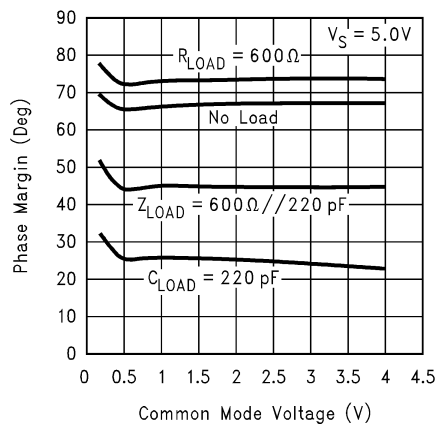


Figure 32. Phase Margin vs Common Mode Voltage for Various Loads

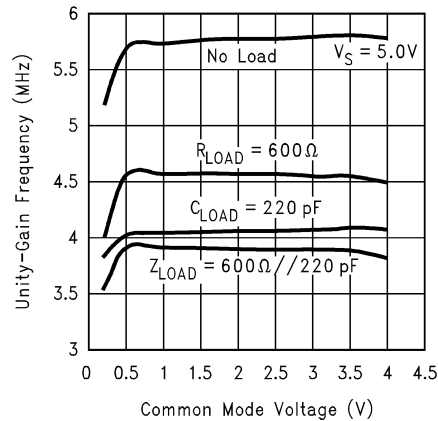


Figure 33. Unity-Gain Frequency vs Common Mode Voltage for Various Loads

### UNITY GAIN PULSE RESPONSE CONSIDERATION

A pull-up resistor is well suited for increasing unity-gain, pulse response stability. For example, a 600  $\Omega$  pull-up resistor reduces the overshoot voltage by about 50%, when driving a 220 pF load. Figure 34 shows how to implement the pull-up resistor for more pulse response stability.

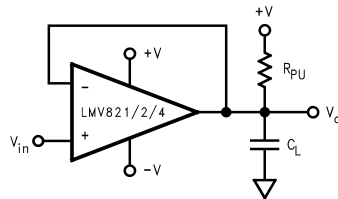


Figure 34. Using a Pull-up Resistor at the Output for Stabilizing Capacitive Loads

Higher capacitances can be driven by decreasing the value of the pull-up resistor, but its value shouldn't be reduced beyond the sinking capability of the part. An alternate approach is to use an isolation resistor as illustrated in Figure 35.

Figure 36 shows the resulting pulse response from a LMV824, while driving a 10,000 pF load through a 20  $\Omega$  isolation resistor.

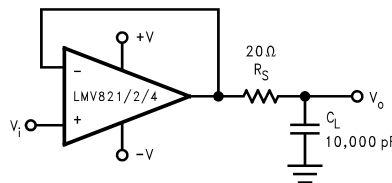


Figure 35. Using an Isolation Resistor to Drive Heavy Capacitive Loads

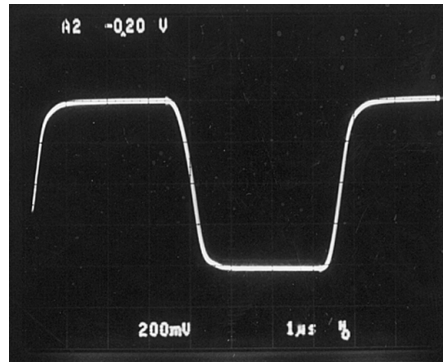


Figure 36. Pulse Response per Figure 35

## INPUT BIAS CURRENT CONSIDERATION

Input bias current ( $I_B$ ) can develop a somewhat significant offset voltage. This offset is primarily due to  $I_B$  flowing through the negative feedback resistor,  $R_F$ . For example, if  $I_B$  is 90 nA (max @ room) and  $R_F$  is 100 k $\Omega$ , then an offset of 9 mV will be developed ( $V_{OS} = I_B \times R_F$ ). Using a compensation resistor ( $R_C$ ), as shown in Figure 37, cancels out this affect. But the input offset current ( $I_{OS}$ ) will still contribute to an offset voltage in the same manner - typically 0.05 mV at room temp.

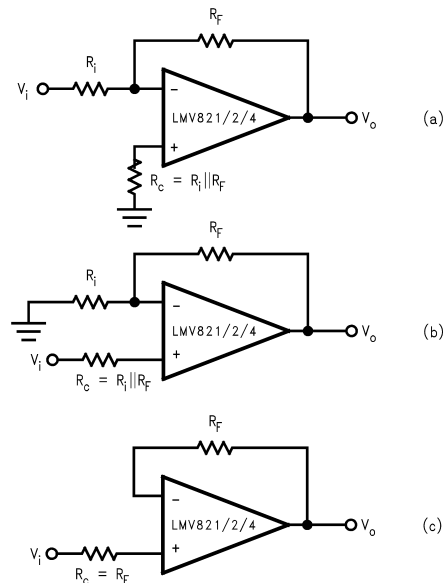


Figure 37. Canceling the Voltage Offset Effect of Input Bias Current

## APPLICATION CIRCUITS

This section covers the following application circuits:

1. Telephone-Line Transceiver
2. "Simple" Mixer (Amplitude Modulator)
3. Dual Amplifier Active Filters (DAAFs)
  - a. Low-Pass Filter (LPF)
  - b. High-Pass Filter (HPF)
4. Tri-level Voltage Detector

## TELEPHONE-LINE TRANSCEIVER

The telephone-line transceiver of Figure 38 provides a full-duplexed connection through a PCMCIA, miniature transformer. The differential configuration of receiver portion (UR), cancels reception from the transmitter portion (UT). Note that the input signals for the differential configuration of UR, are the transmit voltage ( $V_T$ ) and  $V_T/2$ . This is because  $R_{match}$  is chosen to match the coupled telephone-line impedance; therefore dividing  $V_T$  by two (assuming  $R_1 \gg R_{match}$ ). The differential configuration of UR has its resistors chosen to cancel the  $V_T$  and  $V_T/2$  inputs according to the following equation:

$$V_0 = V_T \left( \frac{R_4}{R_3 + R_4} \right) \left( 1 + \frac{R_2}{R_1} \right) - \frac{V_T}{2} \left( \frac{R_2}{R_1} \right) = V_T \frac{1}{3} (3) - \frac{V_T}{2} (2) = 0 \quad (1)$$

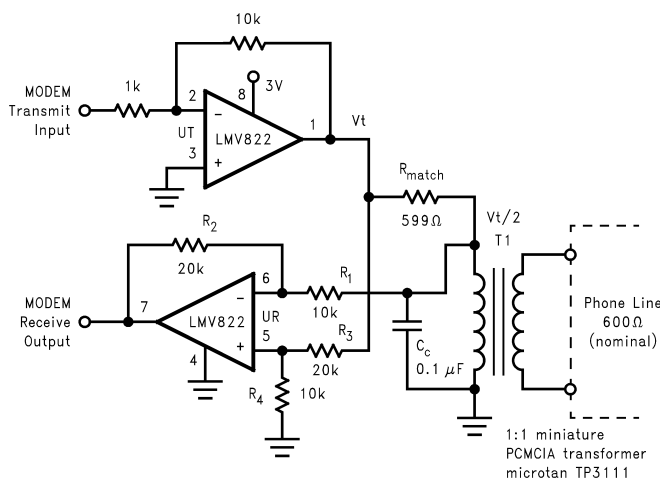


Figure 38. Telephone-line Transceiver for a PCMCIA Modem Card

Note that  $C_r$  is included for canceling out the inadequacies of the lossy, miniature transformer. Refer to application note AN-397 for detailed explanation.

## “SIMPLE” MIXER (AMPLITUDE MODULATOR)

The mixer of Figure 39 is simple and provides a unique form of amplitude modulation.  $V_i$  is the modulation frequency ( $F_M$ ), while a +3V square-wave at the gate of Q1, induces a carrier frequency ( $F_C$ ). Q1 switches (toggles) U1 between inverting and non-inverting unity gain configurations. Offsetting a sine wave above ground at  $V_i$  results in the oscilloscope photo of Figure 40.

The simple mixer can be applied to applications that utilize the Doppler Effect to measure the velocity of an object. The difference frequency is one of its output frequency components. This difference frequency magnitude ( $|F_M - F_C|$ ) is the key factor for determining an object's velocity per the Doppler Effect. If a signal is transmitted to a moving object, the reflected frequency will be a different frequency. This difference in transmit and receive frequency is directly proportional to an object's velocity.

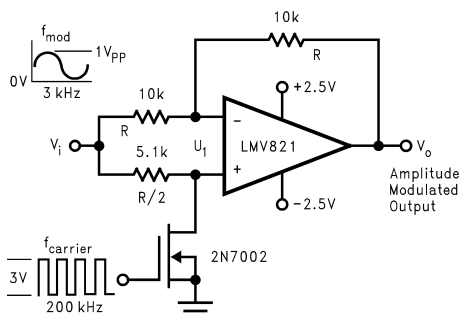


Figure 39. Amplitude Modulator Circuit



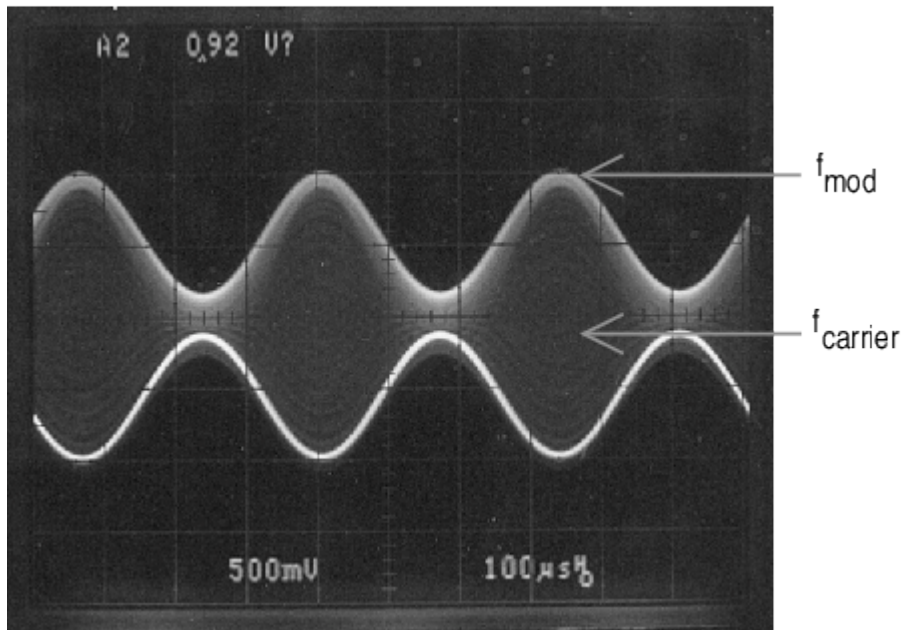
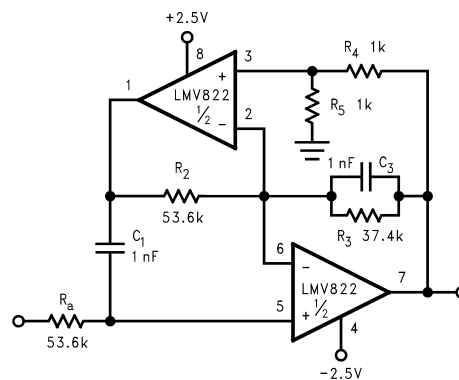


Figure 40. Output signal per the Circuit of Figure 39

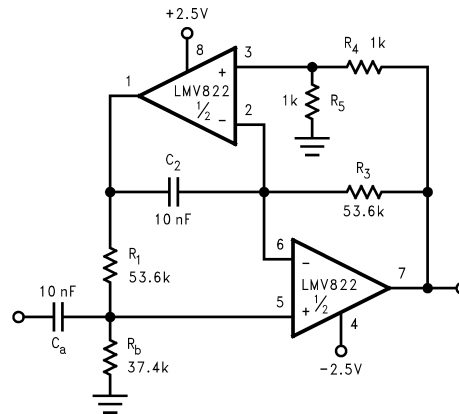
### DUAL AMPLIFIER ACTIVE FILTERS (DAAFs)

The LMV822/24 bring economy and performance to DAAFs. The low-pass and the high-pass filters of Figure 41 and Figure 42 (respectively), offer one key feature: excellent sensitivity performance. Good sensitivity is when deviations in component values cause relatively small deviations in a filter's parameter such as cutoff frequency ( $F_c$ ). Single amplifier active filters like the Sallen-Key provide relatively poor sensitivity performance that sometimes cause problems for high production runs; their parameters are much more likely to deviate out of specification than a DAAF would. The DAAFs of Figure 41 and Figure 42 are well suited for high volume production.



3 kHz Low-Pass Active Filter with a Butterworth Response and a Pass Band Gain of Times Two

Figure 41. Dual Amplifier



300 Hz High-Pass Active Filter with a Butterworth Response and a Pass Band Gain of Times Two

**Figure 42. Dual Amplifier**

Table 1 provides sensitivity measurements for a 10 MΩ load condition. The left column shows the passive components for the 3 kHz low-pass DAAF. The third column shows the components for the 300 Hz high-pass DAAF. Their respective sensitivity measurements are shown to the right of each component column. Their values consists of the percent change in cutoff frequency (Fc) divided by the percent change in component value. The lower the sensitivity value, the better the performance.

Each resistor value was changed by about 10 percent, and this measured change was divided into the measured change in Fc. A positive or negative sign in front of the measured value, represents the direction Fc changes relative to components' direction of change. For example, a sensitivity value of negative 1.2, means that for a 1 percent increase in component value, Fc decreases by 1.2 percent.

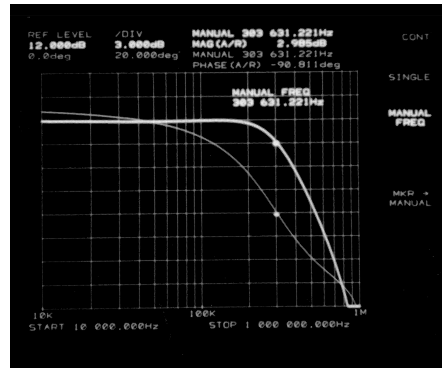
Note that this information provides insight on how to fine tune the cutoff frequency, if necessary. It should be also noted that R<sub>4</sub> and R<sub>5</sub> of each circuit also caused variations in the pass band gain. Increasing R<sub>4</sub> by ten percent, increased the gain by 0.4 dB, while increasing R<sub>5</sub> by ten percent, decreased the gain by 0.4 dB.

**Table 1.**

Component (LPF)	Sensitivity (LPF)	Component (HPF)	Sensitivity (HPF)
R <sub>a</sub>	-1.2	C <sub>a</sub>	-0.7
C <sub>1</sub>	-0.1	R <sub>b</sub>	-1.0
R <sub>2</sub>	-1.1	R <sub>1</sub>	+0.1
R <sub>3</sub>	+0.7	C <sub>2</sub>	-0.1
C <sub>3</sub>	-1.5	R <sub>3</sub>	+0.1
R <sub>4</sub>	-0.6	R <sub>4</sub>	-0.1
R <sub>5</sub>	+0.6	R <sub>5</sub>	+0.1

Active filters are also sensitive to an op amp's parameters -Gain and Bandwidth, in particular. The LMV822/24 provide a large gain and wide bandwidth. And DAAFs make excellent use of these feature specifications.

Single Amplifier versions require a large open-loop to closed-loop gain ratio - approximately 50 to 1, at the Fc of the filter response. Figure 43 shows an impressive photograph of a network analyzer measurement (hp3577A). The measurement was taken from a 300 kHz version of Figure 41. At 300 kHz, the open-loop to closed-loop gain ratio @ Fc is about 5 to 1. This is 10 times lower than the 50 to 1 "rule of thumb" for Single Amplifier Active Filters.



Butterworth Response as Measured by the HP3577A Network Analyzer

**Figure 43. 300 kHz, Low-Pass Filter**

In addition to performance, DAAFs are relatively easy to design and implement. The design equations for the low-pass and high-pass DAAFs are shown below. The first two equations calculate the  $F_c$  and the circuit Quality Factor ( $Q$ ) for the LPF (Figure 41). The second two equations calculate the  $F_c$  and  $Q$  for the HPF (Figure 42).

$$\begin{aligned}
 \text{(LPF)} \quad F_c &= \frac{\sqrt{R_5}}{2\pi\sqrt{R_a}\cdot\sqrt{R_2}\cdot\sqrt{R_4}\cdot\sqrt{C_1}\cdot\sqrt{C_3}} \\
 Q &= 2\pi F_c\sqrt{C_1}\cdot\sqrt{C_3} \\
 \text{(HPF)} \quad F_c &= \frac{\sqrt{R_4}}{2\pi\sqrt{R_1}\cdot\sqrt{R_3}\cdot\sqrt{R_5}\cdot\sqrt{C_a}\cdot\sqrt{C_2}} \\
 Q &= 2\pi F_c\sqrt{C_a}\cdot\sqrt{C_2}
 \end{aligned} \tag{2}$$

To simplify the design process, certain components are set equal to each other. Refer to Figure 41 and Figure 42. These equal component values help to simplify the design equations as follows:

$$\begin{aligned}
 \text{(LPF)} \quad R_a &= R_2 = \frac{1}{2\pi F_c\sqrt{C_1}\cdot\sqrt{C_3}} \\
 R_3 &= \frac{Q}{2\pi F_c\sqrt{C_1}\cdot\sqrt{C_3}} \\
 \text{(HPF)} \quad R_1 &= R_3 = \frac{1}{2\pi F_c\sqrt{C_a}\cdot\sqrt{C_2}} \\
 R_b &= \frac{Q}{2\pi F_c\sqrt{C_a}\cdot\sqrt{C_2}}
 \end{aligned} \tag{3}$$

To illustrate the design process/implementation, a 3 kHz, Butterworth response, low-pass filter DAAF (Figure 41) is designed as follows:

1. Choose  $C_1 = C_3 = C = 1$  nF
2. Choose  $R_4 = R_5 = 1$  k $\Omega$
3. Calculate  $R_a$  and  $R_2$  for the desired  $F_c$  as follows:

$$\begin{aligned}
 R_a = R_2 &= \frac{1}{2\pi(F_c)C} \\
 &= \frac{1}{2\pi(3 \text{ kHz})1 \text{ nF}} \\
 &= 53.1 \text{ k}\Omega \\
 &\cong 53.6 \text{ k}\Omega \text{ (Practical Value)}
 \end{aligned} \tag{4}$$

4. Calculate  $R_3$  for the desired  $Q$ . The desired  $Q$  for a Butterworth (Maximally Flat) response is 0.707 (45 degrees into the s-plane).  $R_3$  calculates as follows:

$$\begin{aligned}
 R_3 &= \frac{Q}{2\pi(F_c)C} \\
 &= \frac{0.707}{2\pi(3 \text{ kHz})1 \text{ nF}} \\
 &= 37.5 \text{ k}\Omega \\
 &\cong 37.4 \text{ k}\Omega \text{ (Practical Value)}
 \end{aligned}
 \tag{5}$$

Notice that  $R_3$  could also be calculated as 0.707 of  $R_a$  or  $R_2$ .

The circuit was implemented and its cutoff frequency measured. The cutoff frequency measured at 2.92 kHz.

The circuit also showed good repeatability. Ten different LMV822 samples were placed in the circuit. The corresponding change in the cutoff frequency was less than a percent.

### TRI-LEVEL VOLTAGE DETECTOR

The tri-level voltage detector of [Figure 44](#) provides a type of window comparator function. It detects three different input voltage ranges: Min-range, Mid-range, and Max-range. The output voltage ( $V_O$ ) is at  $V_{CC}$  for the Min-range.  $V_O$  is clamped at GND for the Mid-range. For the Max-range,  $V_O$  is at  $V_{ee}$ . [Figure 45](#) shows a  $V_O$  vs.  $V_I$  oscilloscope photo per the circuit of [Figure 44](#).

Its operation is as follows:  $V_I$  deviating from GND, causes the diode bridge to absorb  $I_{IN}$  to maintain a clamped condition ( $V_O = 0V$ ). Eventually,  $I_{IN}$  reaches the bias limit of the diode bridge. When this limit is reached, the clamping effect stops and the op amp responds open loop. The design equation directly preceding [Figure 45](#), shows how to determine the clamping range. The equation solves for the input voltage band on each side GND. The mid-range is twice this voltage band.

$$\Delta V = \frac{R}{R_1}(V_{CC} - V_{Diode})$$

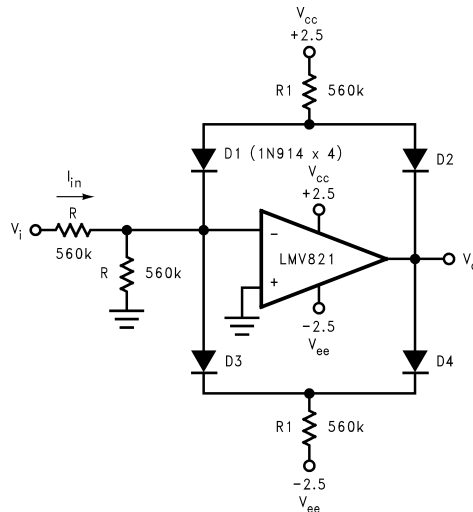


Figure 44. Tri-level Voltage Detector

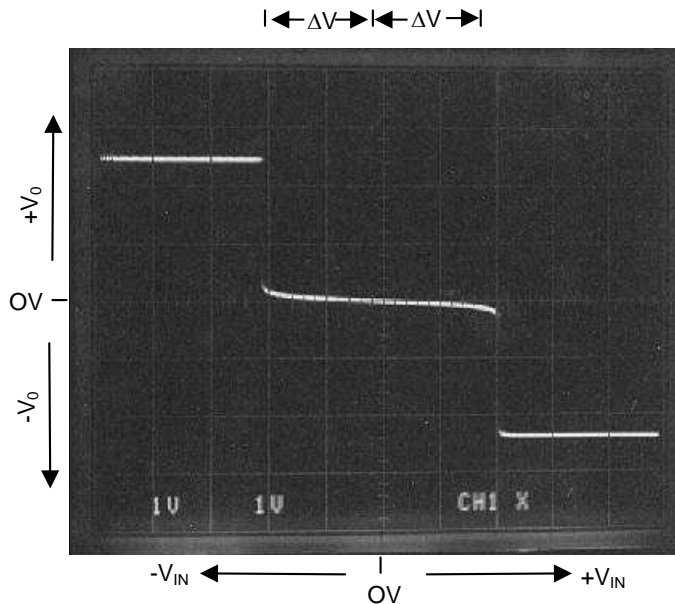


Figure 45. X, Y Oscilloscope Trace showing  $V_{OUT}$  vs  $V_{IN}$  per the Circuit of Figure 44

Connection Diagram

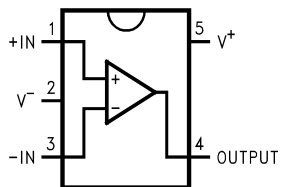


Figure 46. 5-Pin SC70-5/SOT23-5  
Top View  
Package Number DCK0005A/DBV0005A

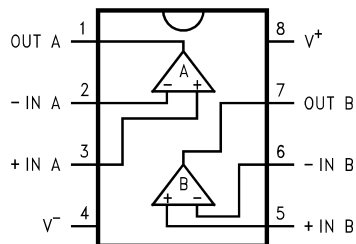


Figure 47. 8-Pin SOIC/VSSOP  
Top View  
Package Number D0008A/DGK0008A

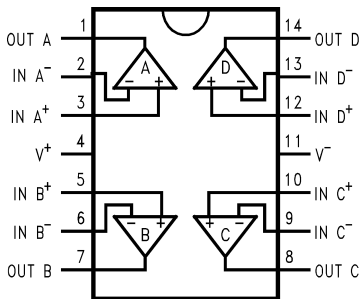


Figure 48. 14-Pin SOIC/TSSOP  
Top View  
Package Number D0014A/PW0014A

## REVISION HISTORY

Changes from Revision D (February 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format .....	21

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV821M5	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A14	<a href="#">Samples</a>
LMV821M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A14	<a href="#">Samples</a>
LMV821M5X	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A14	<a href="#">Samples</a>
LMV821M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A14	<a href="#">Samples</a>
LMV821M7	ACTIVE	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	A15	<a href="#">Samples</a>
LMV821M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A15	<a href="#">Samples</a>
LMV821M7X	ACTIVE	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 85	A15	<a href="#">Samples</a>
LMV821M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A15	<a href="#">Samples</a>
LMV822M	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMV 822M	<a href="#">Samples</a>
LMV822M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV 822M	<a href="#">Samples</a>
LMV822MM	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	V822	<a href="#">Samples</a>
LMV822MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	V822	<a href="#">Samples</a>
LMV822MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 85	V822	<a href="#">Samples</a>
LMV822MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	V822	<a href="#">Samples</a>
LMV822MX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMV 822M	<a href="#">Samples</a>
LMV822MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV 822M	<a href="#">Samples</a>
LMV822Q1MM/NOPB	PREVIEW	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AKAA	
LMV822Q1MMX/NOPB	PREVIEW	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AKAA	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV824M	ACTIVE	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LMV824M	<a href="#">Samples</a>
LMV824M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV824M	<a href="#">Samples</a>
LMV824MT	ACTIVE	TSSOP	PW	14	94	TBD	Call TI	Call TI	-40 to 85	LMV824 MT	<a href="#">Samples</a>
LMV824MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV824 MT	<a href="#">Samples</a>
LMV824MTX	ACTIVE	TSSOP	PW	14	2500	TBD	Call TI	Call TI	-40 to 85	LMV824 MT	<a href="#">Samples</a>
LMV824MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV824 MT	<a href="#">Samples</a>
LMV824MX	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LMV824M	<a href="#">Samples</a>
LMV824MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV824M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**OTHER QUALIFIED VERSIONS OF LMV822-N, LMV822-N-Q1, LMV824-N :**

- Catalog: [LMV822-N](#)
- Automotive: [LMV822-N-Q1](#), [LMV824-N-Q1](#)

NOTE: Qualified Version Definitions:

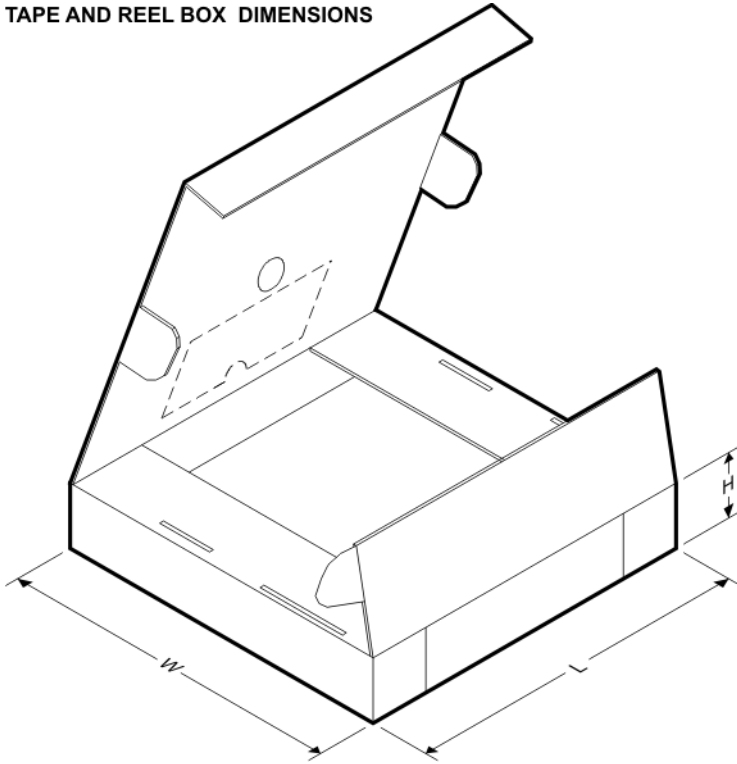
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV821M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV821M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV821M7X	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV821M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV822MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV822MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV824MTX	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LMV824MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LMV824MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV824MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV821M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV821M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV821M5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV821M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV821M7	SC70	DCK	5	1000	210.0	185.0	35.0
LMV821M7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV821M7X	SC70	DCK	5	3000	210.0	185.0	35.0
LMV821M7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV822MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV822MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV822MMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV822MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV822MX	SOIC	D	8	2500	367.0	367.0	35.0
LMV822MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV824MTX	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV824MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV824MX	SOIC	D	14	2500	367.0	367.0	35.0
LMV824MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

DBV (R-PDSO-G5)

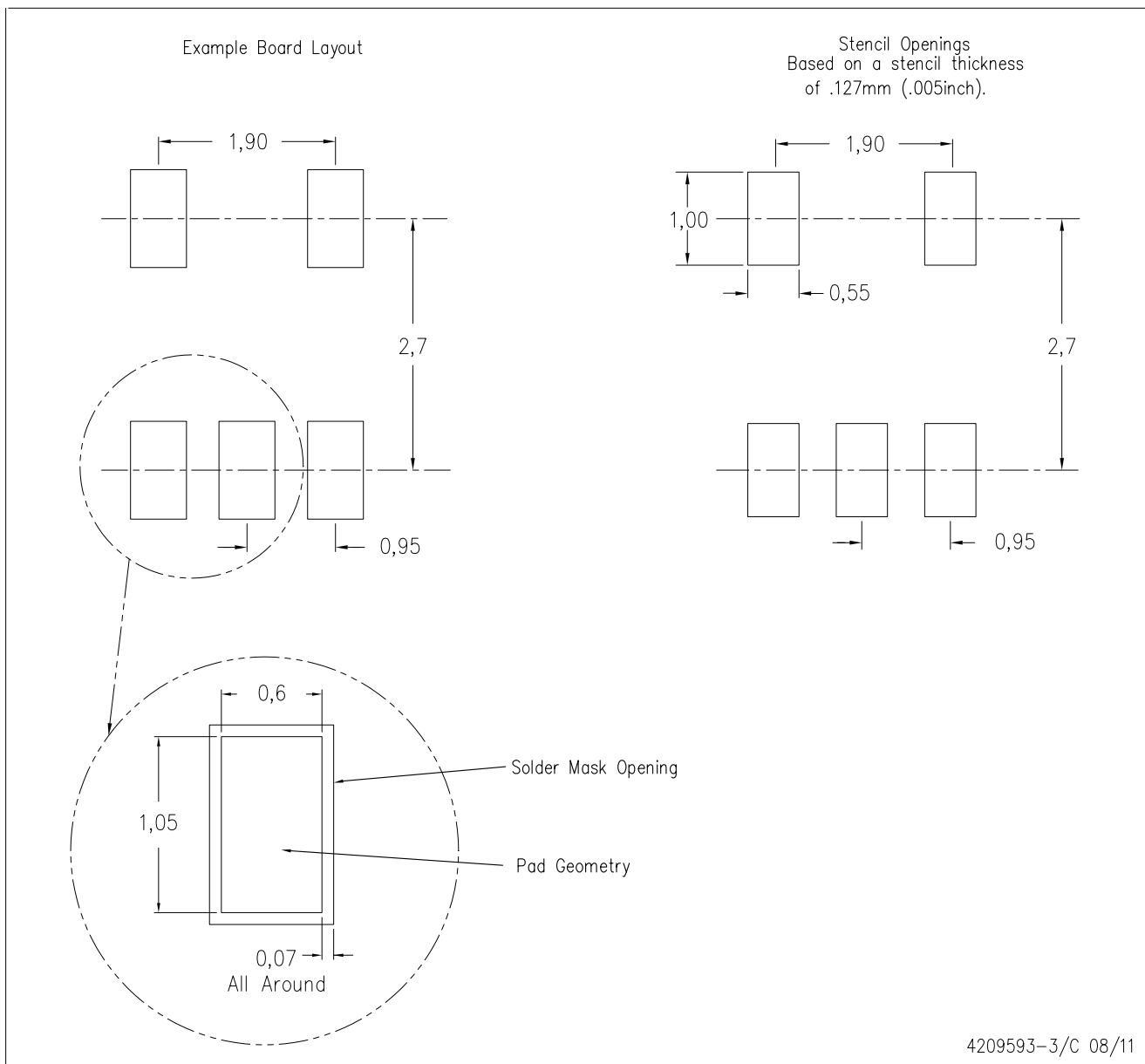
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

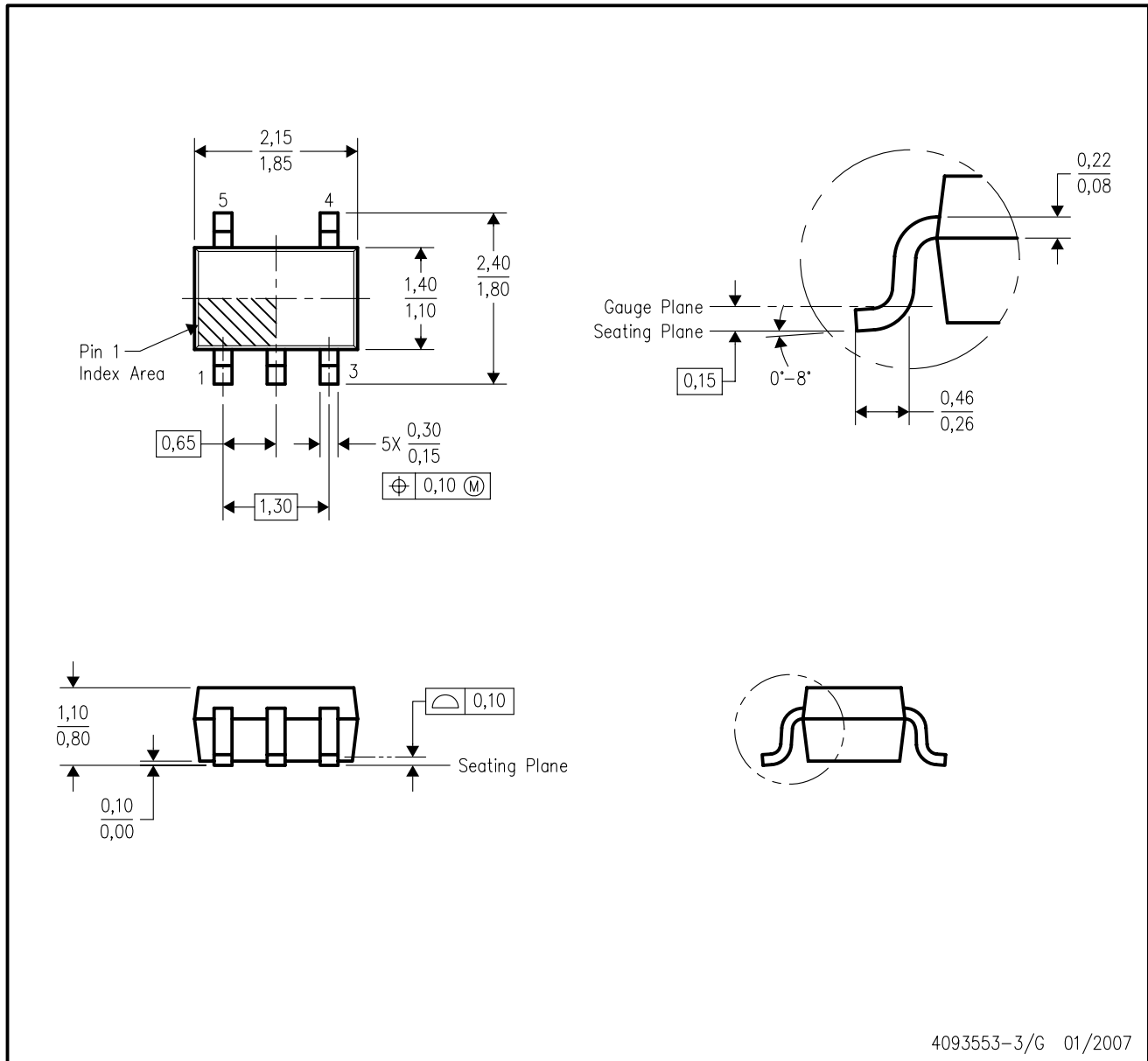
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



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