BURR - BROWN®

OPA2111

Dual Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 100% Tested, 8nV/√Hz max at 10kHz
- LOW BIAS CURRENT: 4pA max
- LOW OFFSET: 500μV max
- LOW DRIFT: 2.8μV/°C
- HIGH OPEN-LOOP GAIN: 114dB min
- HIGH COMMON-MODE REJECTION: 96dB min

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

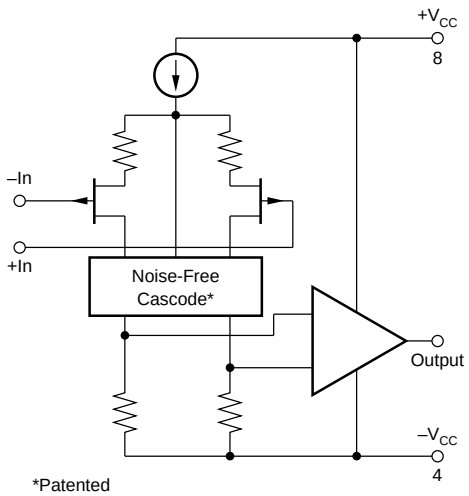
The OPA2111 is a high precision monolithic dielectrically isolated FET (***Difet***) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with patented circuit design techniques. A cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard dual op amp pin configuration allows upgrading of existing designs to higher performance levels.



OPA2111 Simplified Circuit
(Each Amplifier)

BIFET® National Semiconductor Corp., ***Difet***® Burr-Brown Corp.

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SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted

PARAMETER	CONDITION	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM, KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE														
Voltage, f_O = 10Hz	100% Tested		40	80		30	60		40	80		40		nV/√Hz
f_O = 100Hz	100% Tested		15	40		11	30		15	40		15		nV/√Hz
f_O = 1kHz	100% Tested		8	15		7	12		8	15		8		nV/√Hz
f_O = 10kHz	(1)		6	8		6	8		6	8		6		nV/√Hz
f_B = 10Hz to 10kHz	(1)		0.7	1.2		0.6	1		0.7	1.2		0.7		µVrms
f_B = 0.1Hz to 10Hz	(1)		1.6	3.3		1.2	2.5		1.6	3.3		1.6		µVp-p
Current, f_B = 0.1Hz to 10Hz	(1)		15	24		12	19		15	24		15		fAp-p
f_O = 0.1Hz to 20kHz	(1)		0.8	1.3		0.6	1		0.8	1		0.8		fA/√Hz
OFFSET VOLTAGE(2)														
Input Offset Voltage	V_{CM} = 0VDC		±0.1	±0.75		±0.05	±0.5		±0.1	±0.75		±0.3	±2	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±2	±6		±0.5	±2.8		±2	±6		±8	±15	µV/°C
Match			±1			±0.5			2			2		µV/°C
Supply Rejection		90	110		96	110		90	110		86	110		dB
			±3	±31		±3	±16		±3	±31		±3	±50	µV/V
Channel Separation	100Hz, R_L = 2kΩ		136			136			136			136		dB
BIAS CURRENT(2)														
Input Bias Current	V_{CM} = 0VDC		±2	±8		±1.2	±4		±2	±8		±3	±15	pA
Match			±1			±0.5			±1			2		pA
OFFSET CURRENT(2)														
Input Offset Current	V_{CM} = 0VDC		±1.2	±6		±0.6	±3		±1.2	±6		±3	±12	pA
IMPEDANCE														
Differential			10^{13} || 1			10^{13} || 1			10^{13} || 1			10^{13} || 1		Ω || pF
Common-Mode			10^{14} || 3			10^{14} || 3			10^{14} || 3			10^{14} || 3		Ω || pF
VOLTAGE RANGE														
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	90	110		96	110		90	110		82	110		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	R_L ≥ 2kΩ	110	125		114	125		110	125		106	125		dB
Match			3			2			3			3		dB
FREQUENCY RESPONSE														
Unity Gain, Small Signal			2			2			2			2		MHz
Full Power Response	20Vp-p, R_L = 2kΩ	16	32		16	32		16	32			32		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	1	2		1	2		1	2			2		V/µs
Settling Time, 0.1%	Gain = –1, R_L = 2kΩ		6			6			6			6		µs
0.01%	10V Step		10			10			10			10		µs
Overload Recovery, 50% Overdrive(3)	Gain = –1		5			5			5			5		µs
RATED OUTPUT														
Voltage Output	R_L = 2kΩ	±10	±11		±10	±11		±10	±11		±10	±11		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, Open-Loop		100			100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		10	40		mA
POWER SUPPLY														
Rated Voltage			±15			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		5	7		5	7		5	7		5	9	mA
TEMPERATURE RANGE														
Specification	Ambient Temp.	–25		+85	–25		+85	–55		+125	0		+70	°C
Operating "M" Package	Ambient Temp.	–55		+125	–55		+125	–55		+125	–55		+125	°C
"P" Package											–40		+85	°C
Storage "M" Package	Ambient Temp.	–65		+150	–65		+150	–65		+150	–65		+150	°C
"P" Package											–40		+85	°C
θ Junction-Ambient			200			200			200			200(4)		°C/W

NOTES: (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) Typical θ_{J-A} = 150°C/W for plastic DIP.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

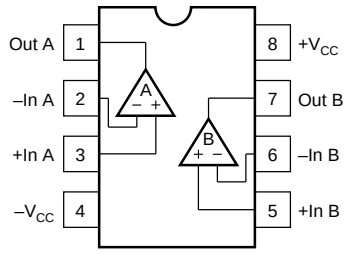
At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITION	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM, KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE														
Specification Range	Ambient Temp.	–25		+85	–25		+85	–55		+125	0		+70	°C
INPUT OFFSET VOLTAGE(1)														
Input Offset Voltage	V_{CM} = 0VDC		±0.22	±1.2		±0.08	±0.75		±0.3	±1.5		±0.9	±5	mV
Average Drift			±2	±6		±0.5	±2.8		±2	±6		±8	±15	µV/°C
Match			1			0.5			2			2		µV/°C
Supply Rejection		86	100		90	100		86	100		82	100		dB
			±10	±50		±10	±32		±10	±50		±10	±80	µV/V
BIAS CURRENT(1)														
Input Bias Current	V_{CM} = 0VDC		±125	±1nA		±75	±500		±2nA	±16.3nA		±125	±500	pA
Match			60			30			1nA					pA
OFFSET CURRENT(1)														
Input Offset Current	V_{CM} = 0VDC		±75	±750		±38	±375		±1.3nA	±12nA		±75	±375	pA
VOLTAGE RANGE														
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	100		90	100		86	100		80	100		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	106	120		110	120		106	120		100	120		dB
Match			5			3			5			5		dB
RATED OUTPUT														
Voltage Output	R_L = 2kΩ	±10.5	±11		±10.5	±11		±10.5	±11		±10.5	±11		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		±5	±10		mA
Short Circuit Current	V_O = 0VDC	10	40		10	40		10	40		10	40		mA
POWER SUPPLY														
Current, Quiescent	I_O = 0mADC		5	8		5	8		5	8		5	10	mA

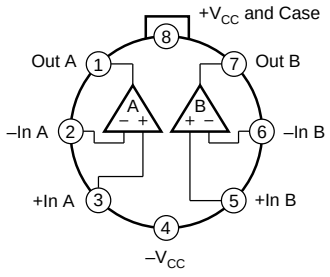
NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

CONNECTION DIAGRAMS

Top View **DIP**



Top View **TO-99**



ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation ($T_J \leq +175°C$)	500mW
Differential Input Voltage	Total V_{CC}
Input Voltage Range	$\pm V_{CC}$
Storage Temperature Range: "M" Package	–65°C to +150°C
"P" Package	–40°C to +85°C
Operating Temperature Range: "M" Package	–55°C to +125°C
"P" Package	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous
Junction Temperature	+175°C

PACKAGE INFORMATION

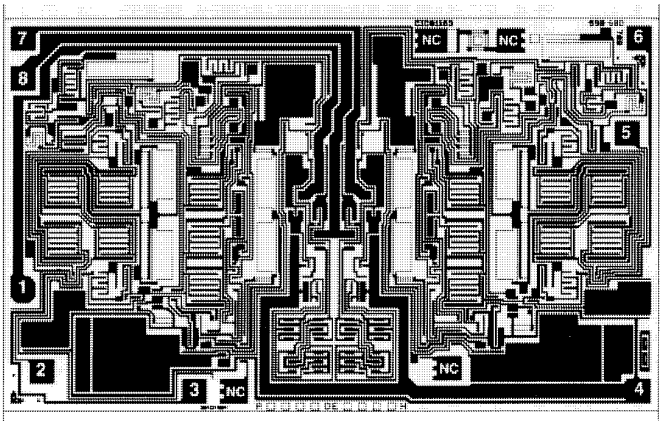
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA2111AM	TO-99	001
OPA2111BM	TO-99	001
OPA2111KM	TO-99	001
OPA2111SM	TO-99	001
OPA2111KP	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE, max (mV)
OPA2111AM	TO-99	–25°C to +85°C	±0.75
OPA2111BM	TO-99	–25°C to +85°C	±0.5
OPA2111KM	TO-99	0°C to +70°C	±2
OPA2111SM	TO-99	–55°C to +125°C	±0.75
OPA2111KP	8-Pin Plastic DIP	0°C to +70°C	±2

DICE INFORMATION



OPA2111AD DIE TOPOGRAPHY

PAD	FUNCTION
1	Out A
2	–In A
3	+In A
4	$-V_S$
5	+In B
6	–In B
7	Out B
8	$+V_S$
NC	No Connection

Substrate Bias: No Connection

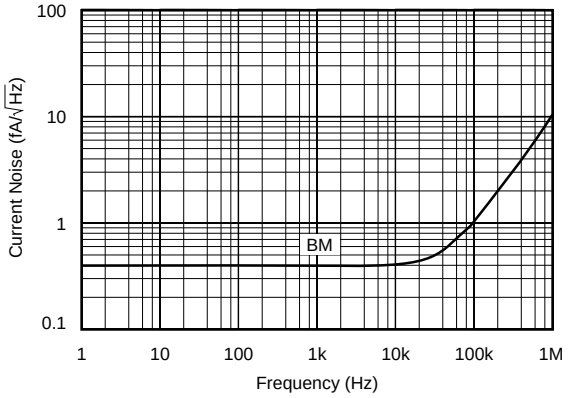
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	138 x 84 ±5	3.51 x 2.13 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		None
Transistor Count		102

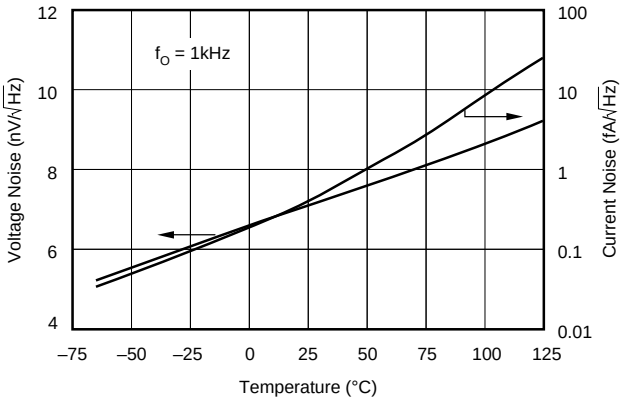
TYPICAL PERFORMANCE CURVES

T_A = +25°C, and V_{CC} = ±15VDC unless otherwise noted.

INPUT CURRENT NOISE SPECTRAL DENSITY



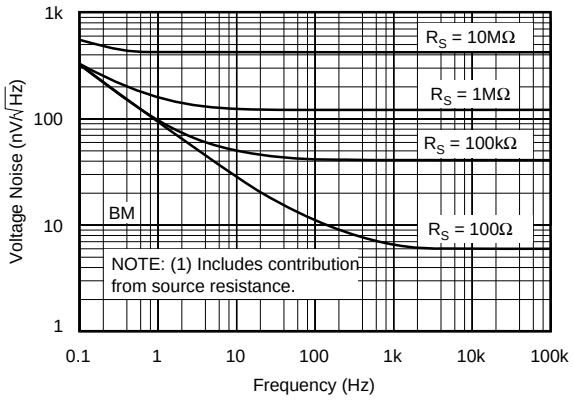
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



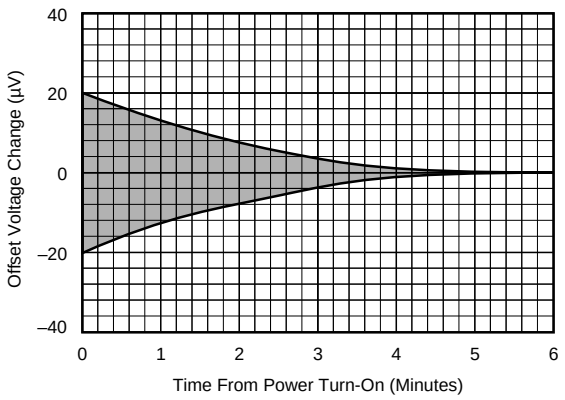
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, and V_{CC} = ±15VDC unless otherwise noted.

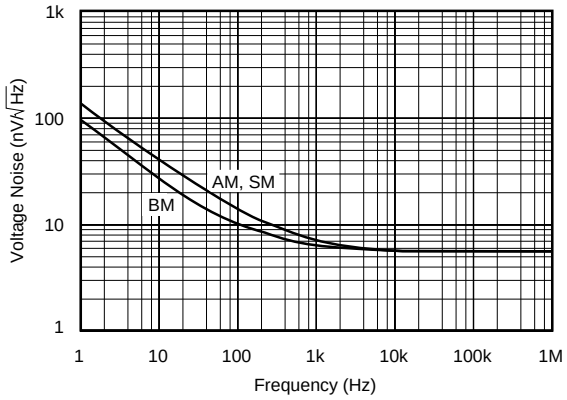
TOTAL[1] INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



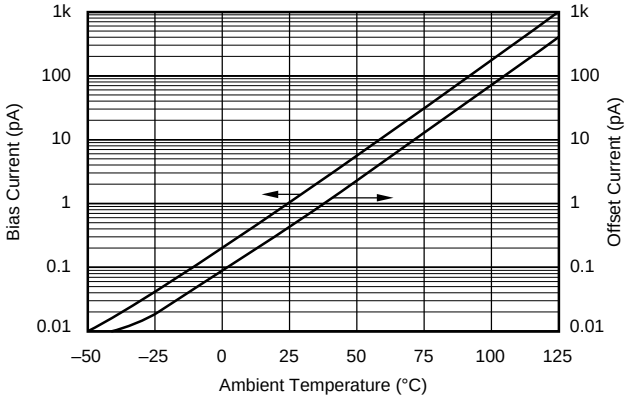
INPUT OFFSET VOLTAGE WARM-UP DRIFT



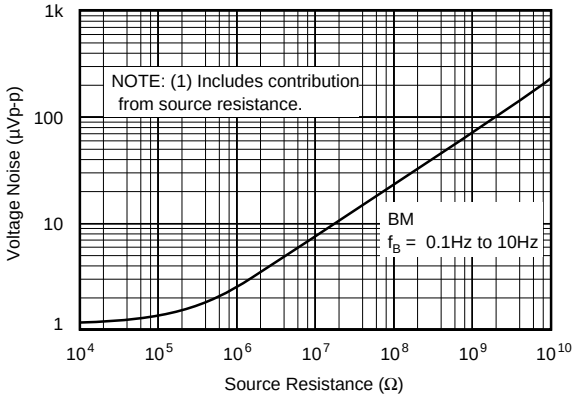
INPUT VOLTAGE NOISE SPECTRAL DENSITY



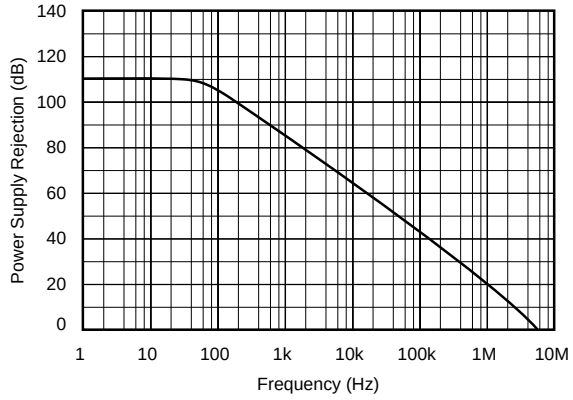
BIAS AND OFFSET CURRENT vs TEMPERATURE



TOTAL[1] INPUT VOLTAGE NOISE (PEAK-TO-PEAK) vs SOURCE RESISTANCE



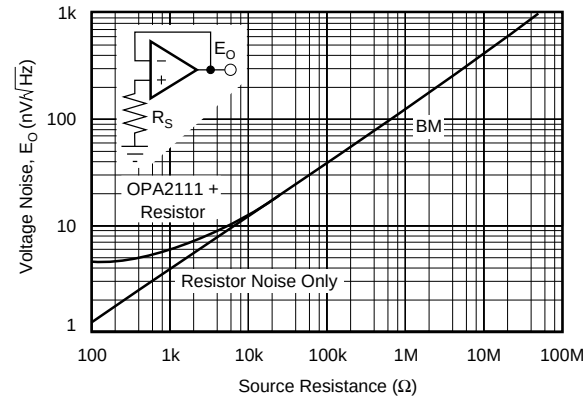
POWER SUPPLY REJECTION vs FREQUENCY



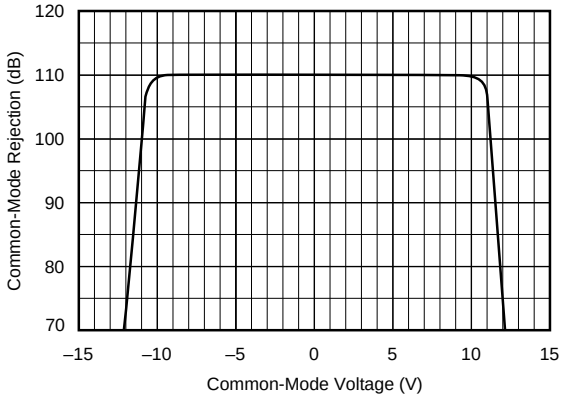
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, and V_{CC} = ±15VDC unless otherwise noted.

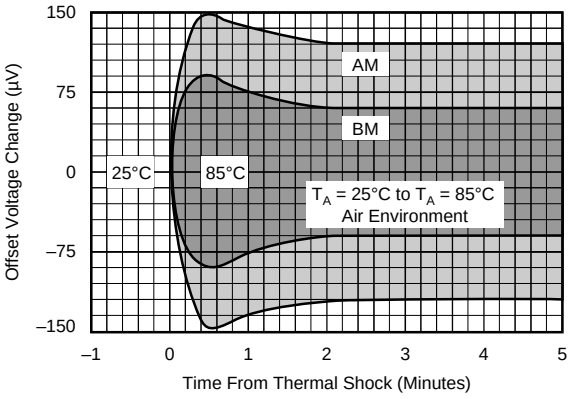
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY
AT 1kHz vs SOURCE RESISTANCE



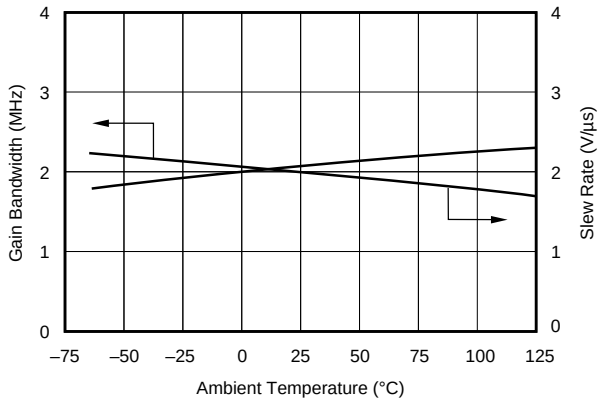
COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



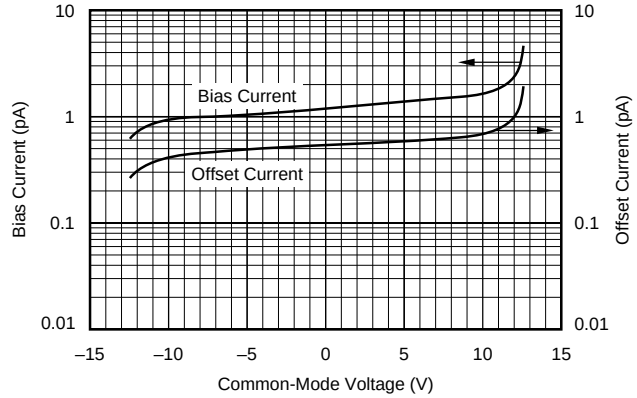
INPUT OFFSET VOLTAGE CHANGE
DUE TO THERMAL SHOCK



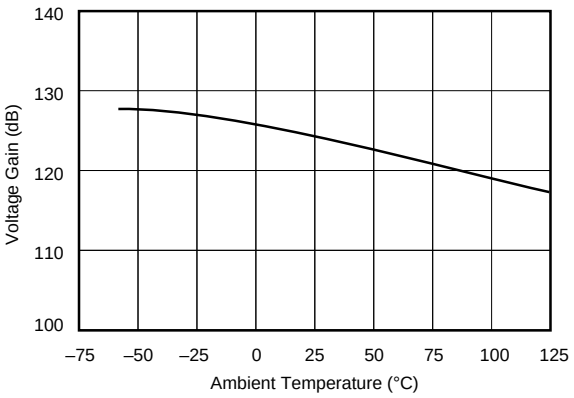
GAIN-BANDWIDTH AND SLEW RATE
vs TEMPERATURE



BIAS AND OFFSET CURRENT
vs INPUT COMMON-MODE VOLTAGE



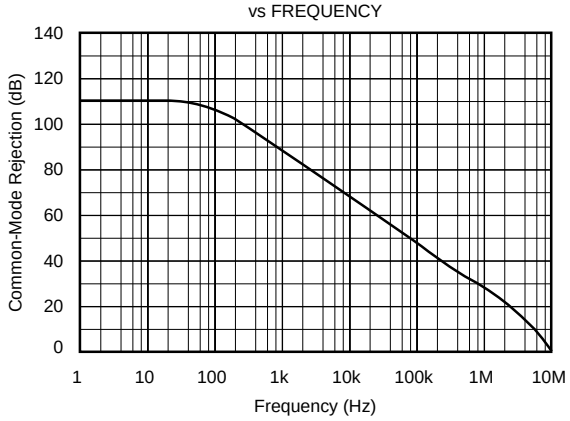
OPEN-LOOP GAIN vs TEMPERATURE



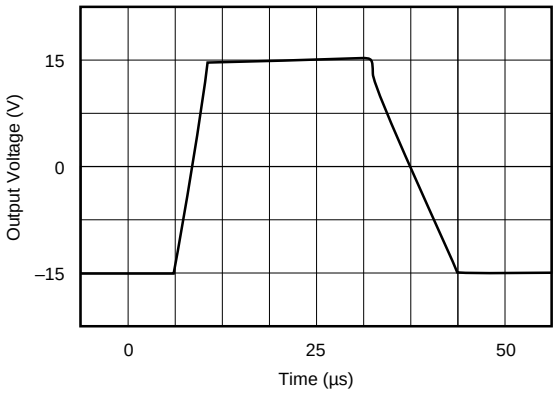
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

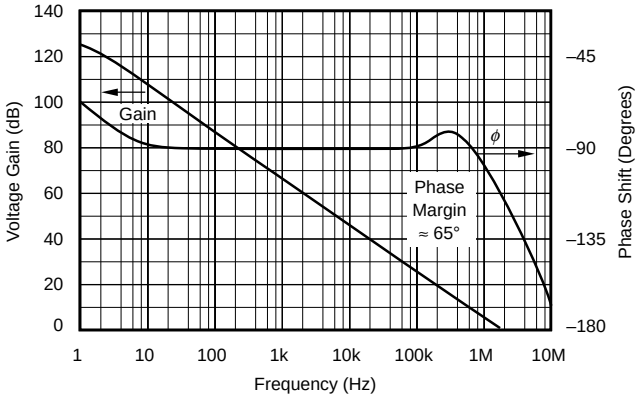
COMMON-MODE REJECTION vs FREQUENCY



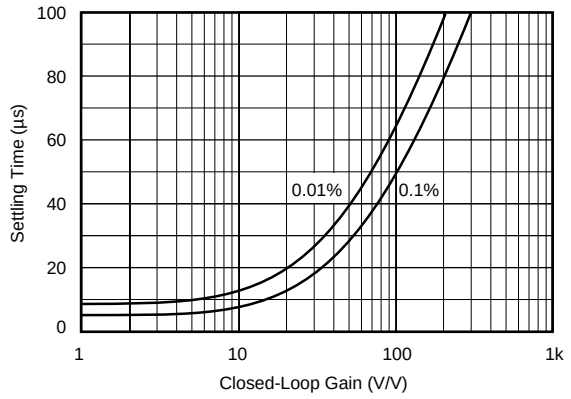
LARGE SIGNAL TRANSIENT RESPONSE



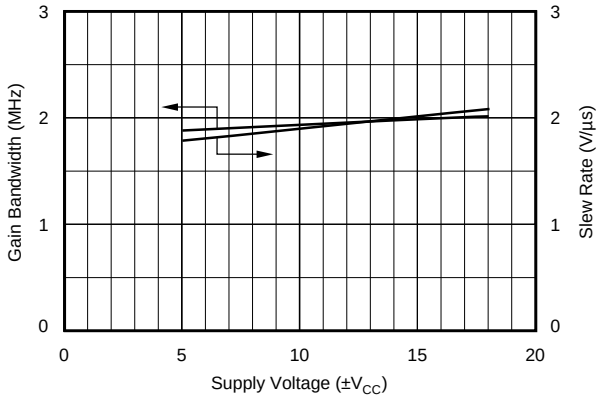
OPEN-LOOP FREQUENCY RESPONSE



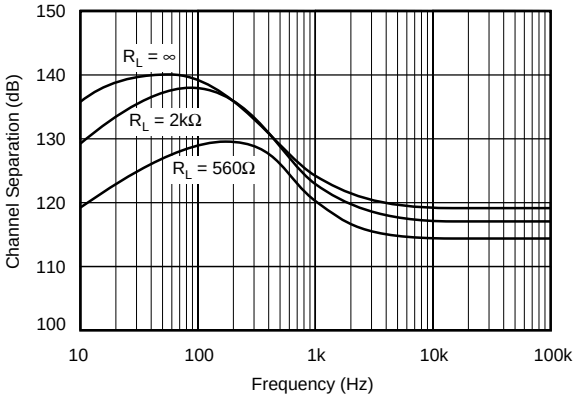
SETTLING TIME vs CLOSED-LOOP GAIN



GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



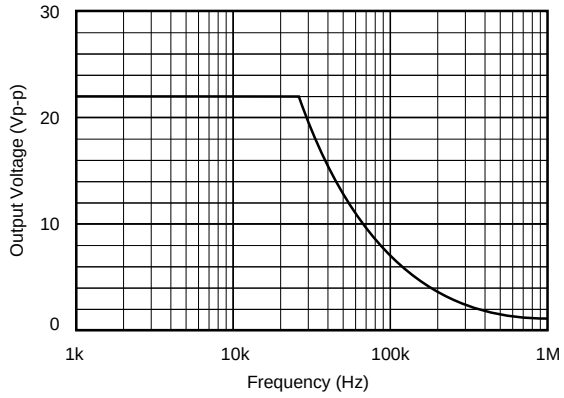
CHANNEL SEPARATION vs FREQUENCY



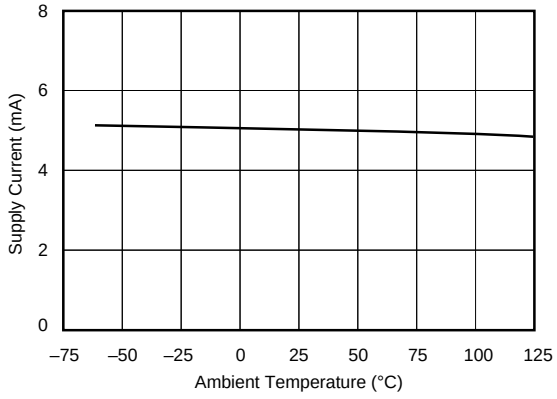
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

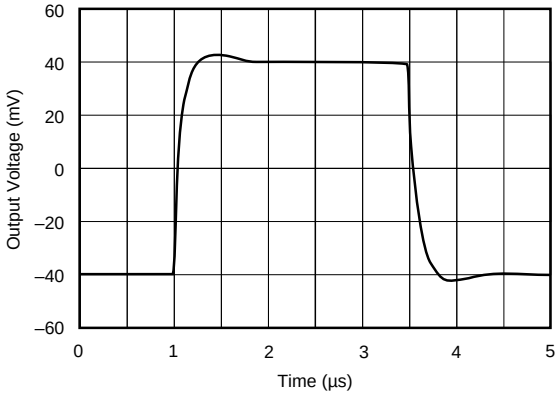
MAXIMUM UNDISTORTED OUTPUT VOLTAGE vs FREQUENCY



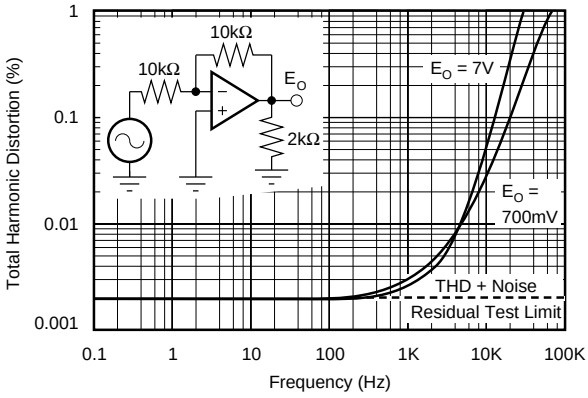
SUPPLY CURRENT vs TEMPERATURE



SMALL SIGNAL TRANSIENT RESPONSE



TOTAL HARMONIC DISTORTION vs FREQUENCY



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA2111 offset voltage is laser-trimmed and will require no further trim for most applications.

Offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

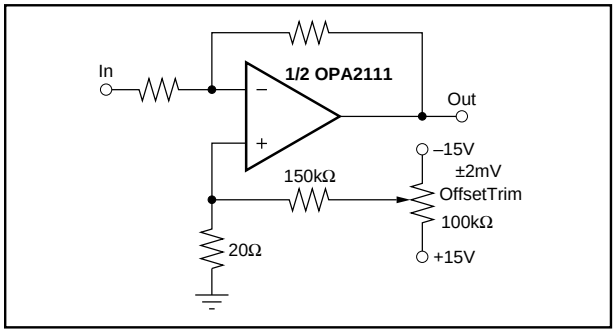


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Because of its dielectric isolation, no special protection is needed on the OPA2111. Of course, the differential and common-mode voltage limits should be observed. Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA2111. To avoid leakage problems, it is recommended that the signal input lead of the OPA2111 be wired to a Teflon standoff. If the OPA2111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 2).

NOISE: FET vs BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the low voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the OPA2111 will have lower total noise than an OP-27 (see Figure 3).

BIAS CURRENT CHANGE vs COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET® operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely low bias current of the OPA2111 is not compromised by common-mode voltage.

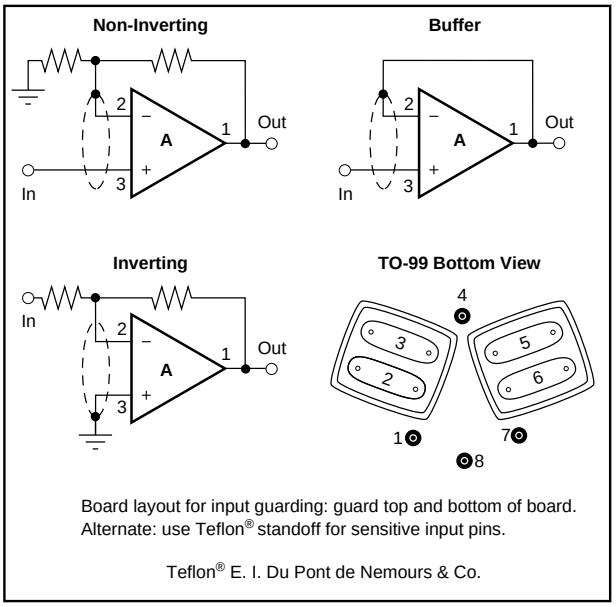


FIGURE 2. Connection of Input Guard.

APPLICATIONS CIRCUITS

Figures 5 through 13 are circuit diagrams of various applications for the OPA2111.

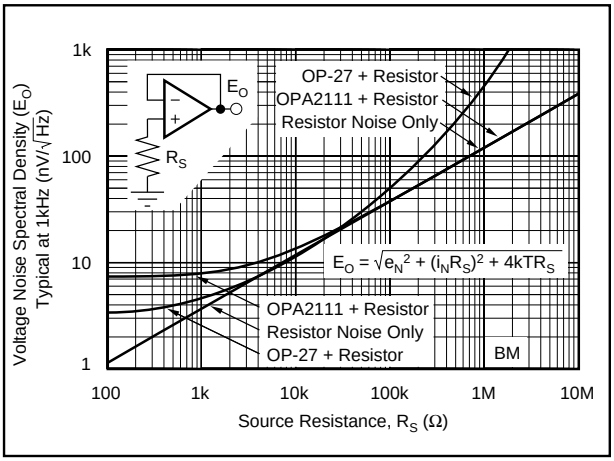


FIGURE 3. Voltage Noise Spectral Density vs Source Resistance.

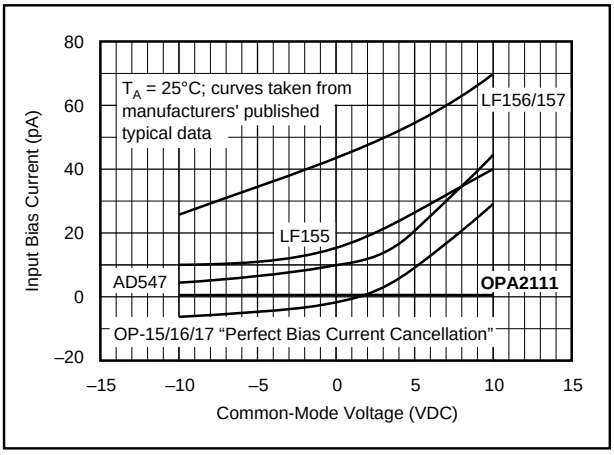


FIGURE 4. Input Bias Currrent vs Common-Mode Voltage.

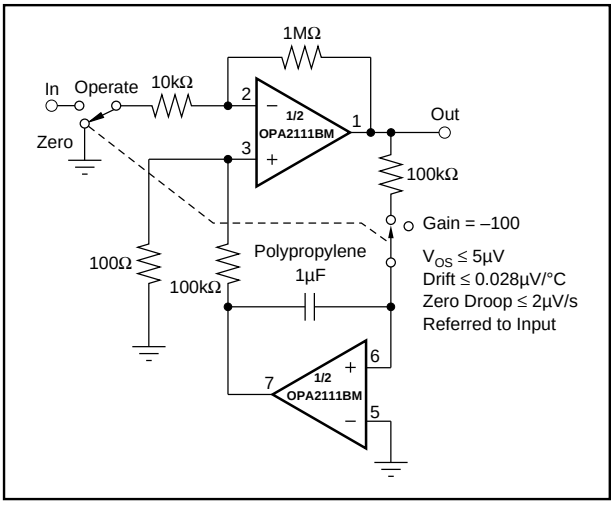


FIGURE 5. Auto-Zero Amplifier.

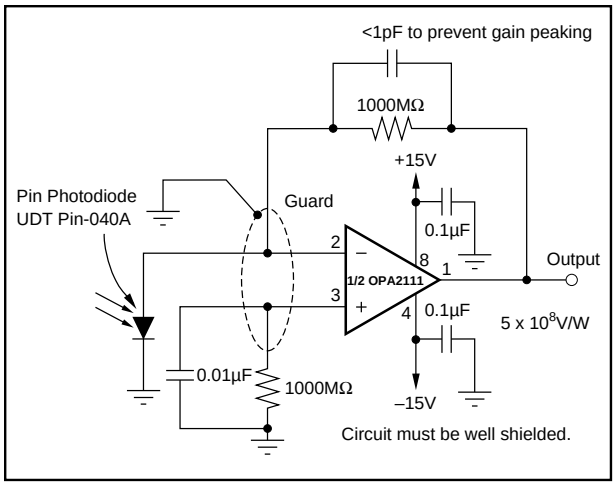


FIGURE 6. Sensitive Photodiode Amplifier.

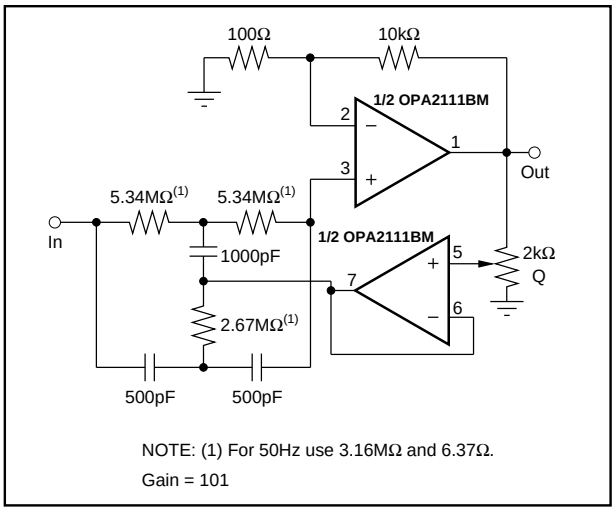


FIGURE 7. High Impedance 60Hz Reject Filter with Gain.

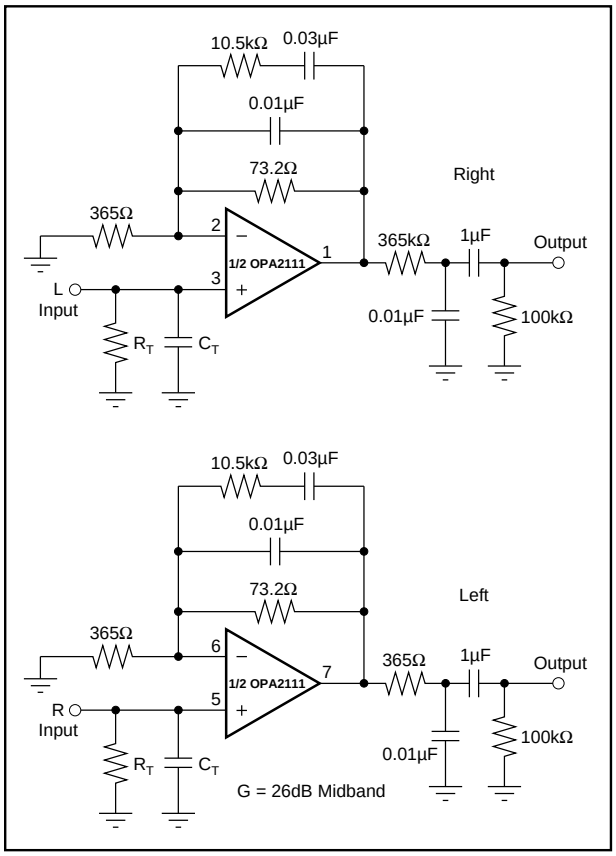


FIGURE 8. RIAA Equalized Stereo Preamplifier.

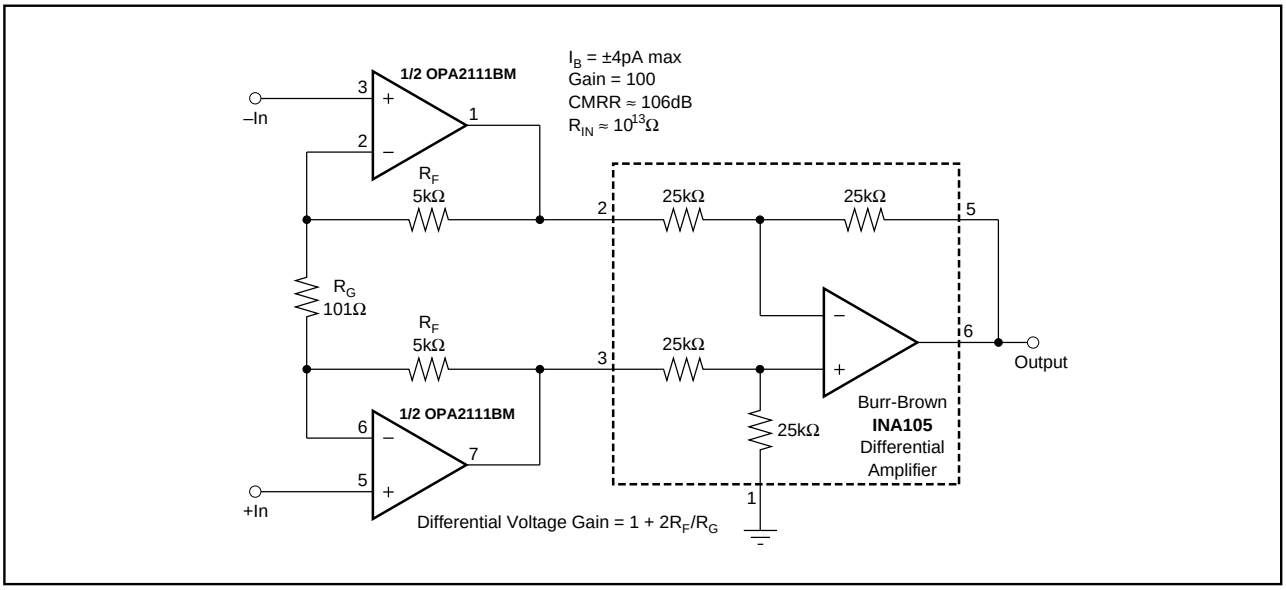


FIGURE 9. FET Input Instrumentation Amplifier.

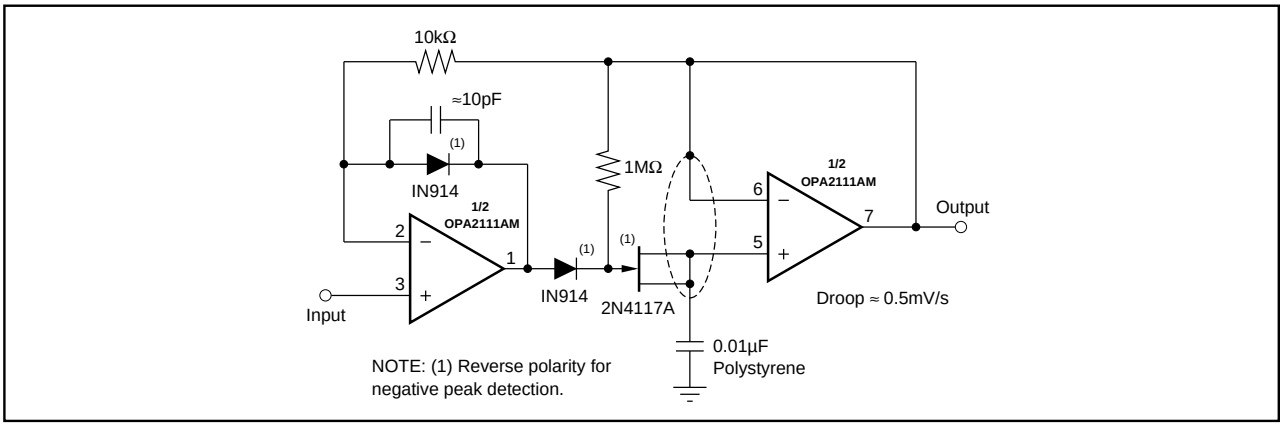


FIGURE 10. Low-Droop Positive Peak Detector.

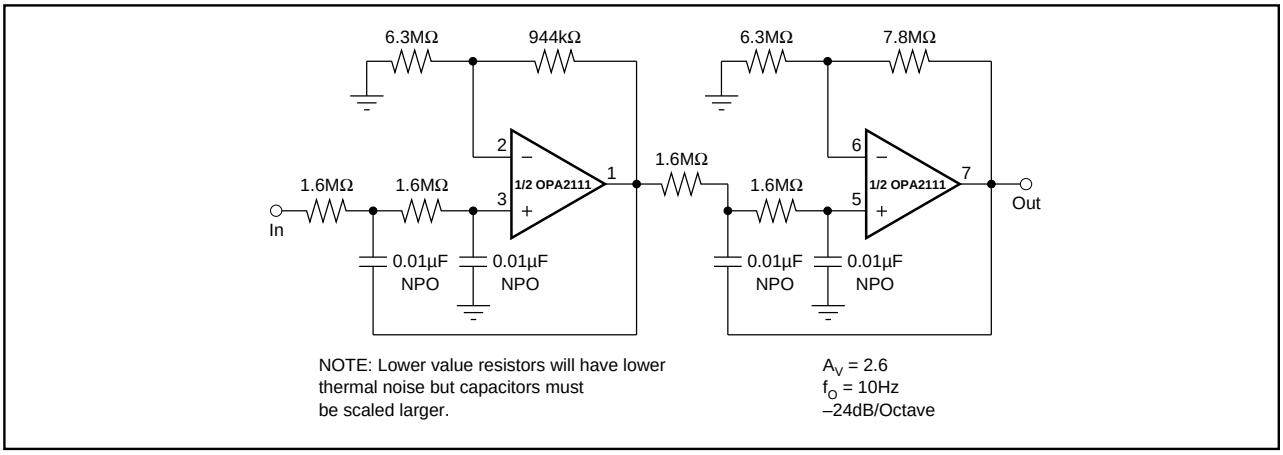


FIGURE 11. 10Hz Fourth-Order Butterworth Low-Pass Filter.

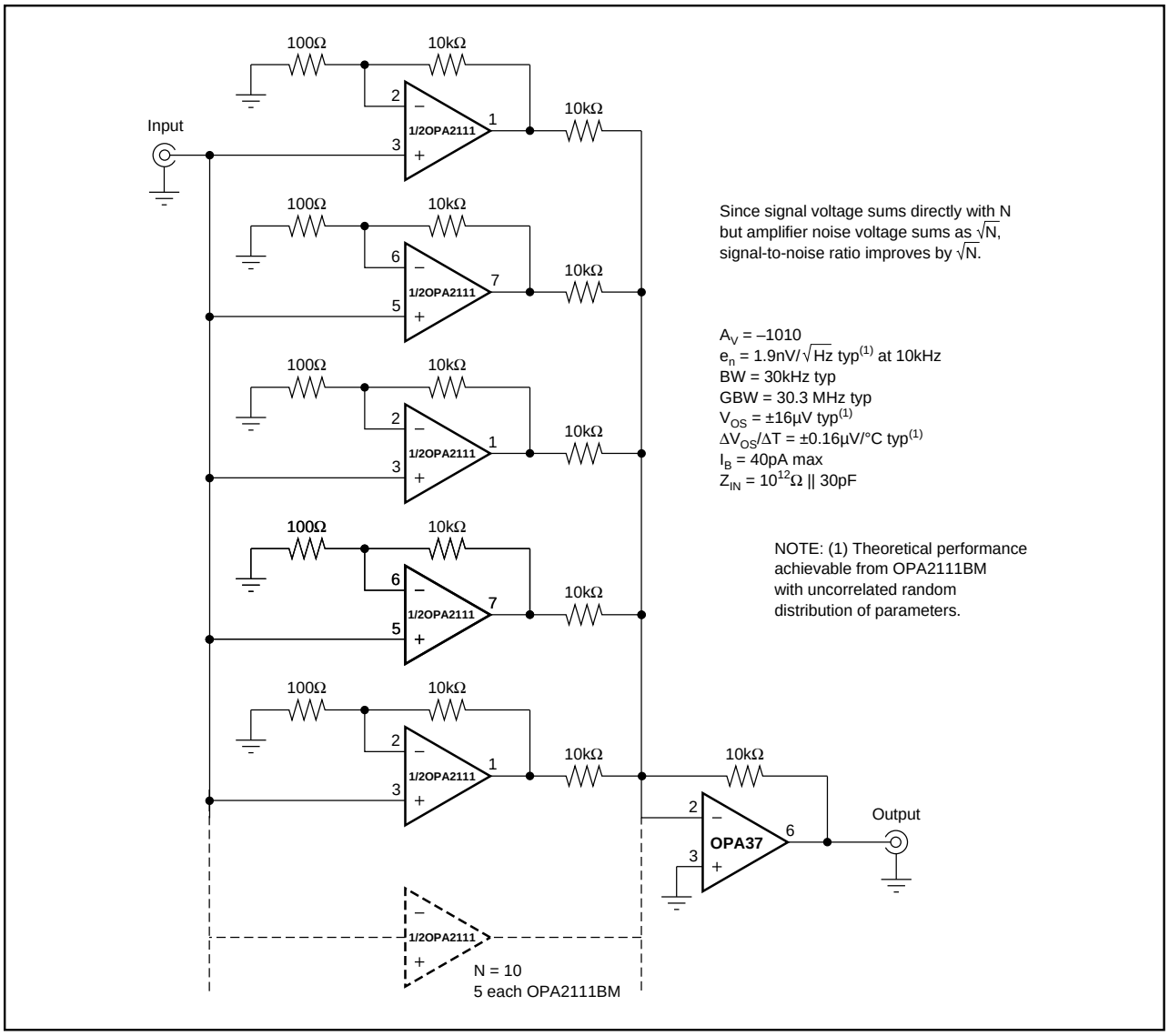
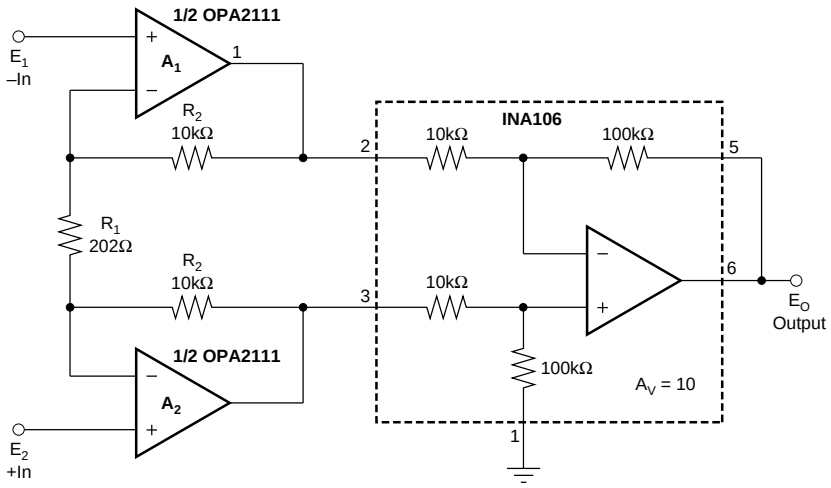


FIGURE 12. 'N' Stage Parallel-Input Amplifier.



$$E_O = 10(1 + 2\ R_2/R_1)(E_2 - E_1) = 1000(E_2 - E_1)$$

Using the INA106 for an output difference amplifier extends the input common-mode range of an instrumentation amplifier to ±10V. A conventional IA with a unity-gain difference amplifier has an input common-mode range limited to ±5V for an output swing of ±10V. This is because a unity-gain difference amp needs ±5V at the input for 10V at the output, allowing only 5V additional for common-mode.

FIGURE 13. Precision Instrumentation Amplifier.

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA2111AM	NRND	TO-99	LMC	8	20	None	Call TI	Level-NA-NA-NA
OPA2111BM	NRND	TO-99	LMC	8	20	None	Call TI	Level-NA-NA-NA
OPA2111KM	NRND	TO-99	LMC	8	20	None	Call TI	Level-NA-NA-NA
OPA2111KP	ACTIVE	PDIP	P	8	50	None	Call TI	Level-NA-NA-NA

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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