Low-Noise, Low Quiescent Current, Precision Operational Amplifier *e-trim*™ Series

Check for Samples: OPA376, OPA2376, OPA4376

FEATURES

- **LOW NOISE: 7.5nV/√Hz at 1kHz**
- **0.1Hz TO 10Hz NOISE: 0.8μV_{PP}**
- **QUIESCENT CURRENT: 760μA (typ)**
- **LOW OFFSET VOLTAGE: 5μV (typ)**
- **GAIN BANDWIDTH PRODUCT: 5.5MHz**
- **RAIL-TO-RAIL INPUT AND OUTPUT**
- **SINGLE-SUPPLY OPERATION**
- **SUPPLY VOLTAGE: 2.2V to 5.5V**
- **SPACE-SAVING PACKAGES:**
  - **SC-70, SOT23, WCSP, MSOP, TSSOP**

APPLICATIONS

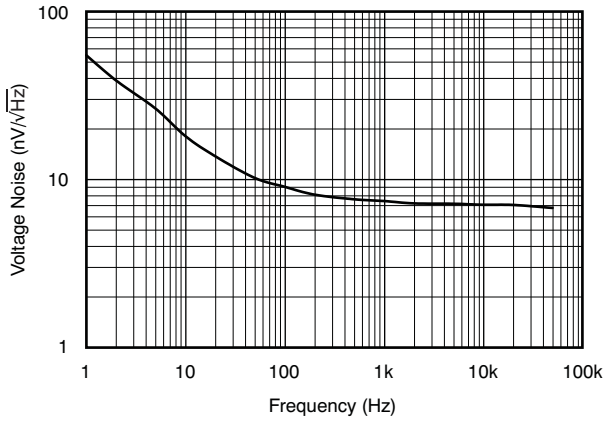
- **ADC BUFFER**
- **AUDIO EQUIPMENT**
- **MEDICAL INSTRUMENTATION**
- **HANDHELD TEST EQUIPMENT**
- **ACTIVE FILTERING**
- **SENSOR SIGNAL CONDITIONING**

DESCRIPTION

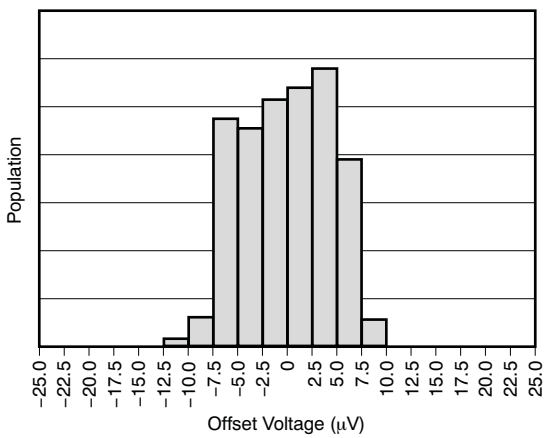
The OPA376 family represent a new generation of low-noise operational amplifiers with *e-trim*, offering outstanding dc precision and ac performance. Rail-to-rail input and output, low offset (25μV max), low noise (7.5nV/√Hz), quiescent current of 950μA max, and a 5.5MHz bandwidth make this part very attractive for a variety of precision and portable applications. In addition, this device has a reasonably wide supply range with excellent PSRR, making it attractive for applications that run directly from batteries without regulation.

The OPA376 (single version) is available in *Micro*SIZE SC70-5, SOT23-5, and SO-8 packages. The OPA2376 (dual) is offered in the WCSP-8, MSOP-8, and SO-8 packages. The OPA4376 (quad) is offered in a TSSOP-14 package. All versions are specified for operation from –40°C to +125°C.

INPUT VOLTAGE NOISE SPECTRAL DENSITY



OFFSET VOLTAGE PRODUCTION DISTRIBUTION



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATING(1)

over operating free-air temperature range (unless otherwise noted)

		OPA376, OPA2376, OPA4376	UNIT
Supply Voltage	V_S = (V+) – (V–)	+7	V
Signal Input Terminals	Voltage(2)	(V–) – 0.5 to (V+) + 0.5	V
	Current(2)	±10	mA
Output Short-Circuit(3)		Continuous	
Operating Temperature	T_A	–40 to +150	°C
Storage Temperature	T_A	–65 to +150	°C
Junction Temperature	T_J	+150	°C
ESD Rating	Human Body Model	4000	V
	Charged Device Model	1000	V
	Machine Model	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA376	SC70-5	DCK	BUR
	SOT23-5	DBV	BUQ
	SO-8	D	OPA376
OPA2376	SO-8	D	OPA2376
	MSOP-8	DGK	OBBI
OPA2376	Lead- (Pb-) Free WCSP-8	YZD	OPA2376
OPA4376	TSSOP-14	PW	OPA4376

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ELECTRICAL CHARACTERISTICS: V_S = +2.2V to +5.5V

Boldface limits apply over the specified temperature range: **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2, and $V_{O\ UT}$ = V_S/2, unless otherwise noted.

PARAMETERS		CONDITIONS	OPA376, OPA2376, OPA4376			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}			5	25	µV
vs Temperature	dV_{OS}/dT	–40°C to +85°C		0.26	1	µV/°C
		–40°C to +125°C		**0.32**	**2**	**µV/°C**
vs Power Supply	PSRR	V_S = +2.2V to +5.5V, V_{CM} < (V+) – 1.3V		5	20	µV/V
Over Temperature		**V_S = +2.2V to +5.5V, V_{CM} < (V+) – 1.3V**		**5**		**µV/V**
Channel Separation, dc (dual, quad)				0.5		mV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			0.2	10	pA
Over Temperature			**See Typical Characteristics**			**pA**
Input Offset Current	I_{OS}			0.2	10	pA
NOISE						
Input Voltage Noise, f = 0.1Hz to 10Hz				0.8		μV_{PP}
Input Voltage Noise Density, f = 1kHz	e_n			7.5		$nV/\sqrt{Hz}$
Input Current Noise, f = 1kHz	i_n			2		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) – 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	CMRR	(V–) < V_{CM} < (V+) – 1.3 V	76	90		dB
INPUT CAPACITANCE						
Differential				6.5		pF
Common-Mode				13		pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	50mV < V_O < (V+) – 50mV, R_L = 10kΩ	120	134		dB
		100mV < V_O < (V+) – 100mV, R_L = 2kΩ	120	126		dB
FREQUENCY RESPONSE		C_L = 100pF, V_S = 5.5V				
Gain-Bandwidth Product	GBW			5.5		MHz
Slew Rate	SR	G = +1		2		V/µs
Settling Time 0.1%	t_S	2V Step , G = +1		1.6		µs
Settling Time 0.01%	t_S	2V Step , G = +1		2		µs
Overload Recovery Time		V_{IN} × Gain > V_S		0.33		µs
THD + Noise	THD+N	V_O = $1V_{RMS}$, G = +1, f = 1kHz, R_L = 10kΩ		0.00027		%
OUTPUT						
Voltage Output Swing from Rail		R_L = 10kΩ(1)		10	20	mV
		R_L = 10kΩ(2)		20	30	mV
Over Temperature		**R_L = 10kΩ**			**40**	**mV**
Voltage Output Swing from Rail		R_L = 2kΩ(1)		40	50	mV
		R_L = 2kΩ(2)		50	60	mV
Over Temperature		**R_L = 2kΩ**			**80**	**mV**
Short-Circuit Current	I_{SC}			+30/–50		mA
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics			
Open-Loop Output Impedance	R_O			150		Ω

(1) SC70-5, SOT23-5, SO-8, MSOP-8, and TSSOP-14 packages only.
(2) Wafer chip-scale package only.

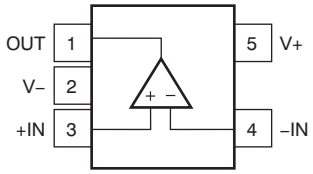
ELECTRICAL CHARACTERISTICS: V_S = +2.2V to +5.5V (continued)

Boldface limits apply over the specified temperature range: **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2, and $V_{O\ UT}$ = V_S/2, unless otherwise noted.

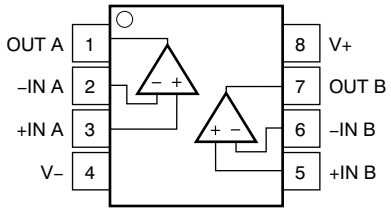
PARAMETERS		CONDITIONS	OPA376, OPA2376, OPA4376			UNIT
			MIN	TYP	MAX	
POWER SUPPLY						
Specified Voltage Range	V_S		2.2		5.5	V
Operating Voltage Range				2 to 5.5		V
Quiescent Current per amplifier	I_Q	I_O = 0, V_S = +5.5V, V_{CM} < (V+) – 1.3V		760	950	µA
Over Temperature					**1**	**mA**
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Operating Range			–40		+150	°C
Thermal Resistance	θ_{JA}					°C/W
SC70				250		°C/W
SOT23				200		°C/W
SO-8, TSSOP-14, MSOP-8				150		°C/W
WCSP-8				250		°C/W

PIN CONFIGURATIONS

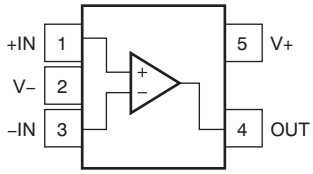
OPA376
SOT23-5
(TOP VIEW)



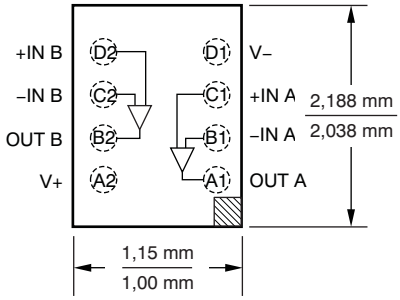
OPA2376
SO-8, MSOP-8
(TOP VIEW)



OPA376
SC70-5
(TOP VIEW)

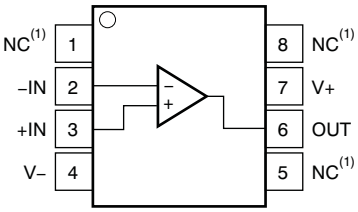


OPA2376
WCSP-8
(TOP VIEW)

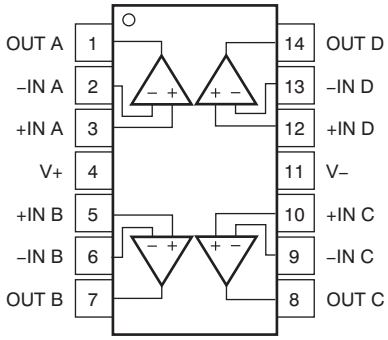


(Bump Side Down)

OPA376
SO-8
(TOP VIEW)



OPA4376
TSSOP-14
(TOP VIEW)



NOTE: (1) NC denotes no internal connection.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to $V_S/2$, V_{CM} = $V_S/2$, and $V_{O\ UT}$ = $V_S/2$, unless otherwise noted.

OPEN-LOOP GAIN/PHASE vs FREQUENCY

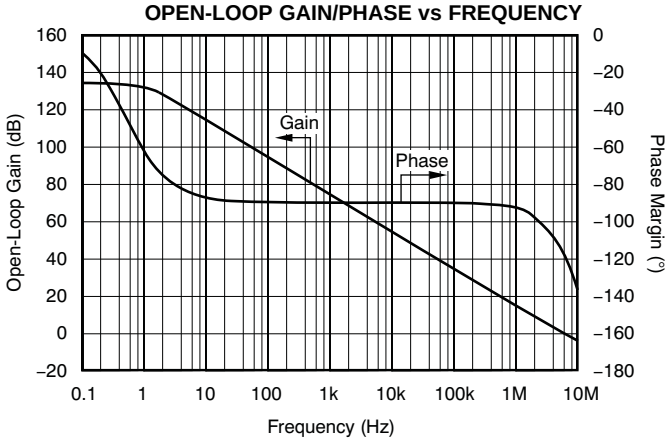


Figure 1.

POWER-SUPPLY AND COMMON-MODE REJECTION RATIO vs FREQUENCY

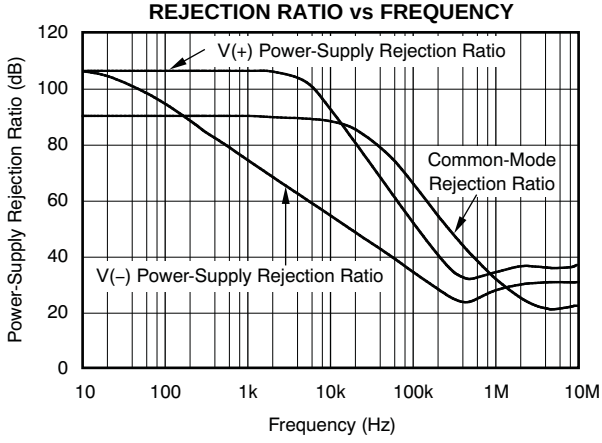


Figure 2.

OPEN-LOOP GAIN AND POWER-SUPPLY REJECTION RATIO vs TEMPERATURE

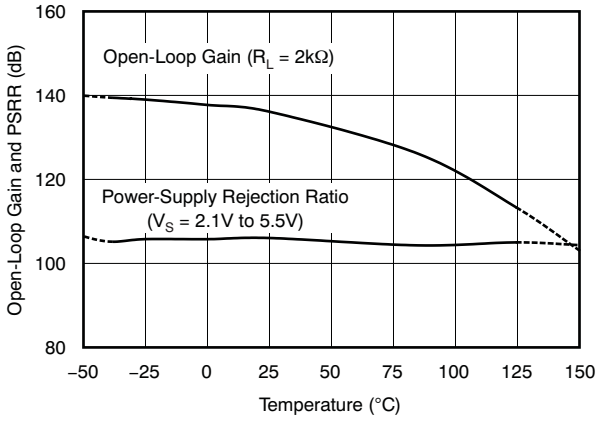


Figure 3.

0.1Hz to 10Hz INPUT VOLTAGE NOISE

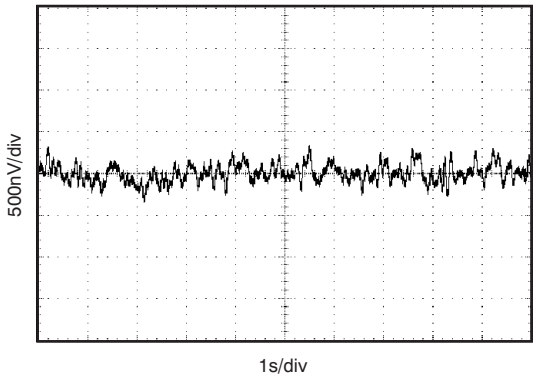


Figure 4.

INPUT VOLTAGE NOISE SPECTRAL DENSITY

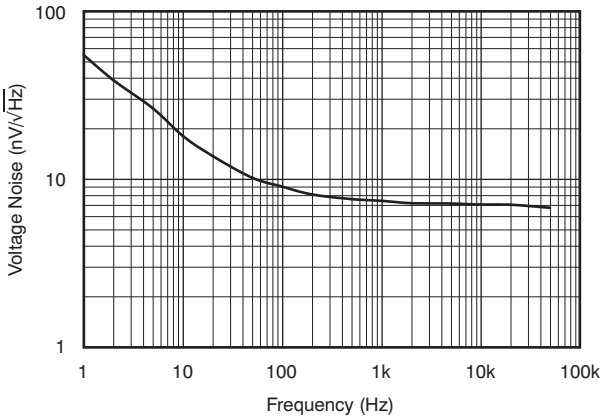


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

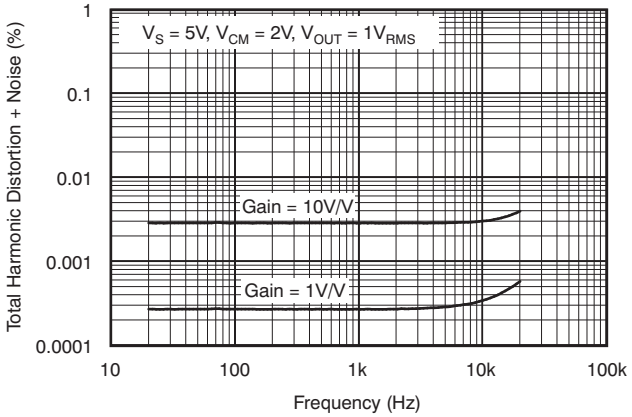


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to $V_S/2$, V_{CM} = $V_S/2$, and $V_{O\ UT}$ = $V_S/2$, unless otherwise noted.

COMMON-MODE REJECTION RATIO vs TEMPERATURE

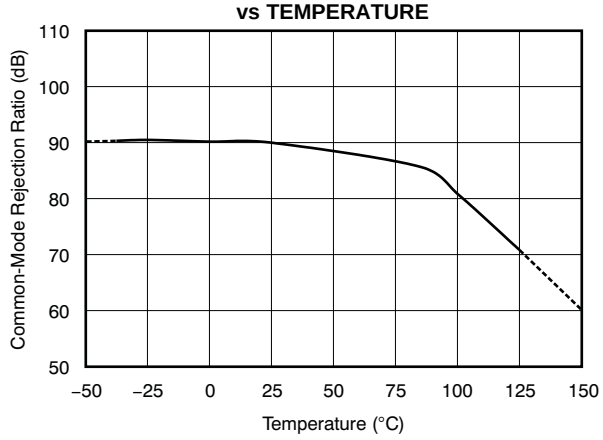


Figure 7.

QUIESCENT CURRENT vs TEMPERATURE

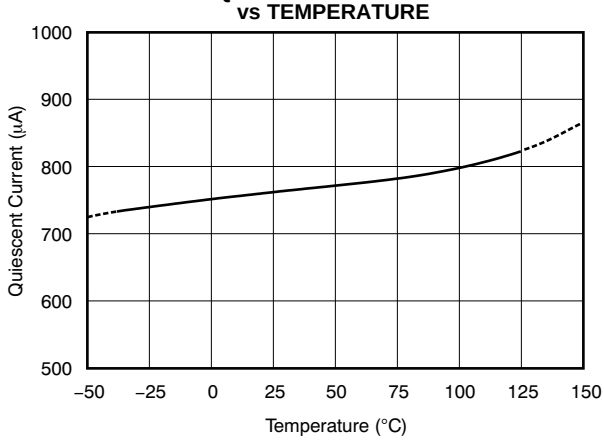


Figure 8.

QUIESCENT AND SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE

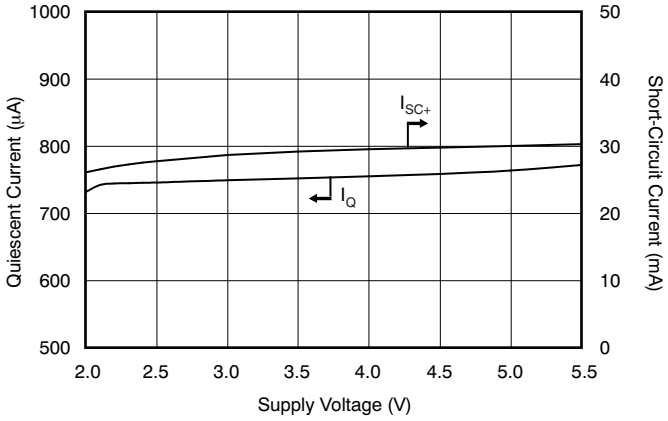


Figure 9.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

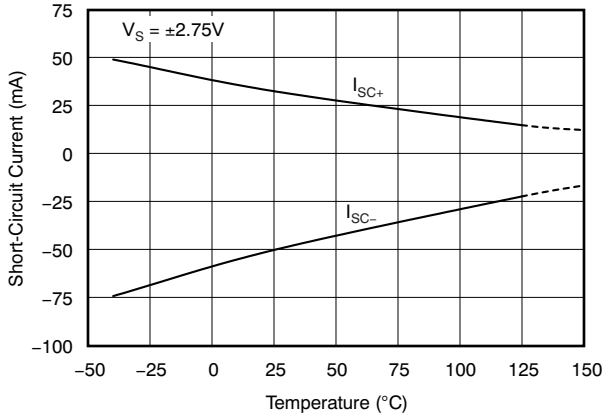


Figure 10.

INPUT BIAS CURRENT vs TEMPERATURE

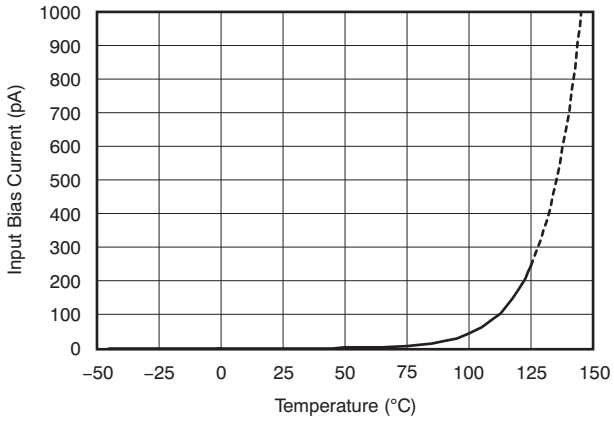


Figure 11.

OUTPUT VOLTAGE vs OUTPUT CURRENT

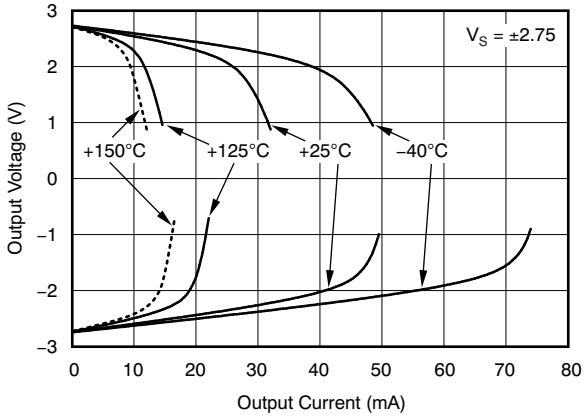


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to $V_S/2$, V_{CM} = $V_S/2$, and $V_{O\ UT}$ = $V_S/2$, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

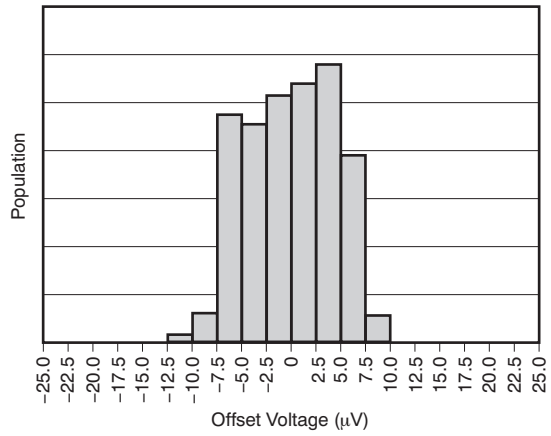


Figure 13.

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION (–40°C to +125°C)

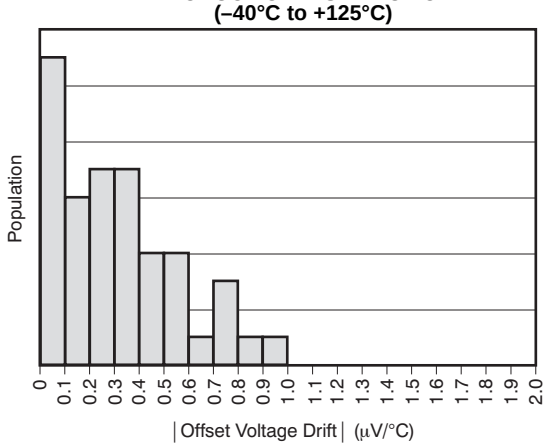


Figure 14.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

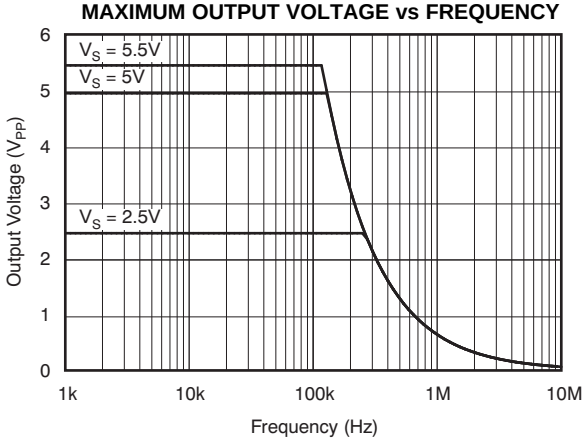


Figure 15.

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

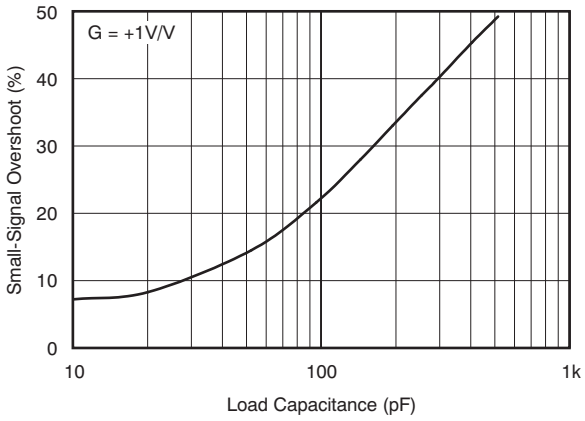


Figure 16.

SMALL-SIGNAL PULSE RESPONSE

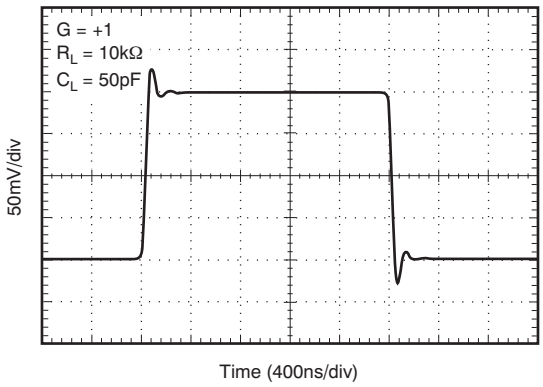


Figure 17.

LARGE-SIGNAL PULSE RESPONSE

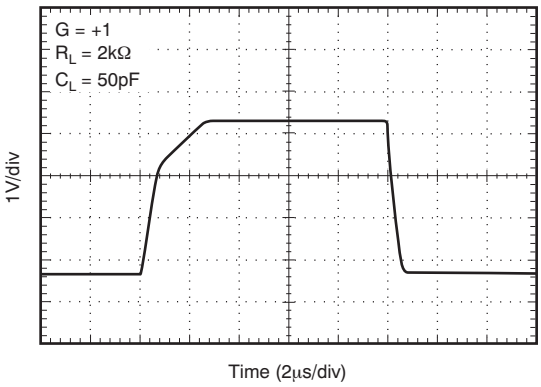


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to $V_S/2$, V_{CM} = $V_S/2$, and $V_{O\ UT}$ = $V_S/2$, unless otherwise noted.

SETTLING TIME vs CLOSED-LOOP GAIN

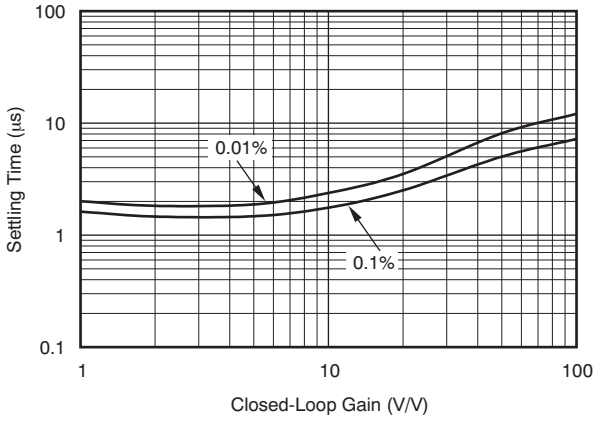


Figure 19.

CHANNEL SEPARATION vs FREQUENCY

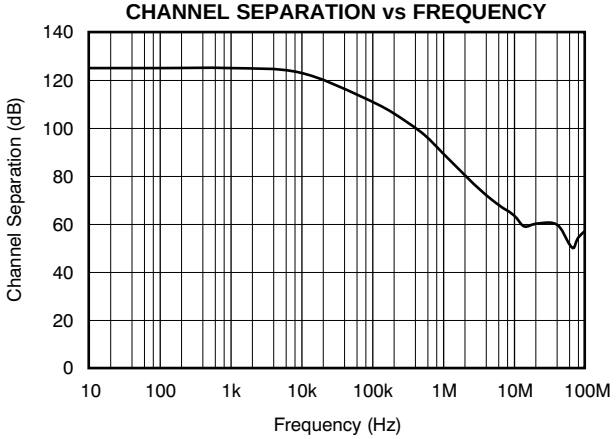


Figure 20.

OPEN-LOOP OUTPUT RESISTANCE vs FREQUENCY

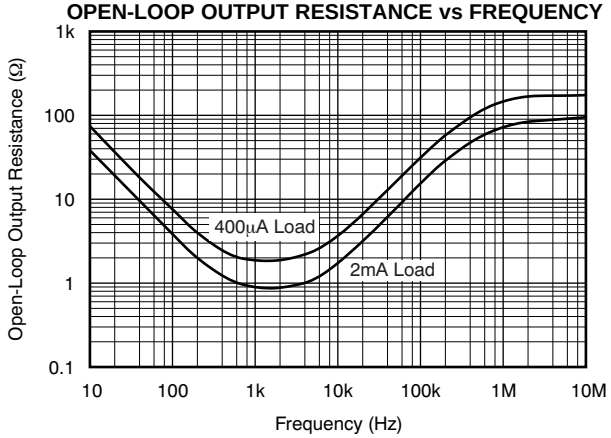


Figure 21.

APPLICATION INFORMATION

The OPA376 family of operational amplifiers is built using *e-trim*, a proprietary technique in which offset voltage is adjusted during the final steps of manufacturing. This technique compensates for performance shifts that can occur during the molding process. Through *e-trim*, the OPA376 family delivers excellent offset voltage (5µV, typ). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and A_{OL}. These 5.5MHz CMOS op amps operate on 760µA (typ) quiescent current.

OPERATING CHARACTERISTICS

The OPA376 family of amplifiers has parameters that are fully specified from 2.2V to 5.5V (±1.1V to ±2.75V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

GENERAL LAYOUT GUIDELINES

For best operational performance of the device, good printed circuit board (PCB) layout practices are required. Low-loss, 0.1µF bypass capacitors must be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

BASIC AMPLIFIER CONFIGURATIONS

The OPA376 family is unity-gain stable. It does not exhibit output phase inversion when the input is overdriven. A typical single-supply connection is shown in Figure 22. The OPA376 is configured as a basic inverting amplifier with a gain of –10V/V. This single-supply connection has an output centered on the common-mode voltage, V_{CM}. For the circuit shown, this voltage is 2.5V, but may be any value within the common-mode input voltage range.

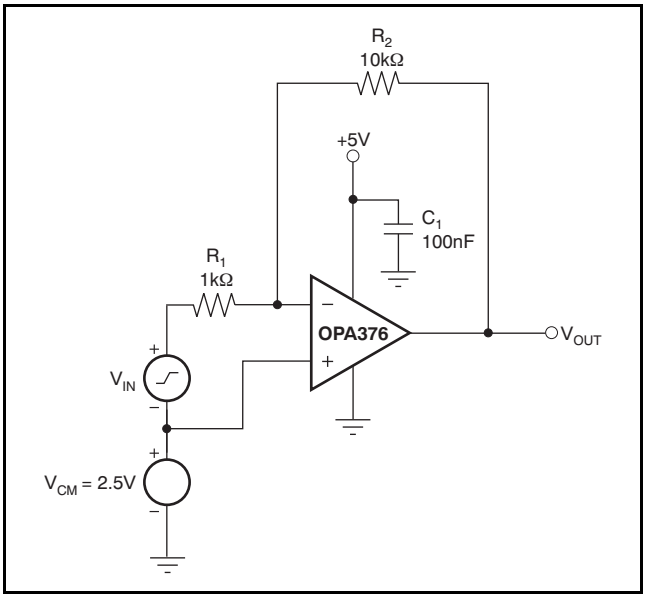


Figure 22. Basic Single-Supply Connection

COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPA376 series extends 100mV beyond the supply rails. The offset voltage of the amplifier is very low, from approximately (V–) to (V+) – 1V, as shown in Figure 23. The offset voltage increases as common-mode voltage exceeds (V+) –1V. Common-mode rejection is specified from (V–) to (V+) – 1.3V.

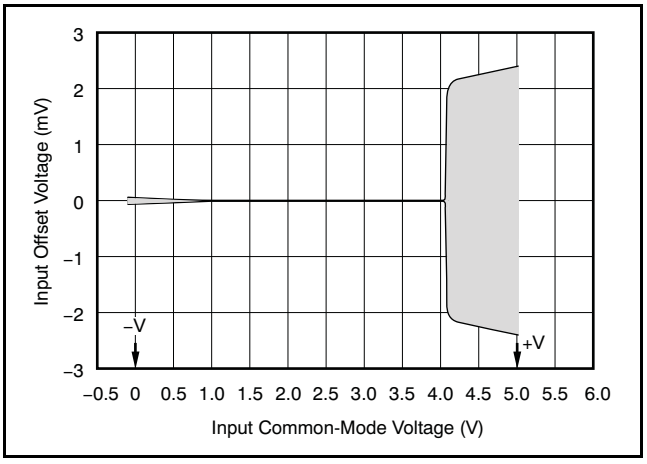


Figure 23. Offset and Common-Mode Voltage

INPUT AND ESD PROTECTION

The OPA376 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10mA as stated in the Absolute Maximum Ratings. Figure 24 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

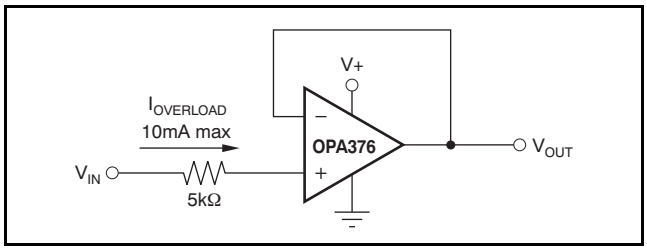


Figure 24. Input Current Protection

CAPACITIVE LOAD AND STABILITY

The OPA376 series of amplifiers may be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPAx376 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation. An op amp in the unity-gain (+1V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

The OPAx376 in a unity-gain configuration can directly drive up to 250pF pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see the typical characteristic plot, *Small-Signal Overshoot vs Capacitive Load*. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10Ω to 20Ω) resistor, R_S, in series with the output, as shown in Figure 25. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S/R_L, and is generally negligible at low output current levels.

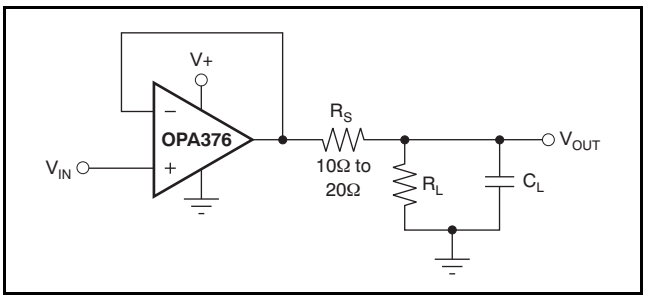


Figure 25. Improving Capacitive Load Drive

ACTIVE FILTERING

The OPA376 series is well-suited for filter applications requiring a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 26 shows a 50kHz, 2nd-order, low-pass filter. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40dB/dec. The Butterworth response is ideal for applications requiring predictable gain characteristics such as the anti-aliasing filter used ahead of an analog-to-digital converter (ADC).

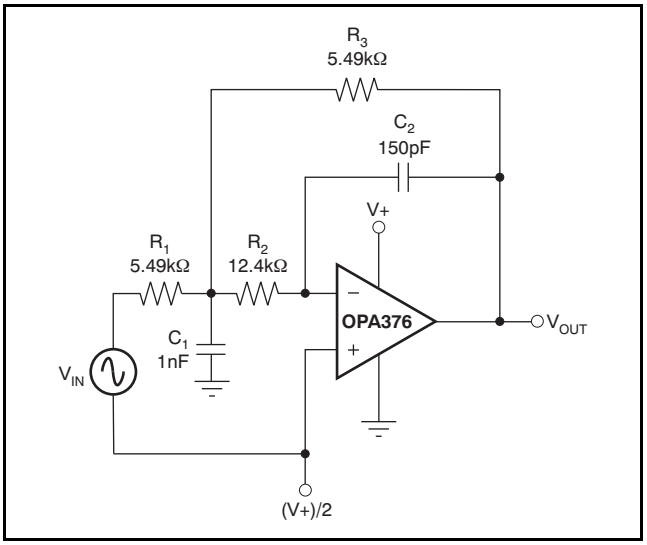


Figure 26. Second-Order Butterworth 50kHz Low-Pass Filter

OPA2376 WCSP PACKAGE

The OPA2376YZD is a lead- (PB-) free, die-level, wafer chip-scale package (WCSP). Unlike devices that are in plastic packages, these devices have no molding compound, lead frame, wire bonds, or leads. Using standard surface-mount assembly procedures, the WCSP can be mounted to a PCB without additional underfill. Figure 27 and Figure 28 detail the pinout and package marking. See the *NanoStar™ and NanoFree™ 300µm Solder Bump WCSP* Application Note (SBVA017) for more detailed information on package characteristics and PCB design.

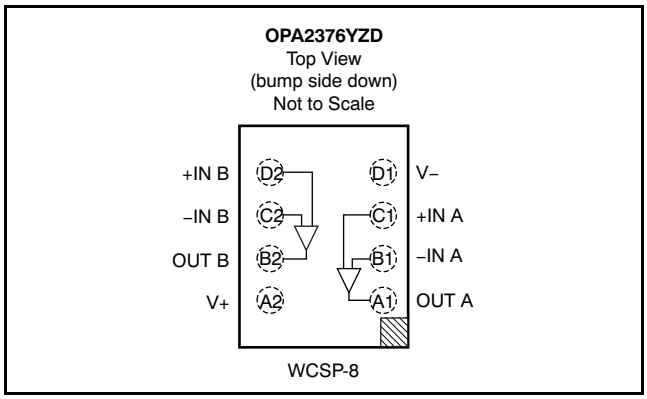


Figure 27. Pin Description

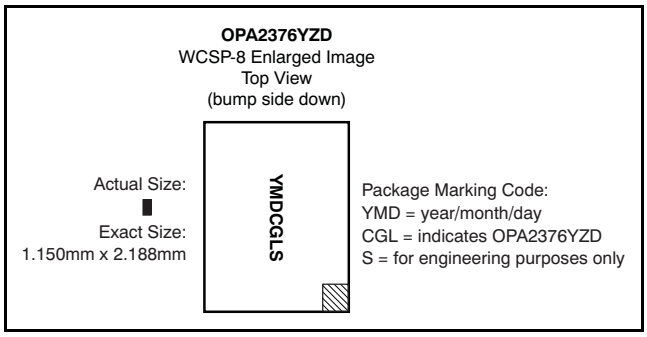


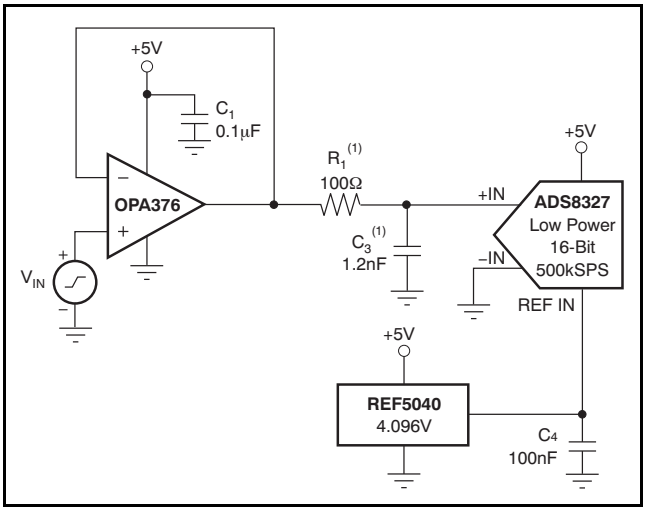
Figure 28. Top View Package Marking

PHOTOSENSITIVITY

Although the OPA2376YZD package has a protective backside coating that reduces the amount of light exposure on the die, unless fully shielded, ambient light can reach the active region of the device. Input bias current for the package is specified in the absence of light. Depending on the amount of light exposure in a given application, an increase in bias current, and possible increases in offset voltage should be expected. Fluorescent lighting may introduce noise or hum because of the time-varying light output. Best layout practices include end-product packaging that provides shielding from possible light sources during operation.

DRIVING AN ANALOG-TO-DIGITAL CONVERTER

The low noise and wide gain bandwidth of the OPA376 family make it an ideal driver for ADCs. Figure 29 illustrates the OPA376 driving an ADS8327, 16-bit, 250kSPS converter. The amplifier is connected as a unity-gain, noninverting buffer.



NOTE: (1) Suggested value; may require adjustment based on specific application.

Figure 29. Driving an ADS8327

PHANTOM-POWERED MICROPHONE

The circuit shown in Figure 30 depicts how a remote microphone amplifier can be powered by a phantom source on the output side of the signal cable. The cable serves double duty, carrying both the differential output signal from and dc power to the microphone amplifier stage.

An OPA2376 serves as a single-ended input to a differential output amplifier with a 6dB gain. Common-mode bias for the two op amps is provided by the dc voltage developed across the electret microphone element. A 48V phantom supply is reduced to 5.1V by the series 6.8kΩ resistors on the output side of the cable, and the 4.7kΩ and zener diode on the input side of the cable. AC coupling blocks the different dc voltage levels from each other on each end of the cable.

An INA163 instrumentation amplifier provides differential inputs and receives the balanced audio signals from the cable.

The INA163 gain may be set from 0dB to 80dB by selecting the R_G value. The INA163 circuit is typical of the input circuitry used in mixing consoles.

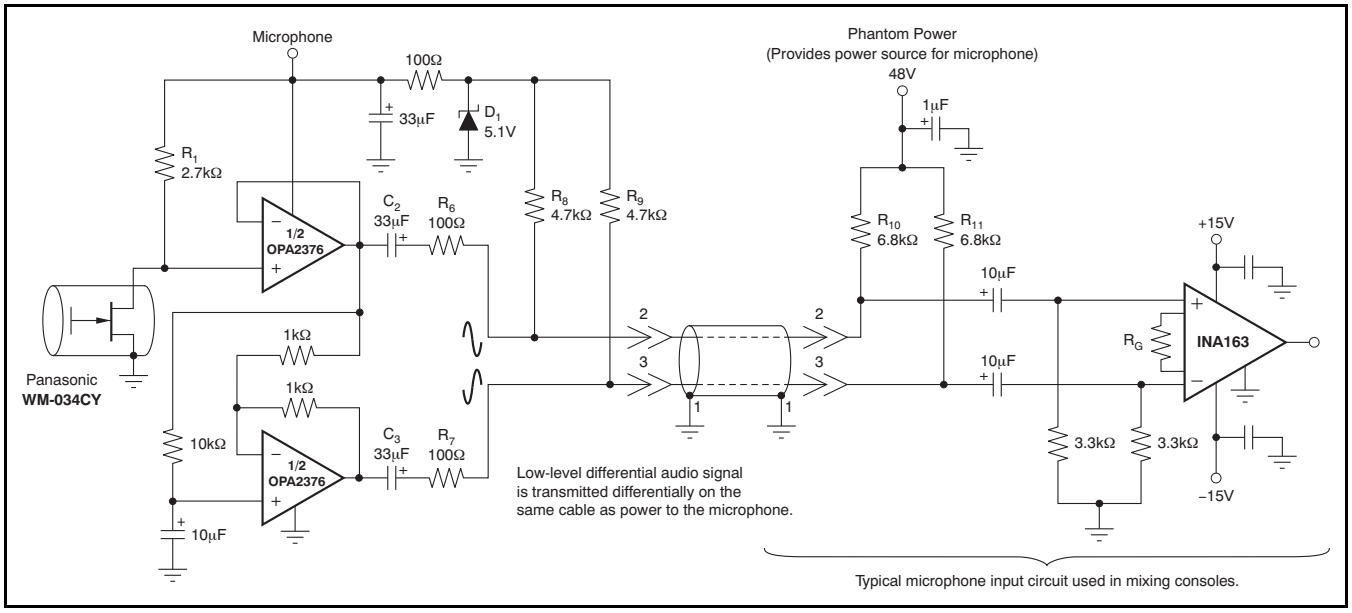
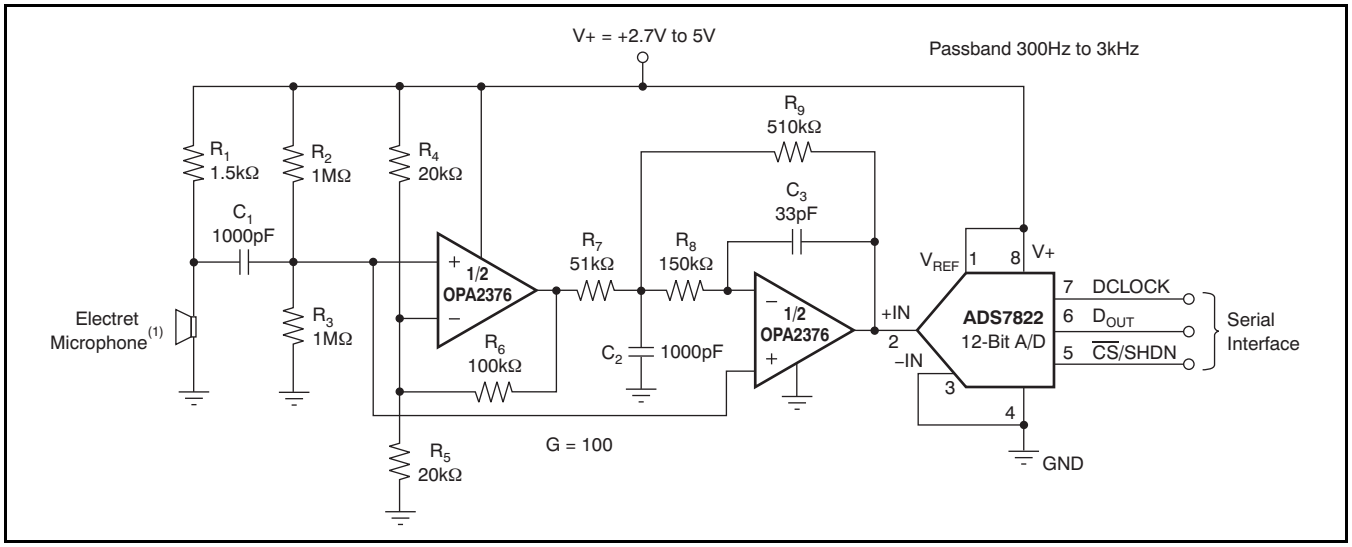


Figure 30. Phantom-Powered Electret Microphone



NOTE: (1) Electret microphone powered by R_1.

Figure 31. OPA2376 as a Speech Bandpass Filtered Data Acquisition System

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2013) to Revision F — **Page**

- Changed unit (typo) for Quiescent Current feature bullet 1
- Changed TSSOP-14 pinout for OPA4376 5

Changes from Revision D (August 2010) to Revision E — **Page**

- Changed rail-to-rail feature bullet to show input and output 1
- Changed description text to show rail-to-rail input and output 1

Changes from Revision C (October 2008) to Revision D — **Page**

- Updated format of *Electrical Characteristics* table 3
- Updated Figure 11 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA2376AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2376	Samples
OPA2376AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2376	Samples
OPA2376AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBBI	Samples
OPA2376AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBBI	Samples
OPA2376AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBBI	Samples
OPA2376AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBBI	Samples
OPA2376AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2376	Samples
OPA2376AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2376	Samples
OPA2376AIYZDR	ACTIVE	DSBGA	YZD	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	OPA2376	Samples
OPA2376AIYZDT	ACTIVE	DSBGA	YZD	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	OPA2376	Samples
OPA376AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 376	Samples
OPA376AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUQ	Samples
OPA376AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUQ	Samples
OPA376AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUQ	Samples
OPA376AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUQ	Samples
OPA376AIDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUR	Samples
OPA376AIDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUR	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA376AIDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUR	Samples
OPA376AIDCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUR	Samples
OPA376AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 376	Samples
OPA376AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 376	Samples
OPA376AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 376	Samples
OPA4376AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4376	Samples
OPA4376AIPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4376	Samples
OPA4376AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4376	Samples
OPA4376AIPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4376	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF OPA376 :

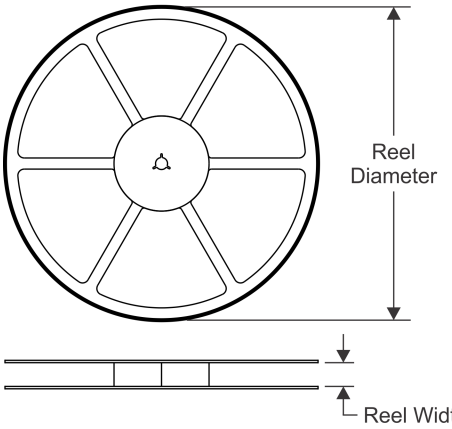
- Automotive: OPA376-Q1

NOTE: Qualified Version Definitions:

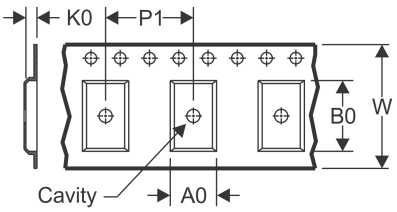
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

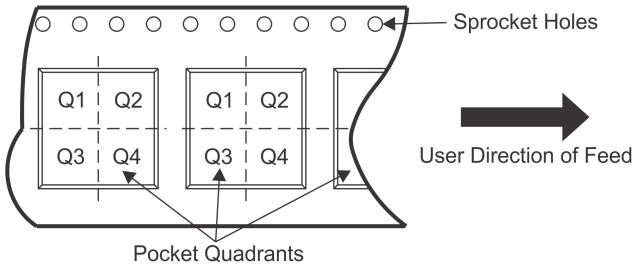


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

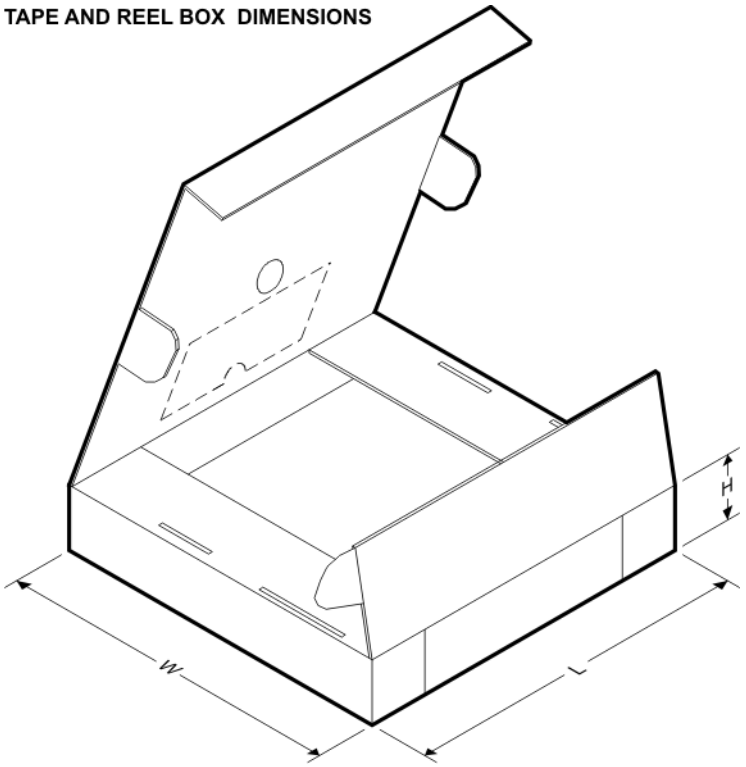
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2376AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2376AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2376AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2376AIYZDR	DSBGA	YZD	8	3000	180.0	8.4	1.24	2.29	0.81	4.0	8.0	Q1
OPA2376AIYZDR	DSBGA	YZD	8	3000	180.0	8.4	1.24	2.29	0.81	4.0	8.0	Q1
OPA2376AIYZDT	DSBGA	YZD	8	250	180.0	8.4	1.24	2.29	0.81	4.0	8.0	Q1
OPA2376AIYZDT	DSBGA	YZD	8	250	180.0	8.4	1.24	2.29	0.81	4.0	8.0	Q1
OPA376AIDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA376AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA376AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA376AIDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA376AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA376AIDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA376AIDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA376AIDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA376AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4376AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

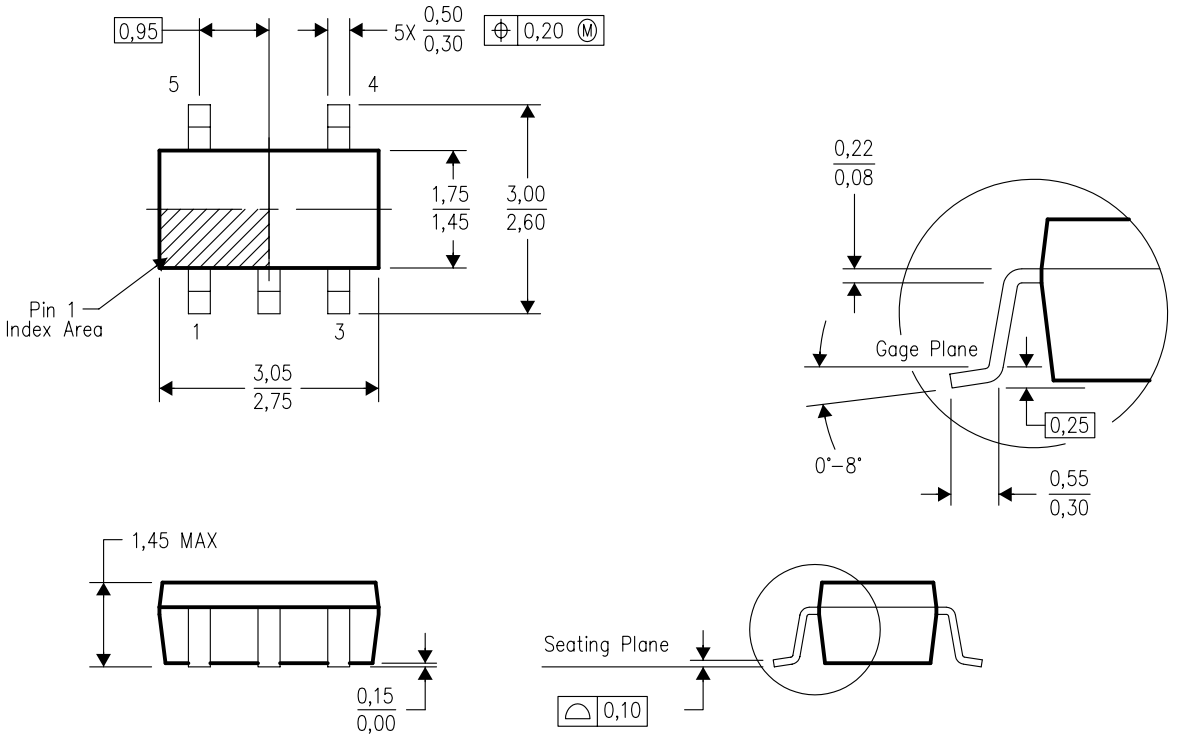
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2376AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2376AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2376AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA2376AIYZDR	DSBGA	YZD	8	3000	220.0	220.0	34.0
OPA2376AIYZDR	DSBGA	YZD	8	3000	210.0	185.0	35.0
OPA2376AIYZDT	DSBGA	YZD	8	250	220.0	220.0	34.0
OPA2376AIYZDT	DSBGA	YZD	8	250	210.0	185.0	35.0
OPA376AIDBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0
OPA376AIDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
OPA376AIDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
OPA376AIDBVT	SOT-23	DBV	5	250	195.0	200.0	45.0
OPA376AIDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA376AIDCKR	SC70	DCK	5	3000	195.0	200.0	45.0
OPA376AIDCKT	SC70	DCK	5	250	180.0	180.0	18.0
OPA376AIDCKT	SC70	DCK	5	250	195.0	200.0	45.0
OPA376AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA4376AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

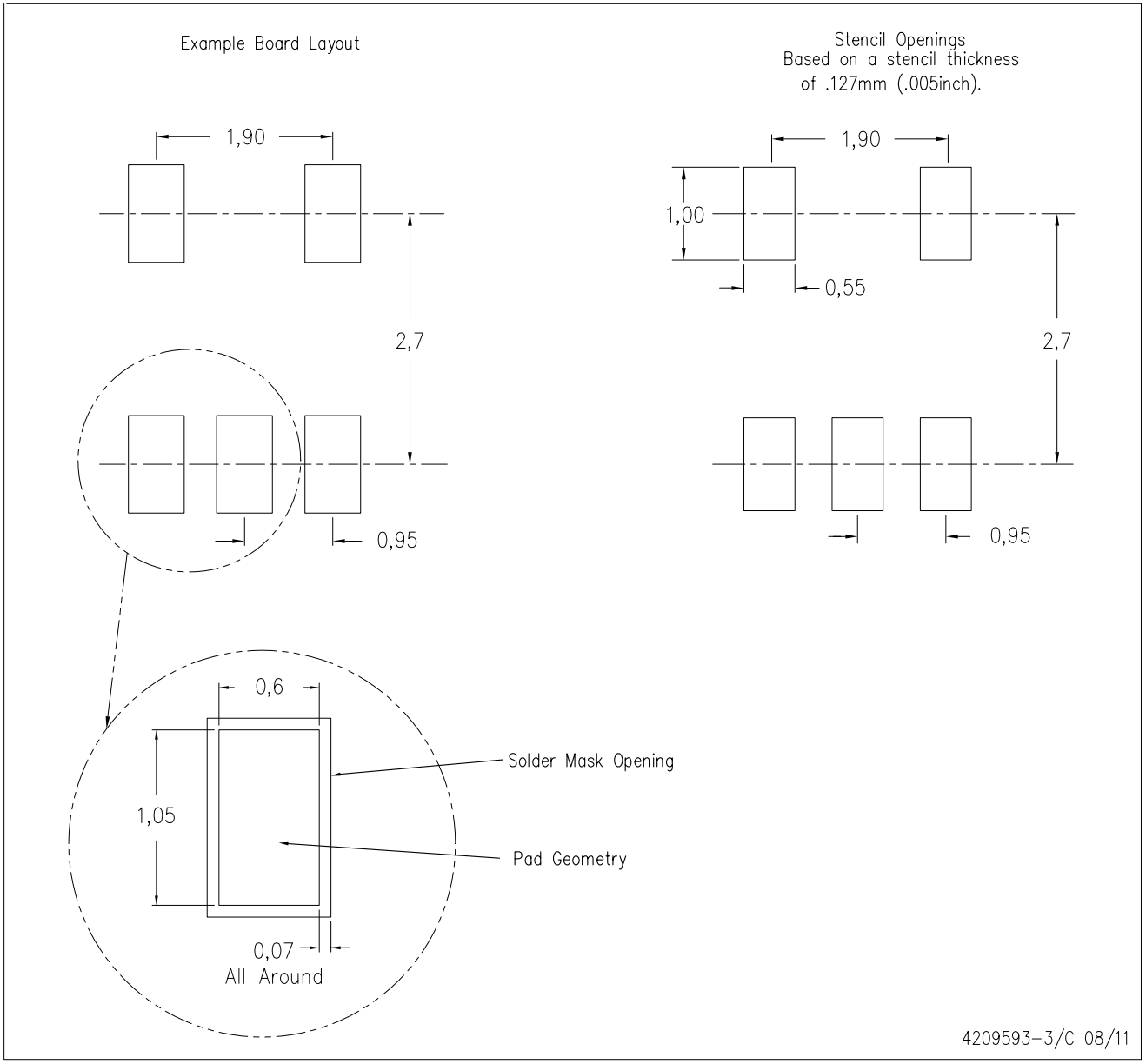
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

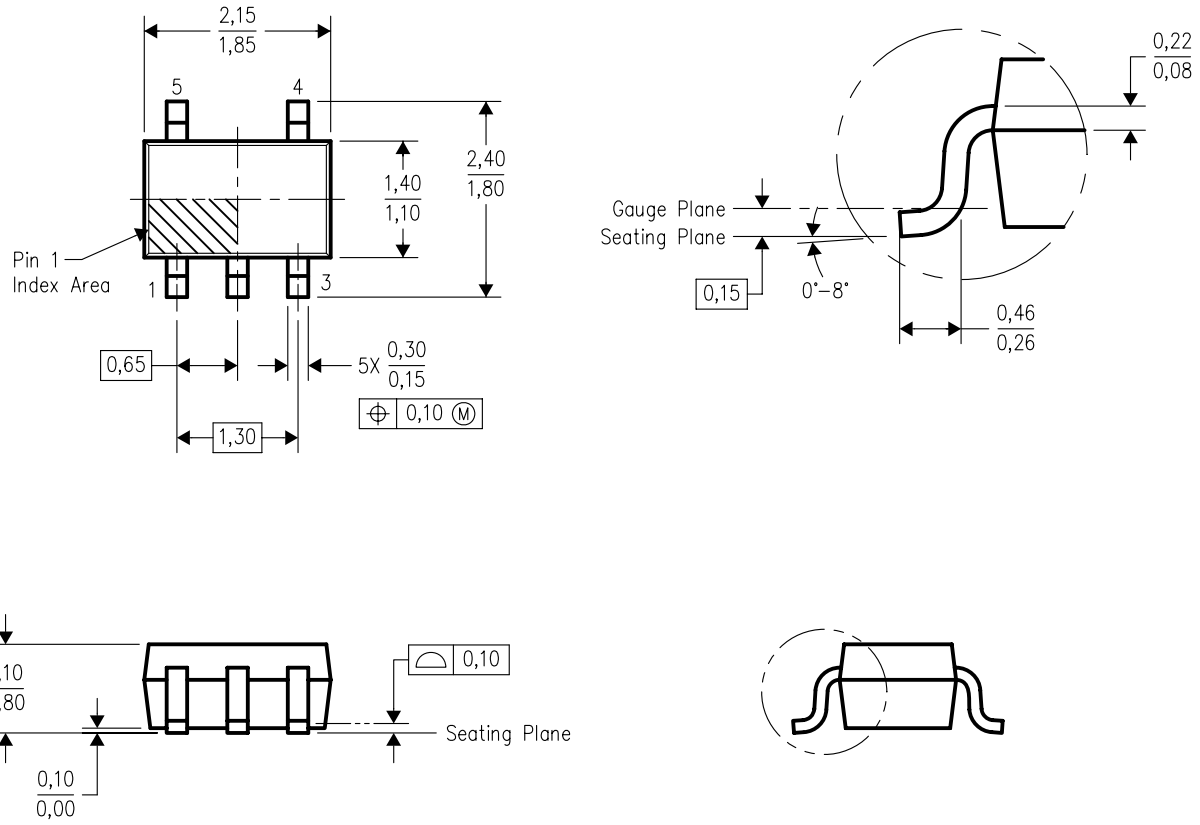
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

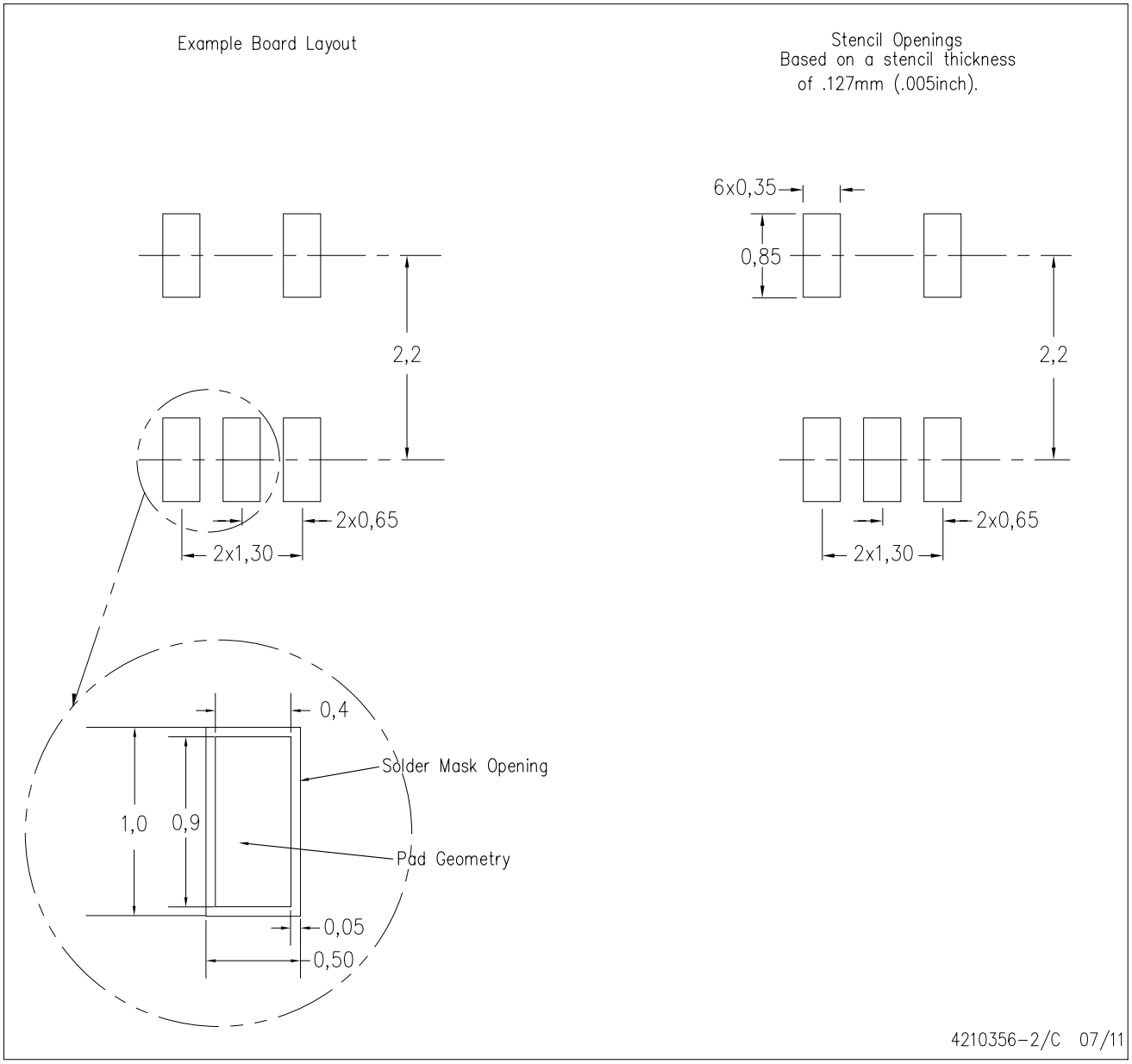
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

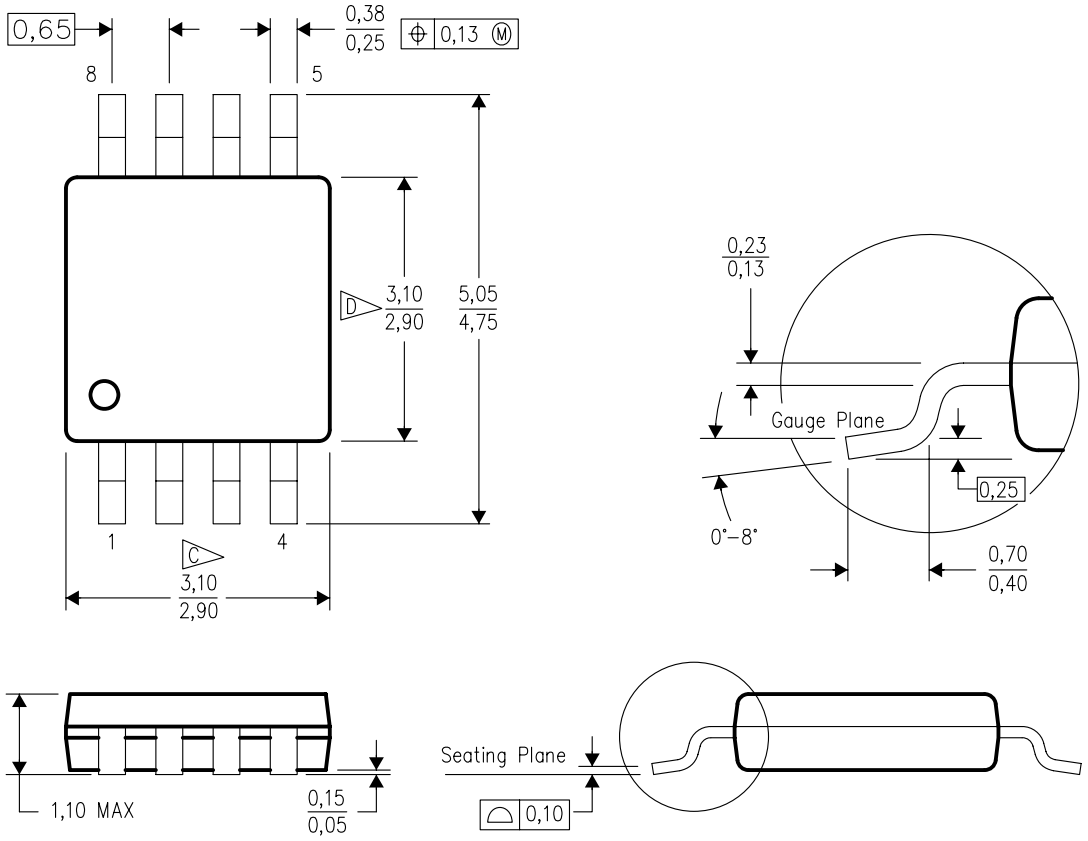
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

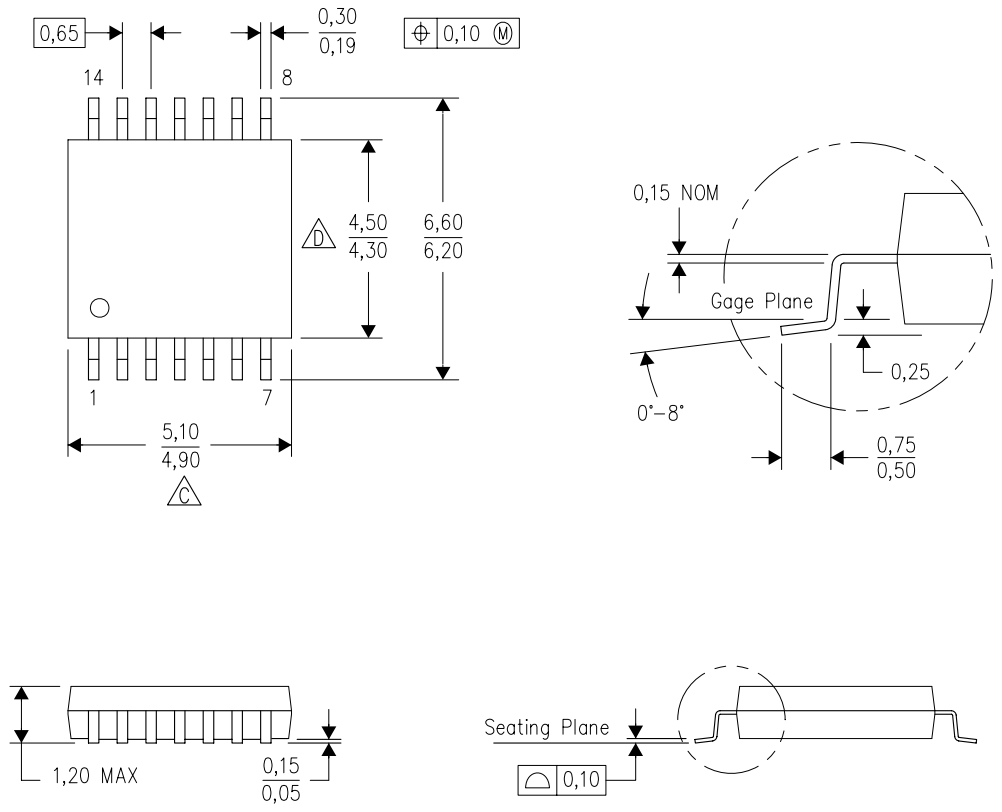
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

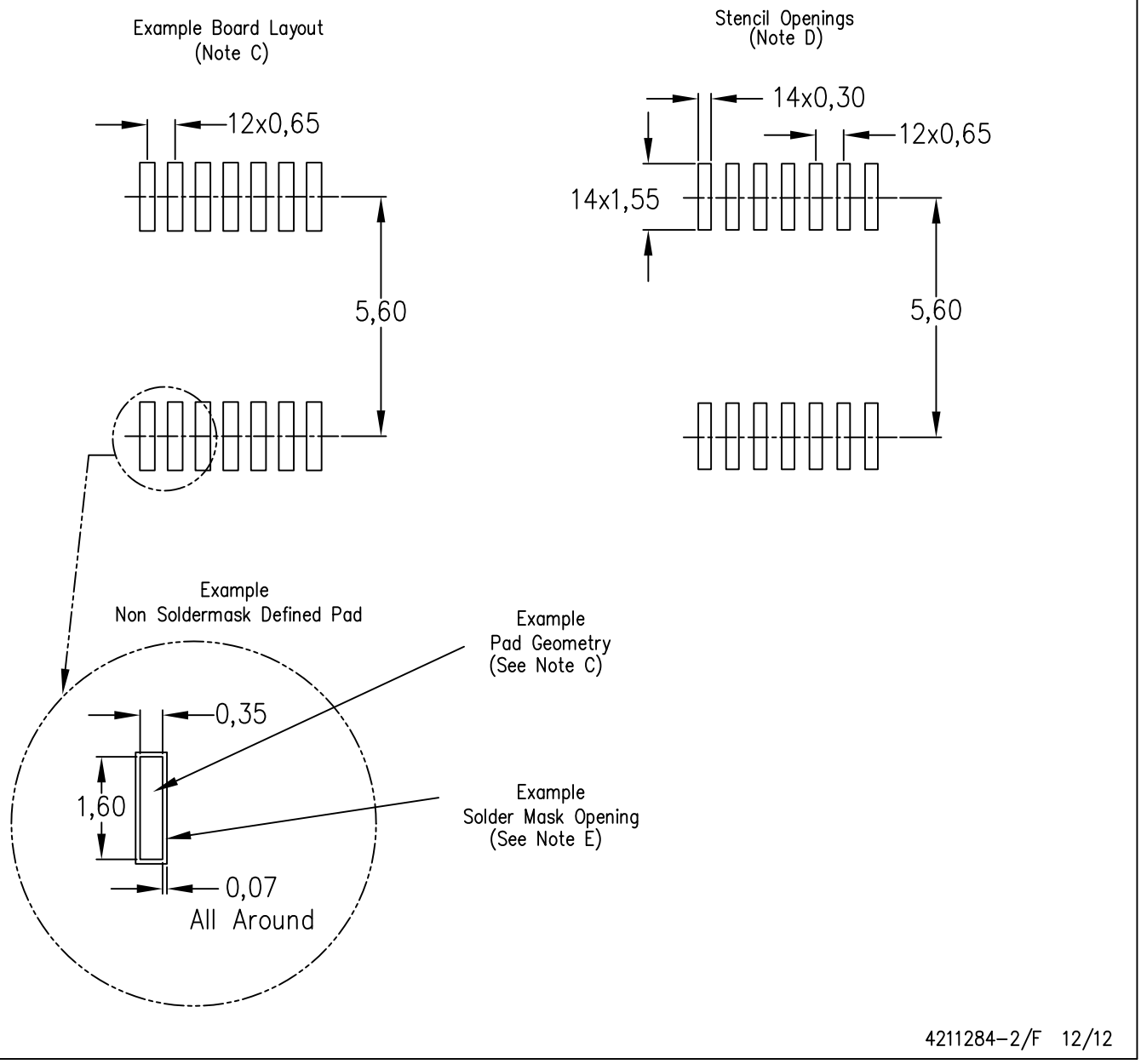
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

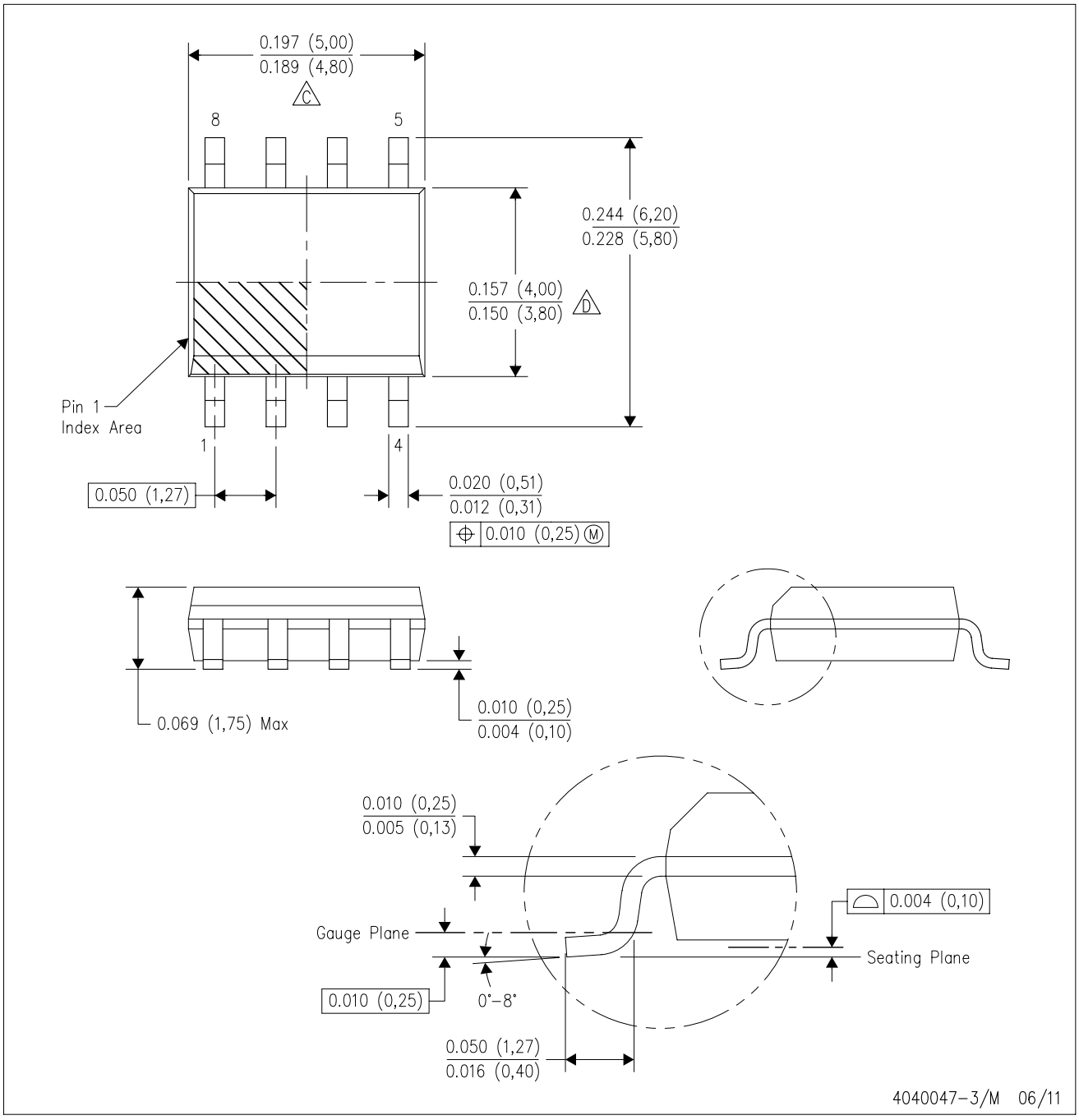
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



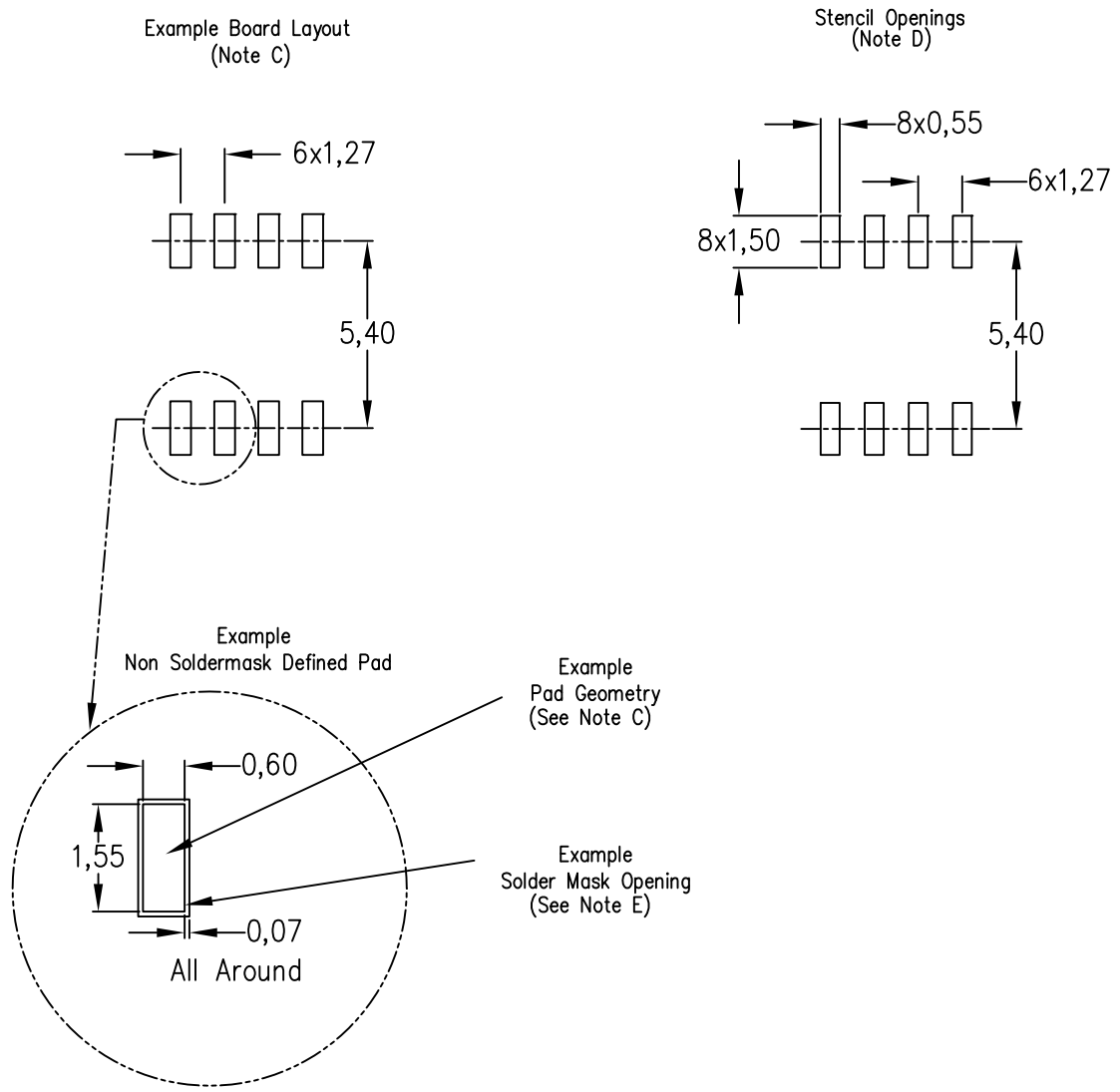
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



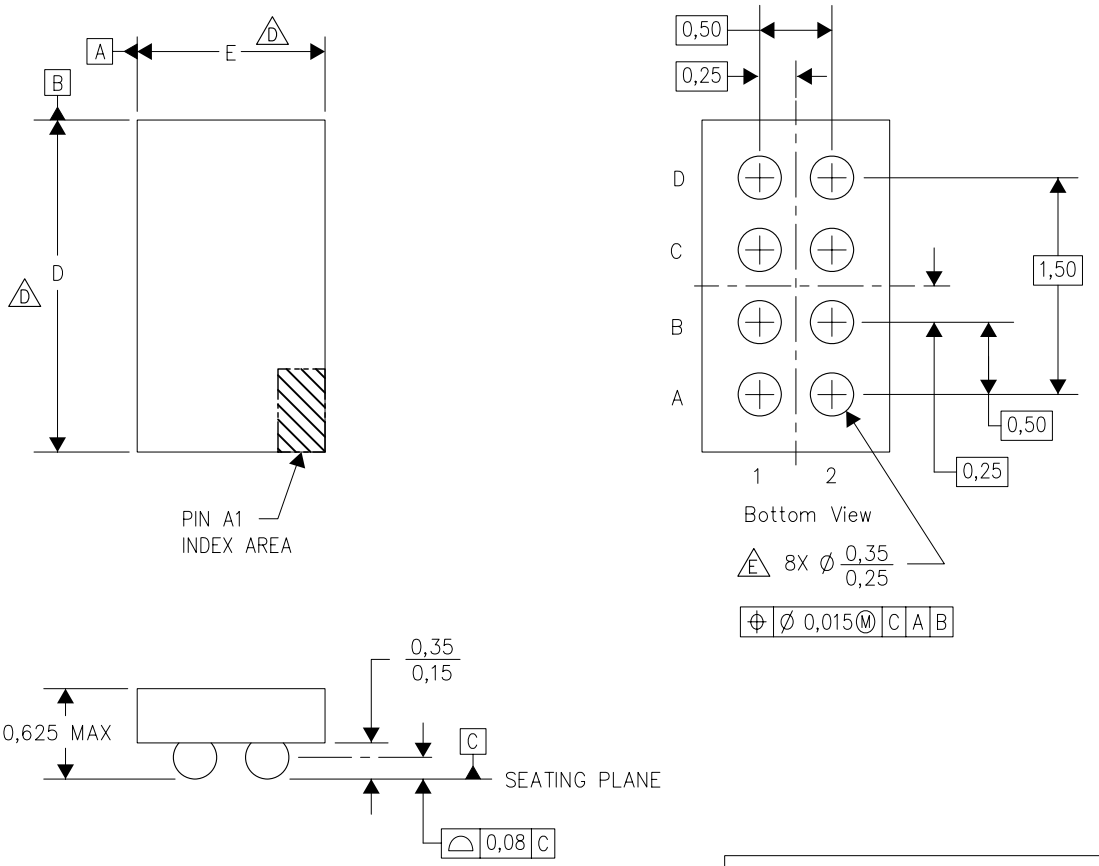
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZD (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



D: Max = 2.178 mm, Min =2.118 mm

E: Max = 1.14 mm, Min = 1.08 mm

4205057/E 08/08

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZD package can have dimension D ranging from 1.94 to 2.65 mm and dimension E ranging from 0.94 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 4 x 2 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YED (Drawing #4204180) for tin–lead (SnPb) balls.

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