

# Dual, Wideband, High Output Current Operational Amplifier

## FEATURES

- WIDEBAND +12V OPERATION: 200MHz (G = +4)
- UNITY-GAIN STABLE: 220MHz (G = +1)
- HIGH OUTPUT CURRENT: 500mA
- OUTPUT VOLTAGE SWING:  $\pm 5V$
- HIGH SLEW RATE: 1800V/ $\mu s$
- LOW SUPPLY CURRENT: 18mA
- FLEXIBLE SUPPLY RANGE:
  - +5 to +12V Single Supply
  - $\pm 2.5$  to  $\pm 6V$  Dual Supplies

## APPLICATIONS

- xDSL LINE DRIVER
- CABLE MODEM DRIVER
- MATCHED I/Q CHANNEL AMPLIFIER
- BROADBAND VIDEO LINE DRIVER
- ARB LINE DRIVER
- POWER LINE MODEM
- HIGH CAP LOAD DRIVER

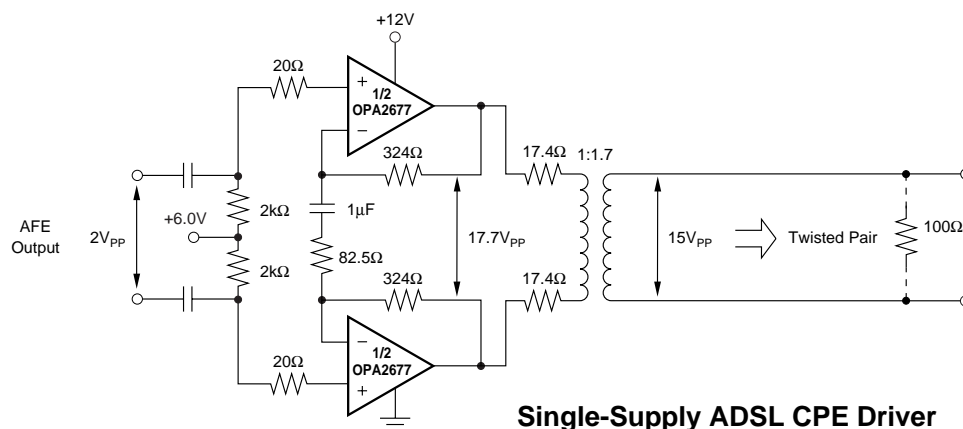
## DESCRIPTION

The OPA2677 provides the high output current and low distortion required in emerging xDSL and Power Line Modem driver applications. Operating on a single +12V supply, the OPA2677 consumes a low 9mA/ch quiescent current to deliver a very high 500mA output current. This output current supports even the most demanding ADSL CPE requirements with > 380mA minimum output current (+25°C minimum value) with low harmonic distortion. Differential driver applications will deliver < -85dBc distortion at the peak upstream power levels of full rate ADSL. The high 200MHz bandwidth will also support the most demanding VDSL line driver requirements.

Specified on  $\pm 6V$  supplies (to support +12V operation), the OPA2677 will also support a single +5V or dual  $\pm 5V$  supply. Video applications will benefit from its very high output current to drive up to 10 parallel video loads (15 $\Omega$ ) with < 0.1%/0.1° dG/dP nonlinearity.

## OPA2677 RELATED PRODUCTS

SINGLES	DUALS	TRIPLES	NOTES
OPA691	OPA2691	OPA3691	Single +12V Capable
—	THS6042	—	$\pm 15V$ Capable
—	OPA2674	—	Single +12V Capable with current limit



Single-Supply ADSL CPE Driver



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Power Supply .....	$\pm 6.5V_{DC}$
Internal Power Dissipation .....	See Thermal Characteristics
Differential Input Voltage .....	$\pm 1.2V$
Input Common-Mode Voltage Range .....	$\pm V_S$
Storage Temperature Range: U, H, T, E .....	$-40^{\circ}C$ to $+125^{\circ}C$
Lead Temperature (soldering, 10s) .....	$+300^{\circ}C$
Junction Temperature ( $T_J$ ) .....	$+150^{\circ}C$
ESD Rating:	
Human Body Model (HBM) <sup>(2)</sup> .....	2000V
Charge Device Model (CDM) .....	1000V
Machine Model (MM) .....	100V

- NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.
- (2) Pins 2 and 6 on SO-8 package, and pins 2 and 5 on SO-16 package > 500V HBM.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

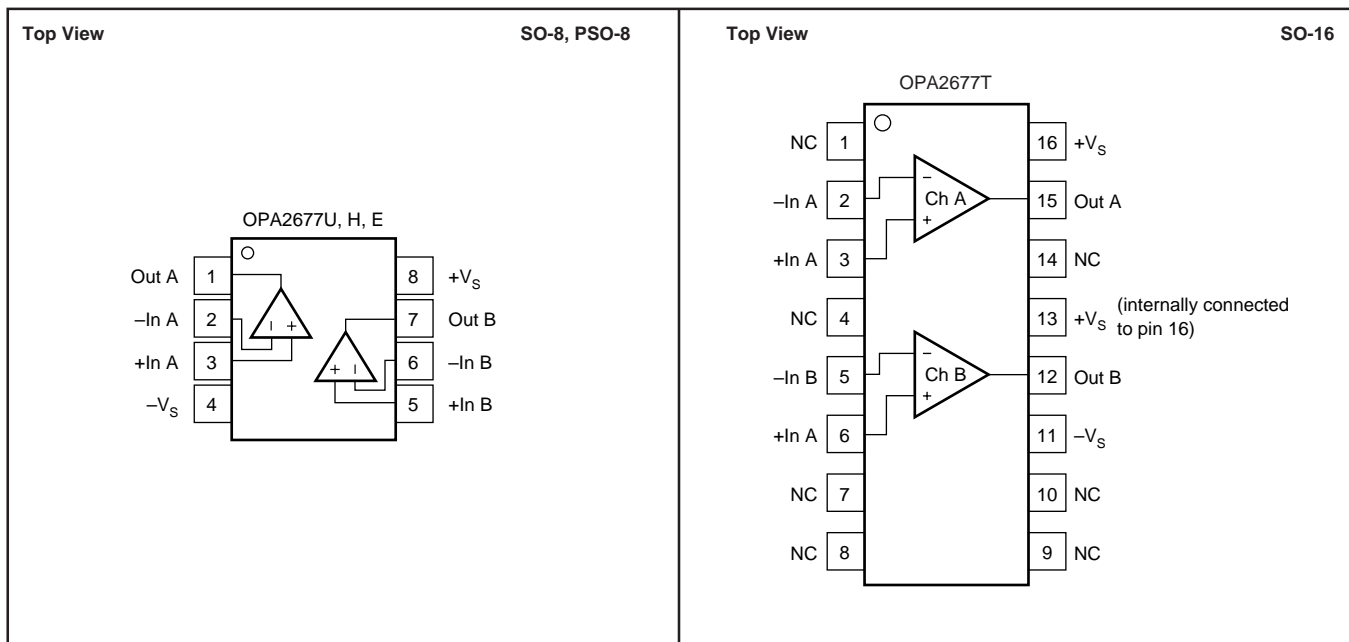
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR <sup>(1)</sup>	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2677	SO-8	D	$-40^{\circ}C$ to $+85^{\circ}C$	OPA2677U	OPA2677U	Rails, 100
"	"	"	"	"	OPA2677U/2K5	Tape and Reel, 2500
OPA2677	PSO-8	DTJ	$-40^{\circ}C$ to $+85^{\circ}C$	OPA2677H	OPA2677H	Rails, 100
"	"	"	"	"	OPA2677H/2K5	Tape and Reel, 2500
OPA2677	SO-16	D	$-40^{\circ}C$ to $+85^{\circ}C$	OPA2677T	OPA2677T	Rails, 48
					OPA2677T/2K5	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at [www.ti.com](http://www.ti.com).

## PIN CONFIGURATIONS



# ELECTRICAL CHARACTERISTICS: $V_S = \pm 6V$

**Boldface limits are tested at +25°C.**

At  $T_A = +25^\circ\text{C}$ ,  $G = +4$ ,  $R_F = 402\Omega$ , and  $R_L = 100\Omega$ , unless otherwise noted. See Figure 1 for AC performance only.

PARAMETER	CONDITIONS	OPA2677U, H, T						TEST LEVEL <sup>(3)</sup>
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C <sup>(1)</sup>	0°C to 70°C <sup>(2)</sup>	-40°C to +85°C <sup>(2)</sup>	UNITS	MIN/MAX	
<b>AC PERFORMANCE (see Figure 1)</b>								
Small-Signal Bandwidth ( $V_O = 0.5V_{PP}$ )	$G = +1$ , $R_F = 511\Omega$	220				MHz	min	B
	$G = +2$ , $R_F = 475\Omega$	200	170	168	165	MHz	min	B
	$G = +4$ , $R_F = 402\Omega$	200	170	168	165	MHz	min	B
	$G = +8$ , $R_F = 250\Omega$	250	225	205	200	MHz	min	B
Peaking at a Gain of +1	$G = +1$ , $R_F = 511\Omega$	0				dB	typ	C
Bandwidth for 0.1dB Gain Flatness	$G = +4$ , $V_O = 0.5V_{PP}$	80	36	32	30	MHz	min	B
Large-Signal Bandwidth	$G = +4$ , $V_O = 5V_{PP}$	200				MHz	typ	C
Slew Rate	$G = +4$ , 5V Step	2000	1500	1450	1400	V/ $\mu\text{s}$	min	B
Rise-and-Fall Time	$G = +4$ , $V_O = 2V$ Step	1.75				ns	typ	C
Harmonic Distortion	$G = +4$ , $f = 5\text{MHz}$ , $V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 100\Omega$	-72	-70	-69	-68	dBc	max	B
	$R_L \geq 500\Omega$	-82	-80	-79	-78	dBc	max	B
3rd-Harmonic	$R_L = 100\Omega$	-96	-92	-91	-90	dBc	max	B
	$R_L \geq 500\Omega$	-99	-95	-94	-92	dBc	max	B
Input Voltage Noise	$f > 1\text{MHz}$	2	2.6	2.9	3.1	nV/ $\sqrt{\text{Hz}}$	max	B
Noninverting Input Current Noise	$f > 1\text{MHz}$	16	20	21	22	pA/ $\sqrt{\text{Hz}}$	max	B
Inverting Input Current Noise	$f > 1\text{MHz}$	24	29	30	31	pA/ $\sqrt{\text{Hz}}$	max	B
NTSC Differential Gain	NTSC, $G = +2$ , $R_L = 150\Omega$	0.03				%	typ	C
	NTSC, $G = +2$ , $R_L = 37.5\Omega$	0.05				%	typ	C
NTSC Differential Phase	NTSC, $G = +2$ , $R_L = 150\Omega$	0.01				degrees	typ	C
	NTSC, $G = +2$ , $R_L = 37.5\Omega$	0.04				degrees	typ	C
Channel-to-Channel Crosstalk	$f = 5\text{MHz}$ , Input Referred	-92				dB	typ	C
<b>DC PERFORMANCE<sup>(4)</sup></b>								
Open-Loop Transimpedance Gain	$V_O = 0V$ , $R_L = 100\Omega$	135	<b>80</b>	76	75	k $\Omega$	min	A
Input Offset Voltage	$V_{CM} = 0V$	$\pm 1.0$	<b><math>\pm 4.5</math></b>	$\pm 5$	$\pm 5.3$	mV	max	A
Average Offset Voltage Drift	$V_{CM} = 0V$	$\pm 4$	$\pm 10$	$\pm 10$	$\pm 12$	$\mu\text{V}/^\circ\text{C}$	max	B
Noninverting Input Bias Current	$V_{CM} = 0V$	$\pm 10$	<b><math>\pm 30</math></b>	$\pm 32$	$\pm 35$	$\mu\text{A}$	max	A
Average Noninverting Input Bias Current Drift	$V_{CM} = 0V$	$\pm 5$	<b><math>\pm 50</math></b>	$\pm 50$	$\pm 75$	nA/ $^\circ\text{C}$	max	B
Inverting Input Bias Current	$V_{CM} = 0V$	$\pm 10$	<b><math>\pm 35</math></b>	$\pm 40$	$\pm 45$	$\mu\text{A}$	max	A
Average Inverting Input Bias Current Drift	$V_{CM} = 0V$	$\pm 10$	<b><math>\pm 100</math></b>	$\pm 100$	$\pm 150$	nA/ $^\circ\text{C}$	max	B
<b>INPUT<sup>(4)</sup></b>								
Common-Mode Input Range (CMIR) <sup>(5)</sup>		$\pm 4.5$	<b><math>\pm 4.1</math></b>	$\pm 4.0$	$\pm 3.9$	V	min	A
Common-Mode Rejection Ratio (CMRR)	$V_{CM} = 0V$ , Input Referred	55	<b>51</b>	50	49	dB	min	A
Noninverting Input Impedance		250    2				k $\Omega$    pF	typ	C
Minimum Inverting Input Resistance	Open-Loop	22	12			$\Omega$	min	B
Maximum Inverting Input Resistance	Open-Loop	22	35			$\Omega$	max	B
<b>OUTPUT<sup>(4)</sup></b>								
Voltage Output Swing	No Load	$\pm 5.1$	<b><math>\pm 4.9</math></b>	$\pm 4.8$	$\pm 4.7$	V	min	A
	$R_L = 100\Omega$	$\pm 5.0$	<b><math>\pm 4.8</math></b>	$\pm 4.7$	$\pm 4.5$	V	min	A
	$R_L = 25\Omega$	$\pm 4.8$				V	typ	C
Current Output	$V_O = 0$	$\pm 500$	<b><math>\pm 380</math></b>	$\pm 350$	$\pm 320$	mA	min	A
Peak Current Output, Sourcing <sup>(6)</sup>	$V_O = 0$	1.2				A	typ	C
Peak Current Output, Sinking <sup>(6)</sup>	$V_O = 0$	-1.6				A	typ	C
Closed-Loop Output Impedance	$G = +4$ , $f \leq 100\text{kHz}$	0.003				$\Omega$	typ	C
<b>POWER SUPPLY</b>								
Specified Operating Voltage		$\pm 6$				V	typ	C
Maximum Operating Voltage			<b><math>\pm 6.3</math></b>	$\pm 6.3$	$\pm 6.3$	V	max	A
Maximum Quiescent Current	$V_S = \pm 6V$	18	<b>18.6</b>	18.8	19.5	mA	max	A
Minimum Quiescent Current	$V_S = \pm 6V$	18	<b>17.4</b>	16.5	16.0	mA	min	A
Power-Supply Rejection Ratio (PSRR)	$f = 100\text{kHz}$ , Input Referred	56	<b>51</b>	49	48	dB	min	A
<b>THERMAL CHARACTERISTICS</b>								
Specification: U, H, T		-40 to +85				$^\circ\text{C}$		
Thermal Resistance, $\theta_{JA}$	Junction-to-Ambient					$^\circ\text{C}/\text{W}$	typ	C
U SO-8		125				$^\circ\text{C}/\text{W}$	typ	C
H PSO-8	Exposed Slug Soldered to Board	55				$^\circ\text{C}/\text{W}$	typ	C
T SO-16		100				$^\circ\text{C}/\text{W}$	typ	C

NOTES: (1) Junction temperature = ambient for +25°C specifications.

(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.

(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

(4) Current is considered positive out of node.  $V_{CM}$  is the input common-mode voltage.

(5) Tested < 3dB below minimum CMRR specifications at  $\pm\text{CMIR}$  limits.

(6) Peak output duration should not exceed junction temperature +150°C for extended periods.

# ELECTRICAL SPECIFICATIONS: $V_S = +5V$

**Boldface limits are tested at +25°C.**

At  $T_A = +25^\circ\text{C}$ ,  $G = +4$ ,  $R_F = 402\Omega$ , and  $R_L = 100\Omega$ , unless otherwise noted. See Figure 3 for AC performance only.

PARAMETER	CONDITIONS	OPA2677U, H, T						TEST LEVEL <sup>(3)</sup>
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C <sup>(1)</sup>	0°C to 70°C <sup>(2)</sup>	-40°C to +85°C <sup>(2)</sup>	UNITS	MIN/MAX	
<b>AC PERFORMANCE (see Figure 3)</b>								
Small-Signal Bandwidth ( $V_O = 0.5V_{PP}$ )	$G = +1, R_F = 536\Omega$	160				MHz	min	B
	$G = +2, R_F = 511\Omega$	150	120	118	115	MHz	min	B
	$G = +4, R_F = 453\Omega$	150	130	128	125	MHz	min	B
	$G = +8, R_F = 332\Omega$	160	130	128	125	MHz	min	B
Peaking at a Gain of +1	$G = +1, R_F = 511\Omega$	0				dB	typ	C
Bandwidth for 0.1dB Gain Flatness	$G = +4, V_O = 0.5V_{PP}$	70	23	20	19	MHz	min	B
Large-Signal Bandwidth	$G = +4, V_O = 5V_{PP}$	100				MHz	typ	C
Slew Rate	$G = +4, 2V$ Step	1100	830	827	825	V/ $\mu\text{s}$	min	B
Rise-and-Fall Time	$G = +4, V_O = 2V$ Step	2				ns	typ	C
Harmonic Distortion	$G = +4, f = 5\text{MHz}, V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 100\Omega$	-67	-65	-64	-63	dBc	max	B
	$R_L \geq 500\Omega$	-71	-68	-67	-66	dBc	max	B
3rd-Harmonic	$R_L = 100\Omega$	-87	-82	-81	-80	dBc	max	B
	$R_L \geq 500\Omega$	-87	-82	-81	-80	dBc	max	B
Input Voltage Noise	$f > 1\text{MHz}$	2	2.6	2.9	3.1	nV/ $\sqrt{\text{Hz}}$	max	B
Noninverting Input Current Noise	$f > 1\text{MHz}$	16	20	21	22	pA/ $\sqrt{\text{Hz}}$	max	B
Inverting Input Current Noise	$f > 1\text{MHz}$	24	29	30	31	pA/ $\sqrt{\text{Hz}}$	max	B
Channel-to-Channel Crosstalk	$f = 5\text{MHz}$ , Input Referred	-92				dB	typ	C
<b>DC PERFORMANCE</b>								
Open-Loop Transimpedance Gain	$V_O = 0V, R_L = 100\Omega$	110	<b>72</b>	70	68	k $\Omega$	min	A
Input Offset Voltage	$V_{CM} = 0V$	$\pm 0.8$	<b><math>\pm 3.5</math></b>	$\pm 4.0$	$\pm 4.3$	mV	max	A
Average Offset Voltage Drift	$V_{CM} = 0V$	$\pm 4$	$\pm 10$	$\pm 10$	$\pm 12$	$\mu\text{V}/^\circ\text{C}$	max	B
Noninverting Input Bias Current	$V_{CM} = 0V$	$\pm 10$	<b><math>\pm 30</math></b>	$\pm 32$	$\pm 35$	$\mu\text{A}$	max	A
Average Noninverting Input Bias Current Drift	$V_{CM} = 0V$	$\pm 5$	<b><math>\pm 50</math></b>	$\pm 50$	$\pm 75$	nA/ $^\circ\text{C}$	max	B
Inverting Input Bias Current	$V_{CM} = 0V$	$\pm 10$	<b><math>\pm 30</math></b>	$\pm 40$	$\pm 45$	$\mu\text{A}$	max	A
Average Inverting Input Bias Current Drift	$V_{CM} = 0V$	$\pm 10$	<b><math>\pm 100</math></b>	$\pm 100$	$\pm 150$	nA/ $^\circ\text{C}$	max	B
<b>INPUT</b>								
Most Positive Input Voltage		3.7	<b>3.3</b>	3.2	3.1	V	min	A
Most Negative Input Voltage		1.3	<b>1.7</b>	1.8	1.9	V	min	A
Common-Mode Rejection Ratio (CMRR)	$V_{CM} = 2.5V$ , Input Referred	52	<b>49</b>	48	47	dB	min	A
Noninverting Input Impedance		250    2				k $\Omega$    pF	typ	C
Minimum Inverting Input Resistance	Open-Loop	25	15			k $\Omega$	min	B
Maximum Inverting Input Resistance	Open-Loop	25	40			k $\Omega$	max	B
<b>OUTPUT</b>								
Most Positive Output Voltage	No Load	4.1	<b>3.9</b>	3.8	3.6	V	min	A
	$R_L = 100\Omega$	3.5	<b>3.8</b>	3.7	3.5	V	min	A
Least Positive Output Voltage	No Load	0.8	<b>1.0</b>	1.1	1.3	V	min	A
	$R_L = 100\Omega$	1.0	<b>1.1</b>	1.2	1.5	V	min	A
Current Output	$V_O = 0$	$\pm 300$	<b><math>\pm 200</math></b>	$\pm 180$	$\pm 100$	mA	min	A
Closed-Loop Output Impedance	$G = +4, f \leq 100\text{kHz}$	0.02				$\Omega$	typ	C
<b>POWER SUPPLY</b>								
Specified Operating Voltage		+5				V	typ	C
Maximum Operating Voltage			<b>12.6</b>	12.6	12.6	V	max	A
Maximum Quiescent Current	$V_S = \pm 6V$	13.6	<b>14.8</b>	15.2	15.6	mA	max	A
Minimum Quiescent Current	$V_S = \pm 6V$	13.6	<b>12.0</b>	11.7	11.4	mA	min	A
Power-Supply Rejection Ratio (PSRR)	$f = 100\text{kHz}$ , Input Referred	52				dB	typ	C
<b>THERMAL CHARACTERISTICS</b>								
Specification: U, H, T		-40 to +85				$^\circ\text{C}$		
Thermal Resistance, $\theta_{JA}$	Junction-to-Ambient							
U SO-8		125				$^\circ\text{C}/\text{W}$	typ	C
H PSO-8	Exposed Slug Soldered to Board	55				$^\circ\text{C}/\text{W}$	typ	C
T SO-16		100				$^\circ\text{C}/\text{W}$	typ	C

NOTES: (1) Junction temperature = ambient for +25°C specifications.

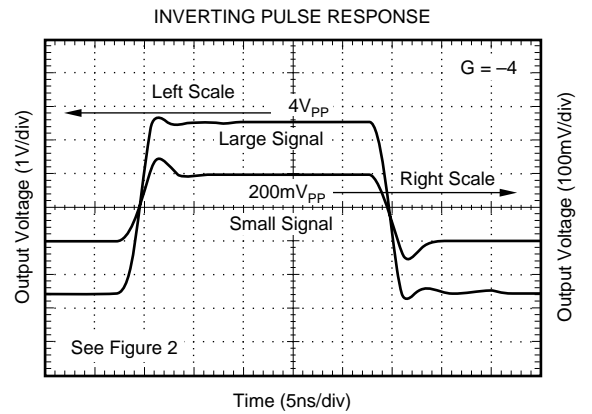
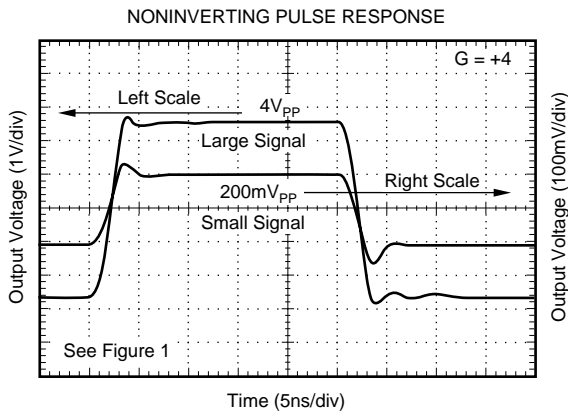
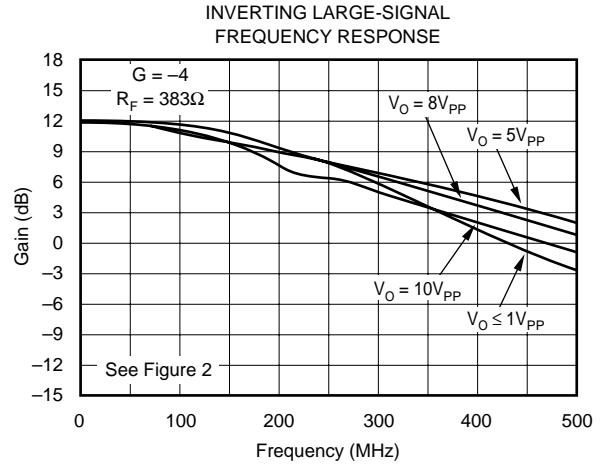
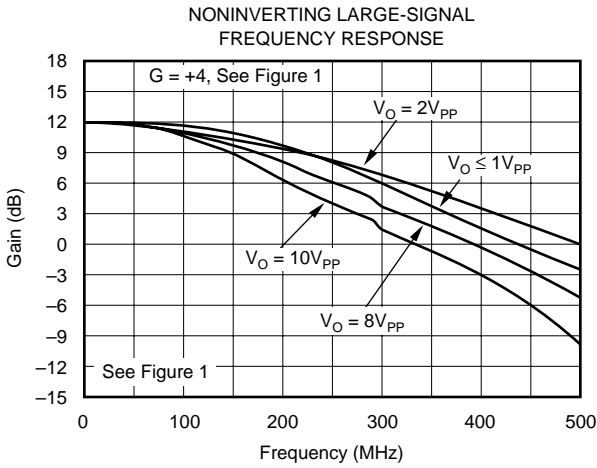
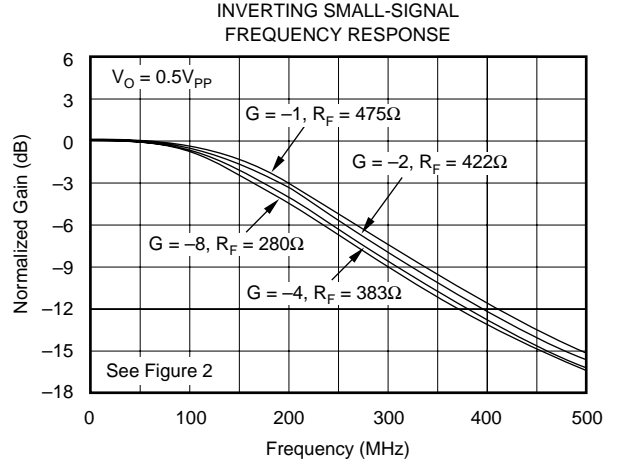
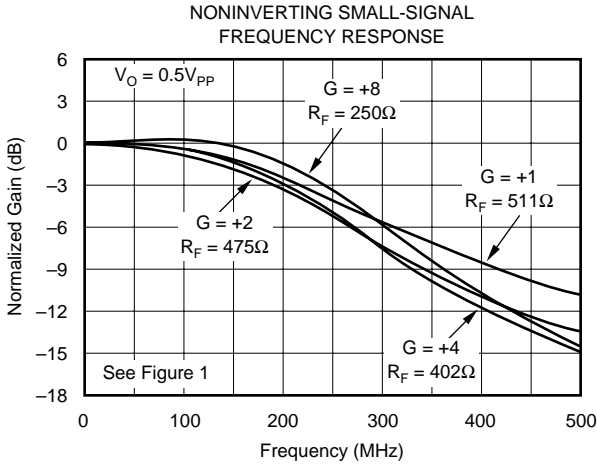
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +9°C at high temperature limit for over temperature specifications.

(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation.

(C) Typical value only for information.

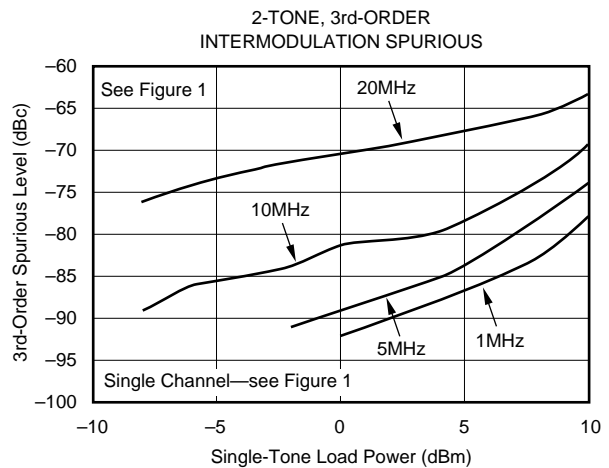
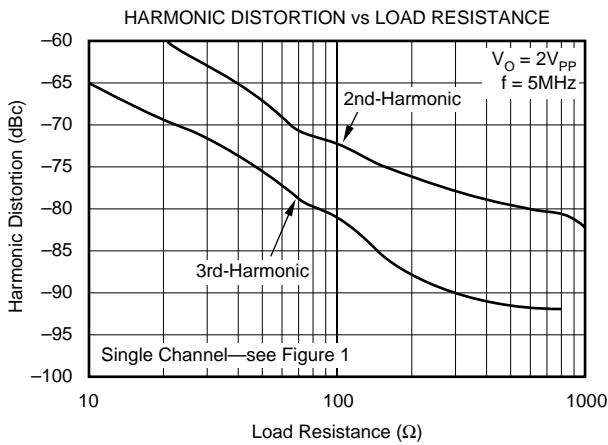
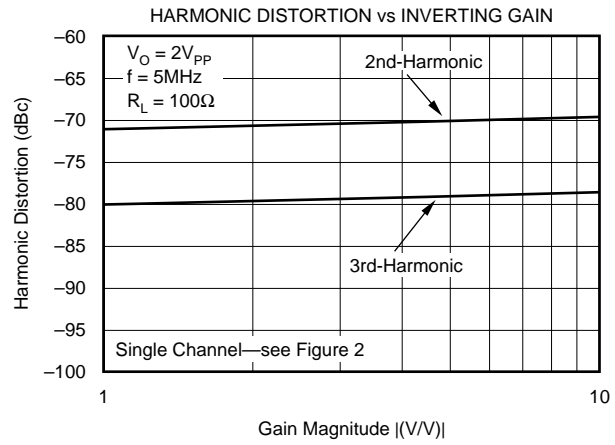
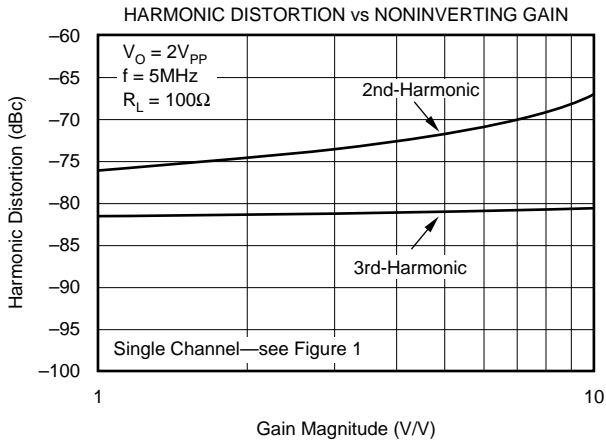
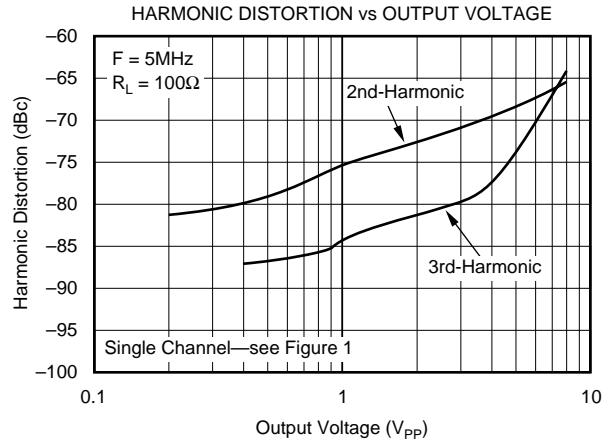
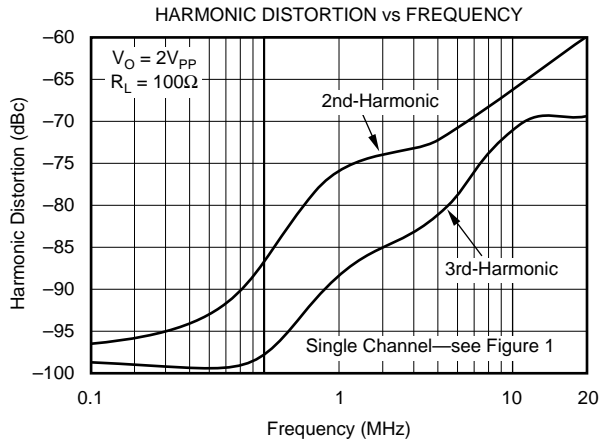
# TYPICAL CHARACTERISTICS: $V_S = \pm 6V$

At  $T_A = +25^\circ C$ ,  $G = +4$ ,  $R_F = 402\Omega$ , and  $R_L = 100\Omega$ , unless otherwise noted.



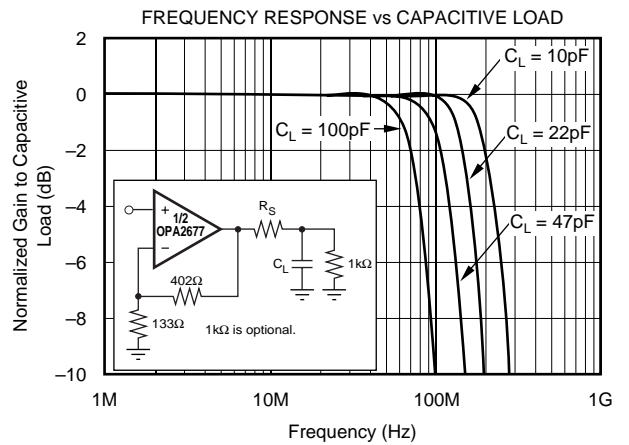
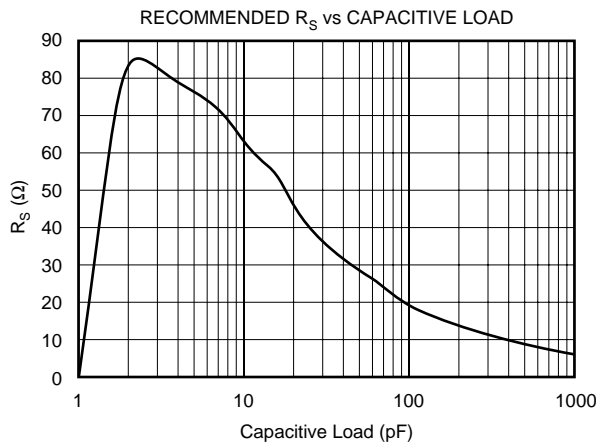
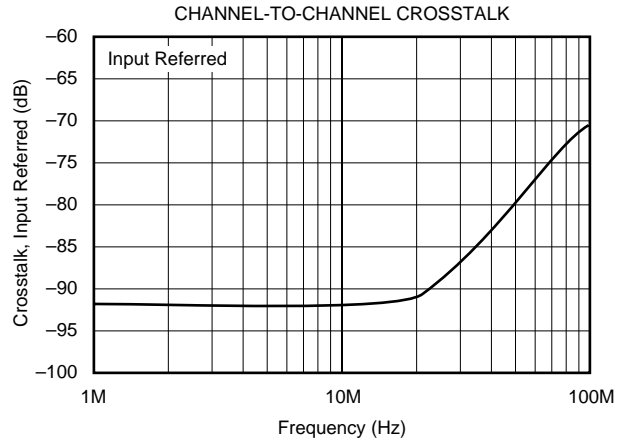
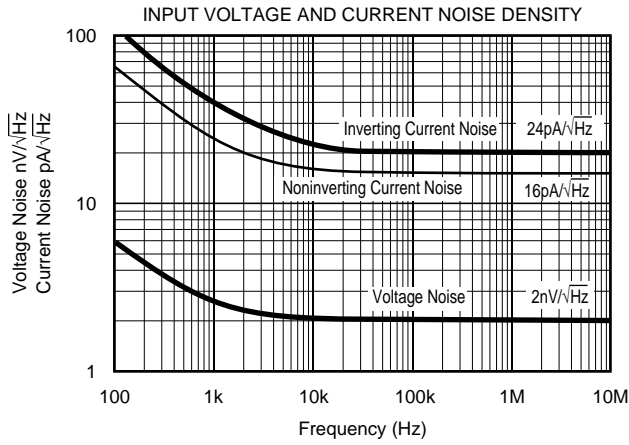
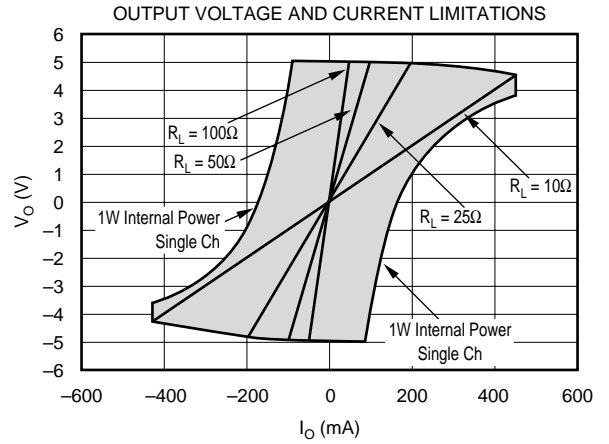
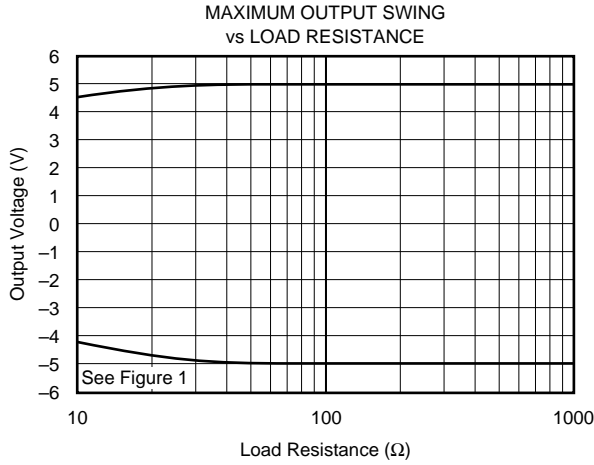
# TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (Cont.)

At  $T_A = +25^\circ C$ ,  $G = +4$ ,  $R_F = 402\Omega$ , and  $R_L = 100\Omega$ , unless otherwise noted.



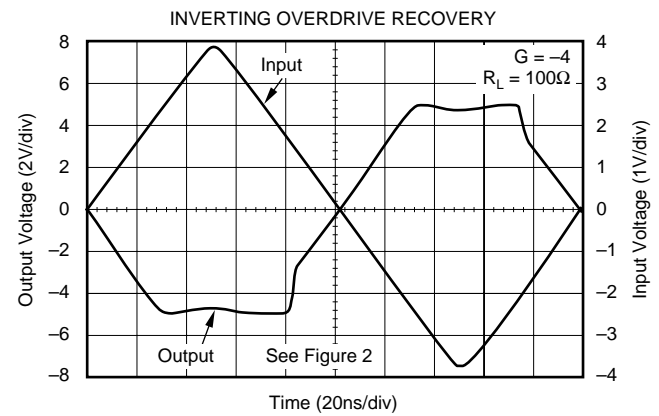
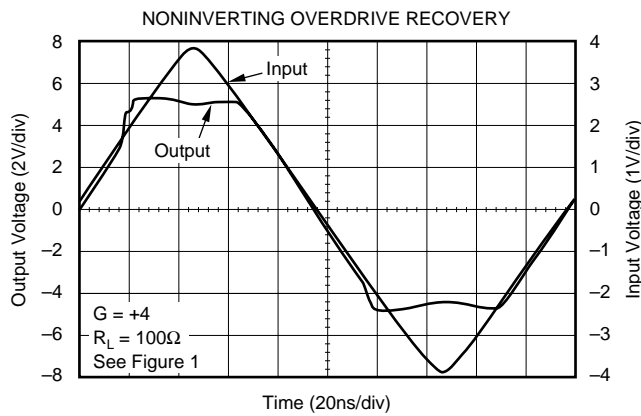
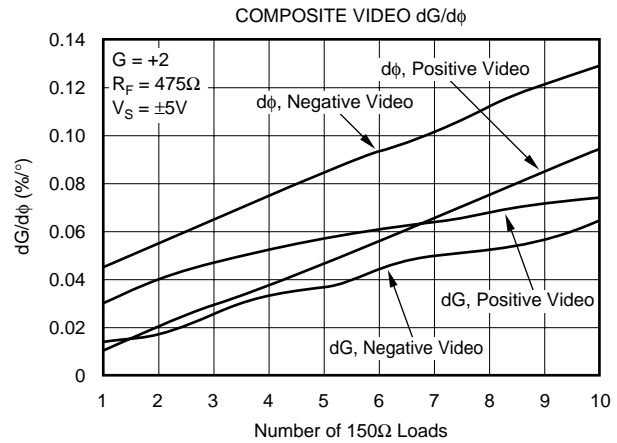
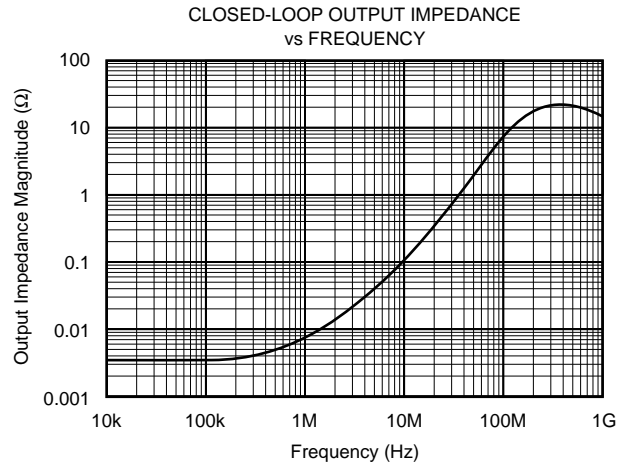
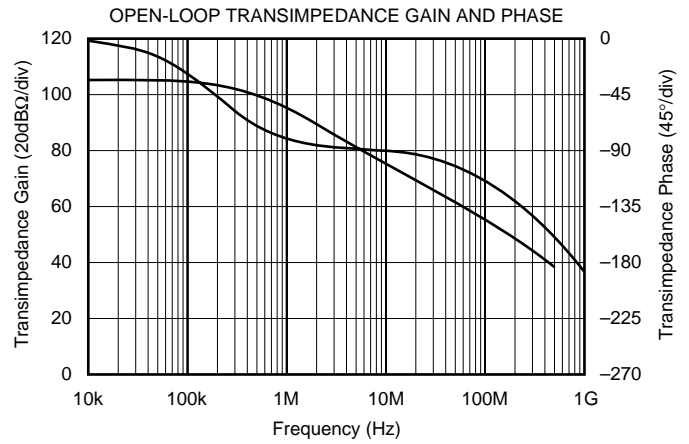
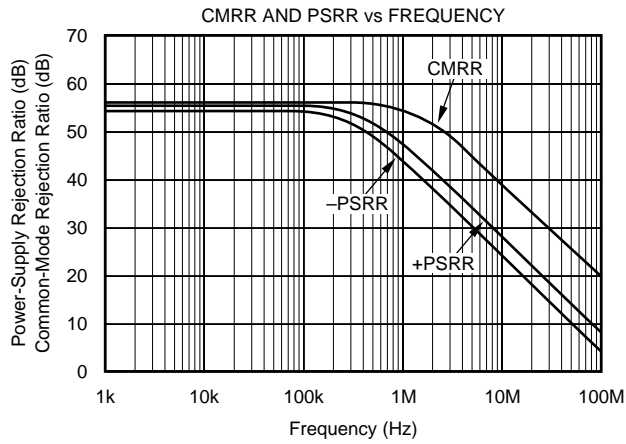
# TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (Cont.)

At  $T_A = +25^\circ C$ ,  $G = +4$ ,  $R_F = 402\Omega$ , and  $R_L = 100\Omega$ , unless otherwise noted.



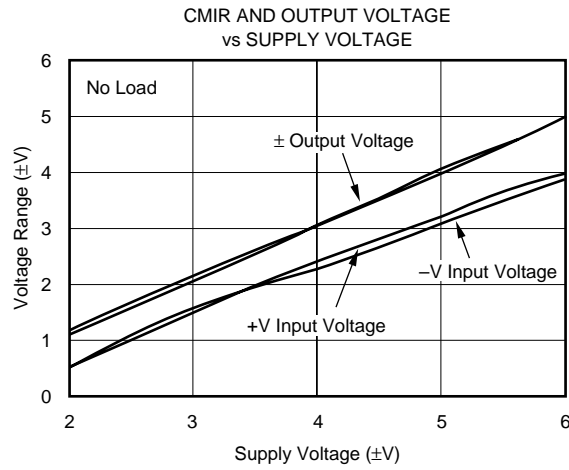
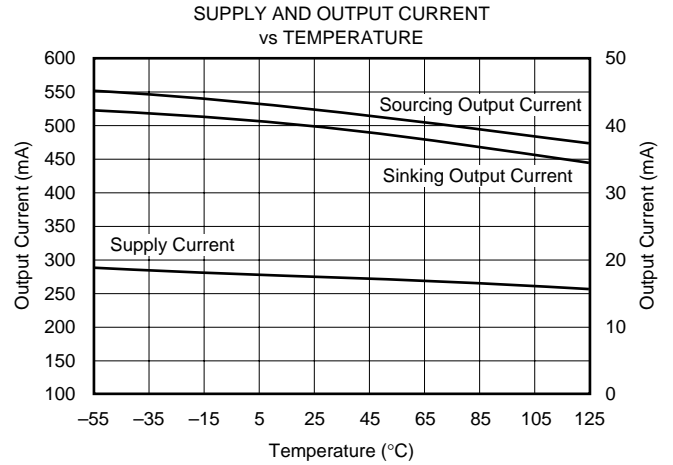
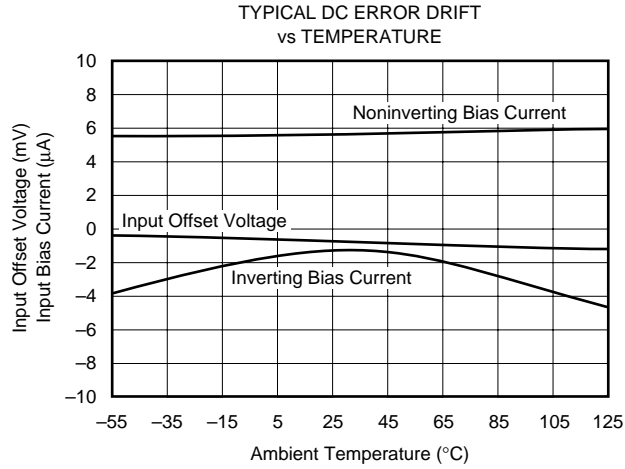
# TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (Cont.)

At  $T_A = +25^\circ C$ ,  $G = +4$ ,  $R_F = 402\Omega$ , and  $R_L = 100\Omega$ , unless otherwise noted.



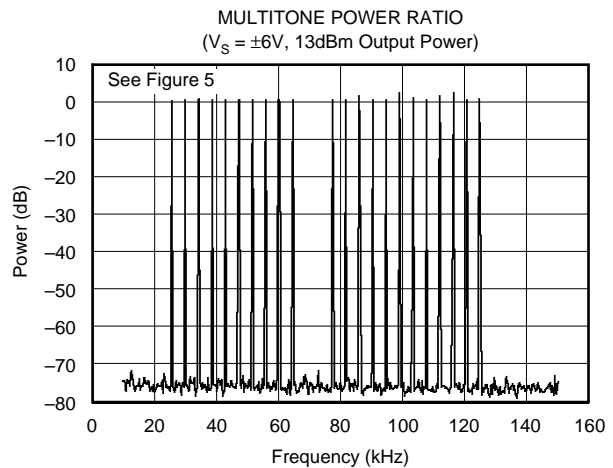
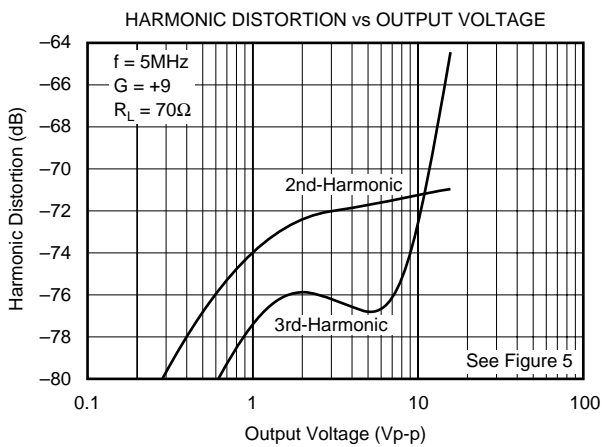
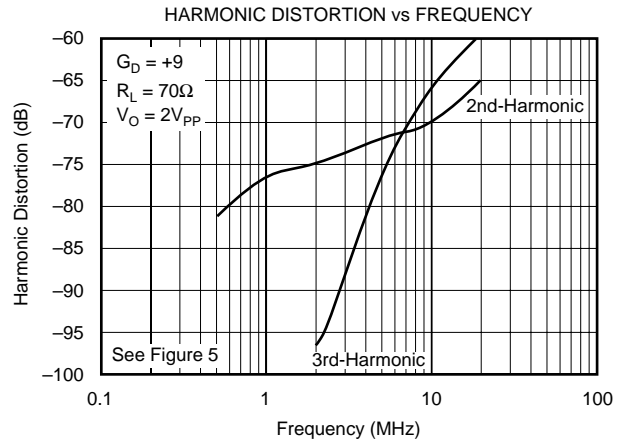
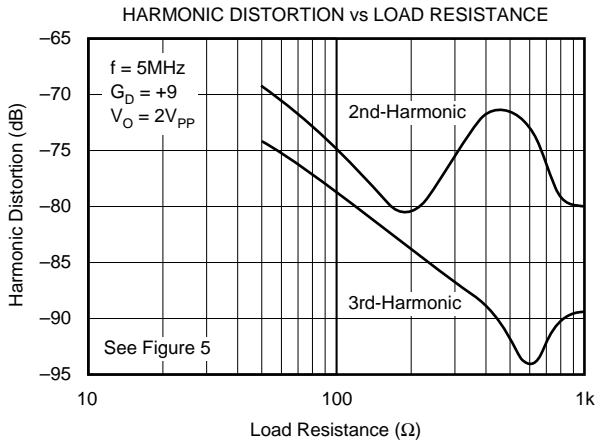
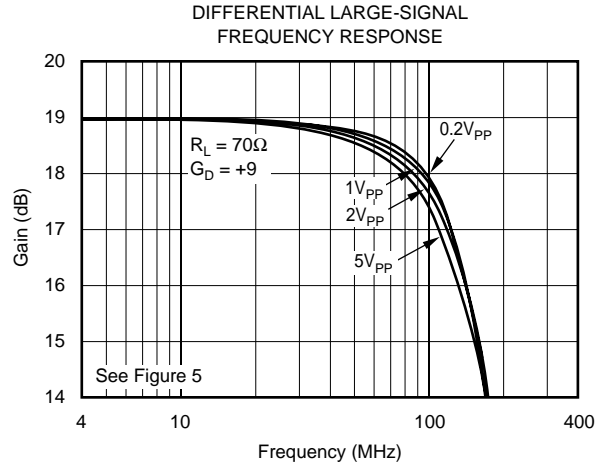
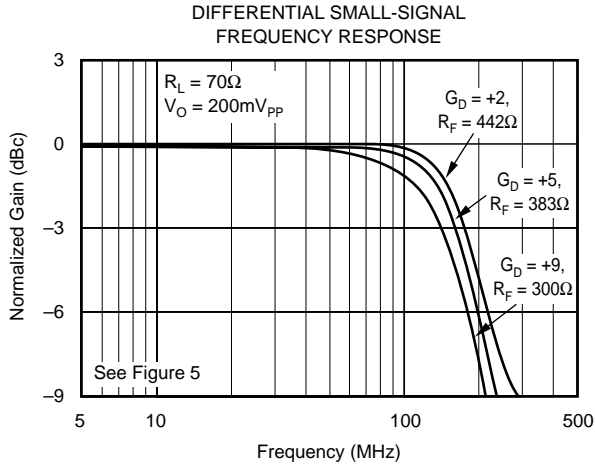
# TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (Cont.)

At  $T_A = +25^\circ C$ ,  $G = +4$ ,  $R_F = 402\Omega$ , and  $R_L = 100\Omega$ , unless otherwise noted.



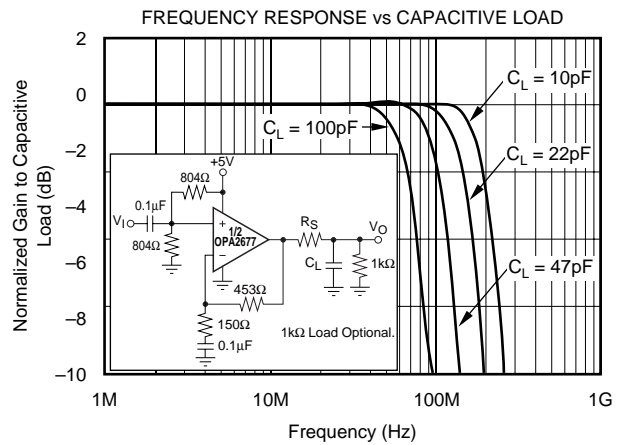
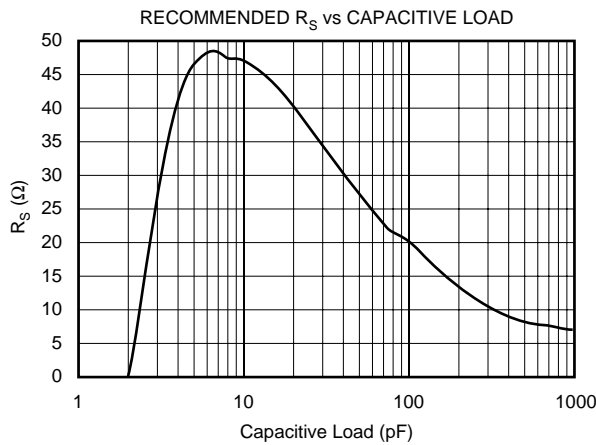
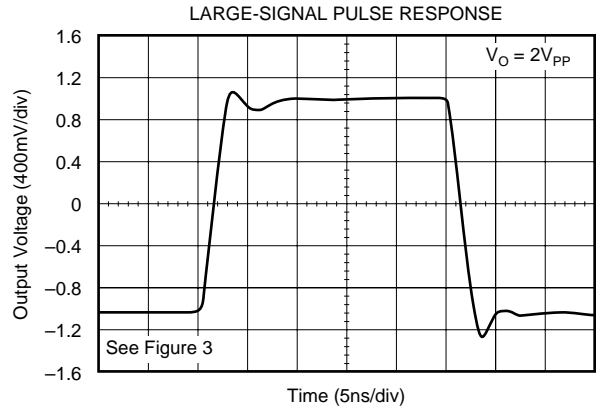
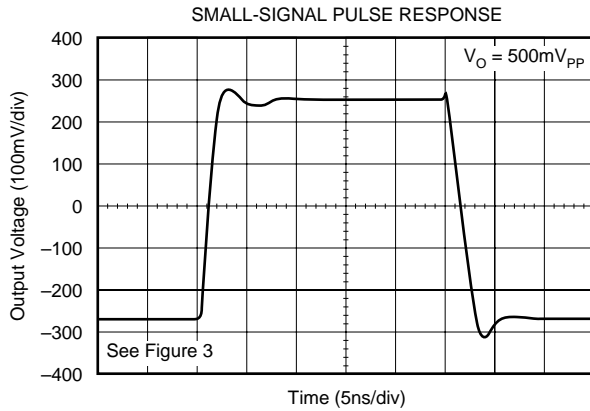
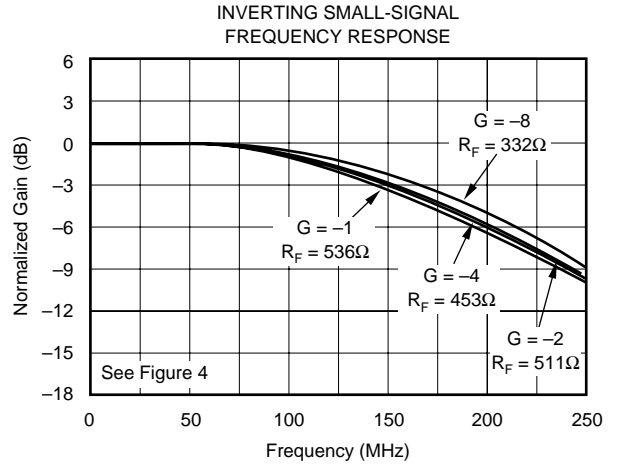
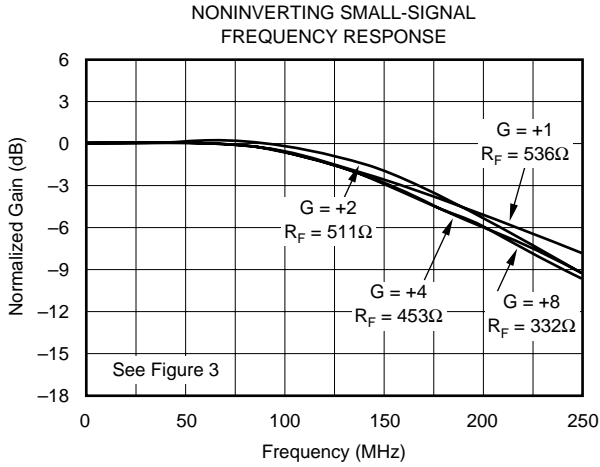
# TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (Cont.)

At  $T_A = +25^\circ C$ , Differential Gain = +9,  $R_F = 300\Omega$ , and  $R_L = 70\Omega$ , unless otherwise noted. See Figure 5 for AC performance only.



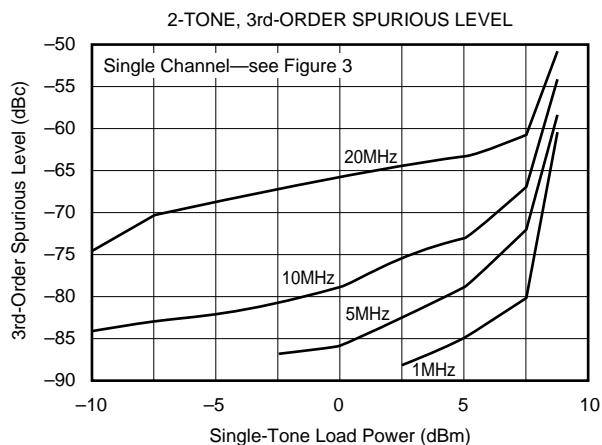
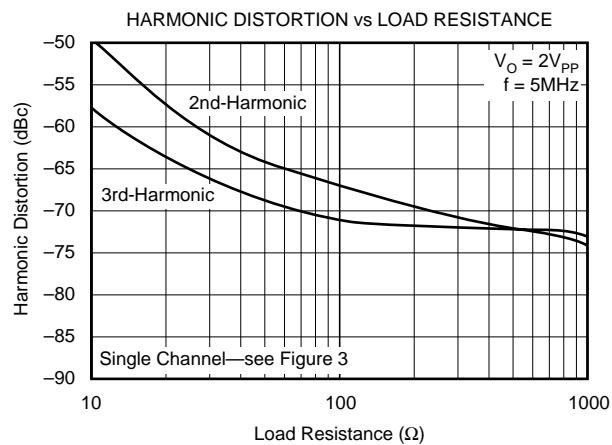
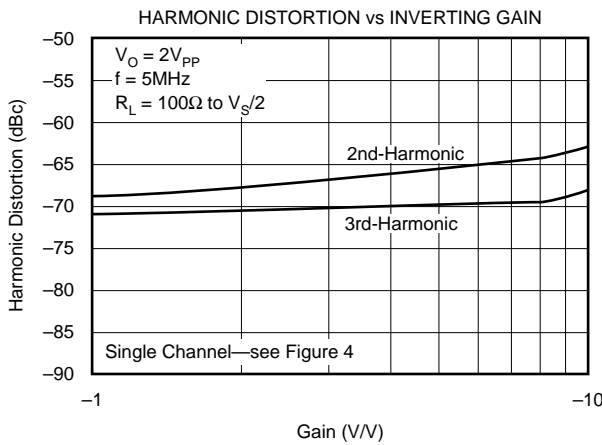
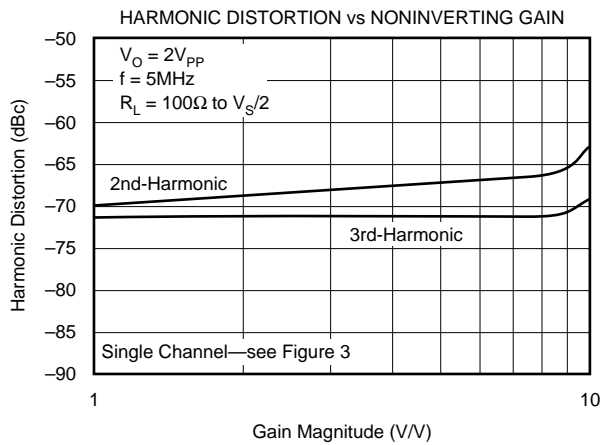
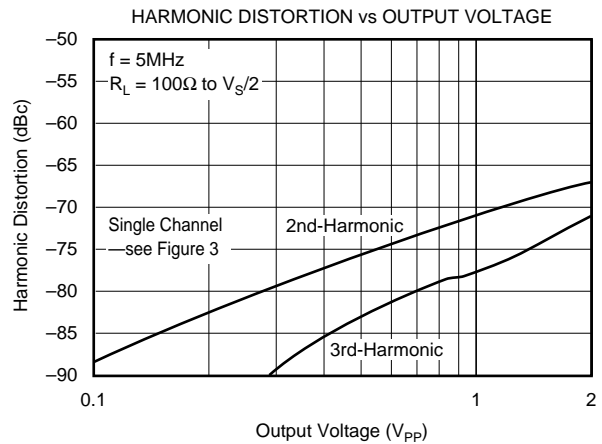
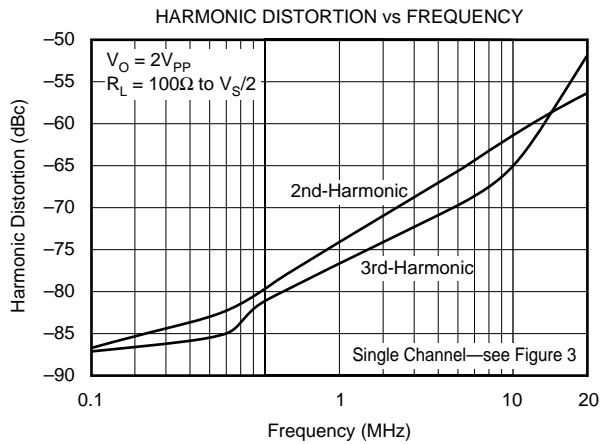
# TYPICAL CHARACTERISTICS: $V_S = +5V$

At  $T_A = +25^\circ C$ ,  $G = +4$ ,  $R_F = 453\Omega$ , and  $R_L = 100\Omega$  to  $V_S/2$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS: $V_S = +5V$ (Cont.)

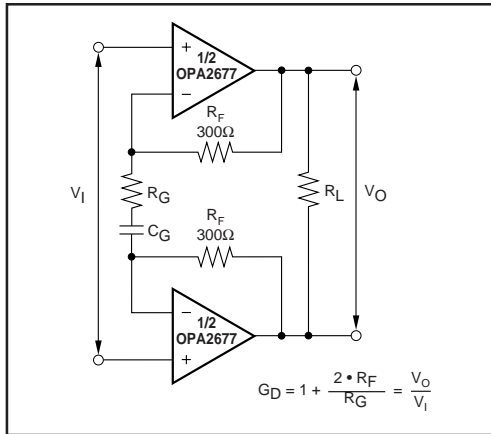
At  $T_A = +25^\circ C$ ,  $G = +4$ ,  $R_F = 453\Omega$ , and  $R_L = 100\Omega$  to  $V_S/2$ , unless otherwise noted.



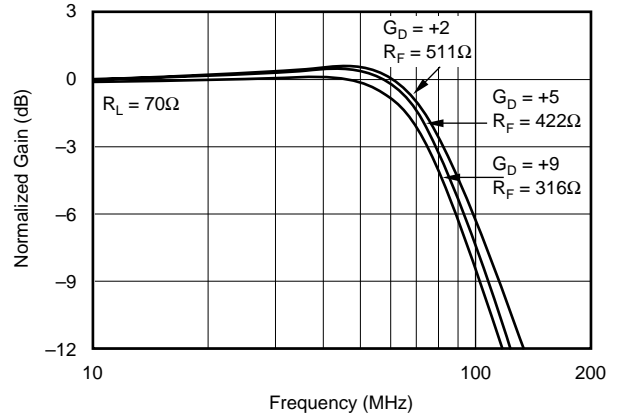
# TYPICAL CHARACTERISTICS: $V_S = +5V$ (Cont.)

At  $T_A = +25^\circ C$ , Differential Gain = +9,  $R_F = 316\Omega$ , and  $R_L = 70\Omega$ , unless otherwise noted.

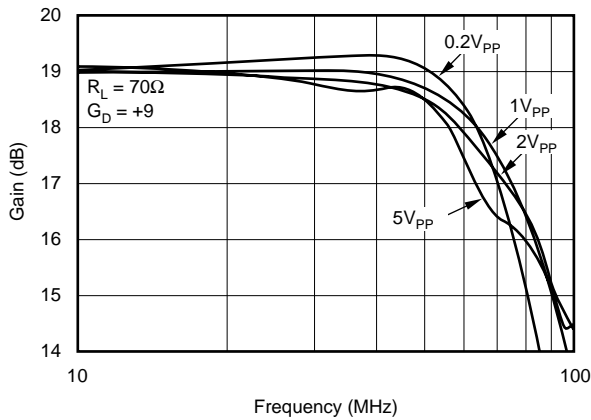
DIFFERENTIAL PERFORMANCE TEST CIRCUIT



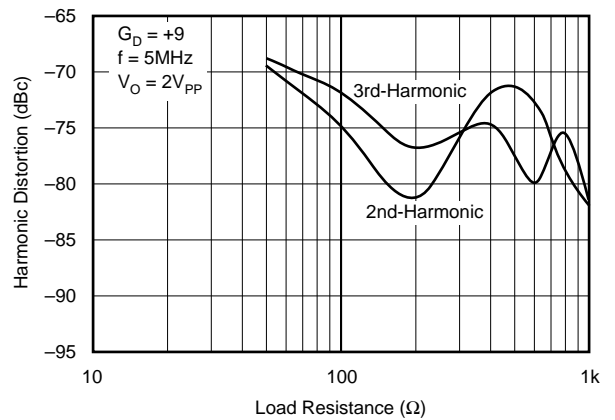
DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE



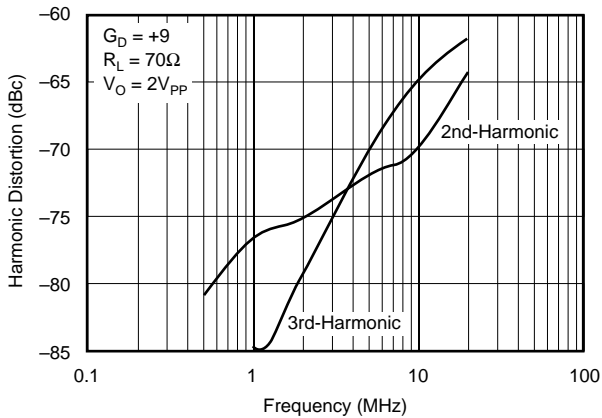
DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE



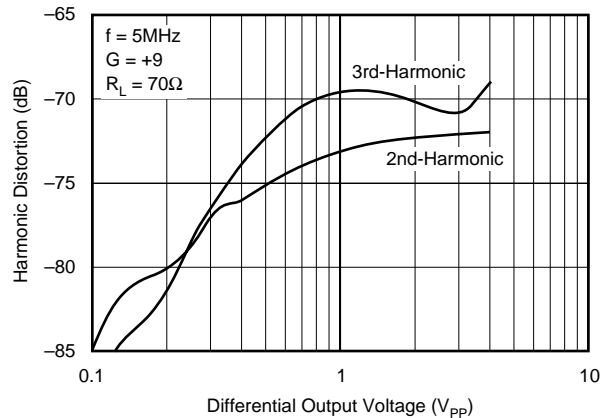
HARMONIC DISTORTION vs LOAD RESISTANCE



HARMONIC DISTORTION vs FREQUENCY



HARMONIC DISTORTION vs OUTPUT VOLTAGE



# APPLICATION INFORMATION

## WIDEBAND CURRENT-FEEDBACK OPERATION

The OPA2677 gives the exceptional AC performance of a wideband current-feedback op amp with a highly linear, high-power output stage. Requiring only 9mA/ch quiescent current, the OPA2677 swings to within 1V of either supply rail and delivers in excess of 380mA at room temperature. This low-output headroom requirement, along with supply voltage independent biasing, gives remarkable single (+5V) supply operation. The OPA2677 delivers greater than 150MHz bandwidth driving a 2V<sub>PP</sub> output into 100Ω on a single +5V supply. Previous boosted output stage amplifiers typically suffer from very poor crossover distortion as the output current goes through zero. The OPA2677 achieves a comparable power gain with much better linearity. The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that AC performance (bandwidth and distortion) is relatively independent of signal gain. Figure 1 shows the DC-coupled, gain of +4, dual power-supply circuit configuration used as the basis of the ±6V Electrical and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the electrical characteristics are taken directly at the input and output pins, whereas load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load is 100Ω || 535Ω = 84Ω.

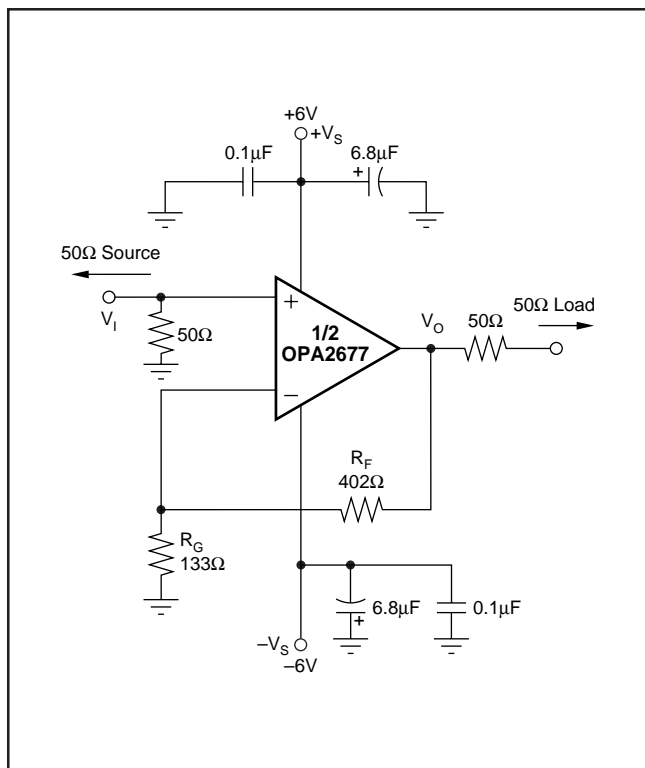


FIGURE 1. DC-Coupled, G = +4, Bipolar Supply, Specification and Test Circuit.

Figure 2 shows the DC-coupled, bipolar supply circuit configuration used as the basis for the Inverting Gain ±6V Typical Characteristics. Key design considerations of the inverting configuration are developed in the *Inverting Amplifier Operation* section.

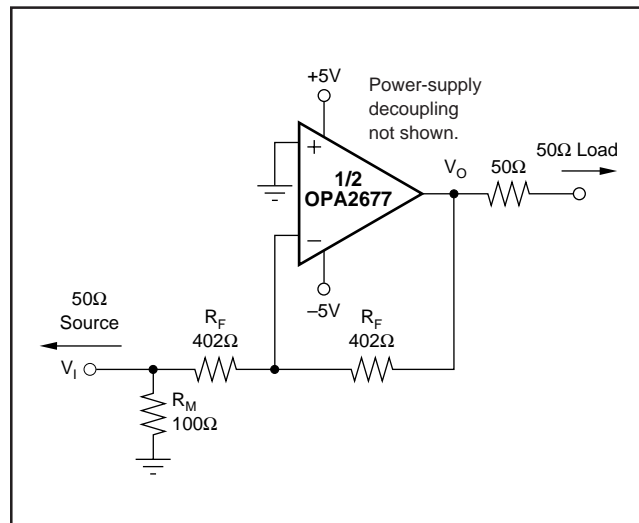


FIGURE 2. DC-Coupled, G = -4, Bipolar Supply, Specification and Test Circuit.

Figure 3 shows the AC-coupled, gain of +4, single-supply circuit configuration used as the basis of the +5V Electrical and Typical Characteristics. Though not a rail-to-rail design, the OPA2677 requires minimal input and output voltage headroom compared to other very wideband current-feedback op amps. It will deliver a 3V<sub>PP</sub> output swing on a single +5V supply with greater than 100MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 3 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 806Ω resistors). The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.3V of either supply pin, giving a 2.4V<sub>PP</sub> input signal range centered between the supply pins. The input impedance matching resistor (57.6Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R<sub>G</sub>) is AC-coupled, giving the circuit a DC gain of +1—which puts the input DC bias voltage (2.5V) on the output as well. The feedback resistor value is adjusted from the bipolar supply condition to re-optimize for a flat frequency response in +5V, gain of +4, operation. Again, on a single +5V supply, the output voltage can swing to within 1V of either supply pin while delivering more than 200mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage used in the OPA2677 can deliver large bipolar output currents into this midpoint load with minimal crossover distortion, as shown by the +5V supply, harmonic distortion plots.

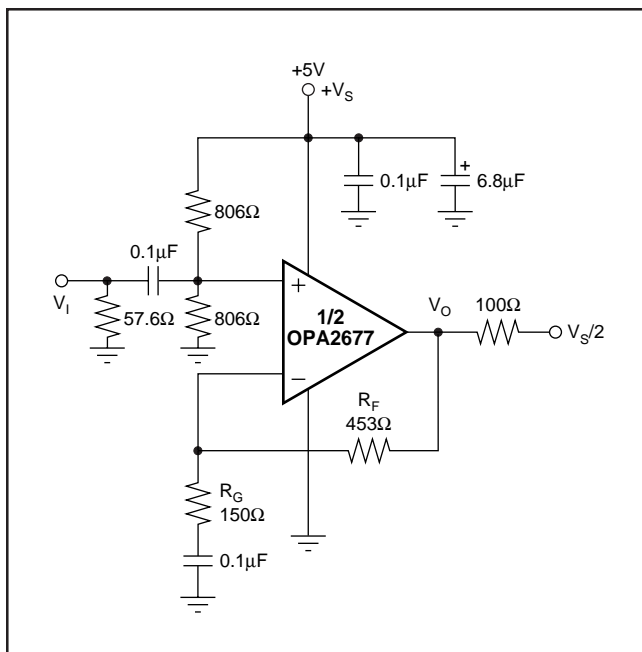


FIGURE 3. AC-Coupled,  $G = +4$ , Single-Supply, Specification and Test Circuit.

The last configuration used as the basis of the +5V Electrical and Typical Characteristics is shown in Figure 4. Design considerations for this inverting, bipolar supply configuration are covered either in single-supply configuration (as shown in Figure 3) or in the *Inverting Amplifier Operation* section.

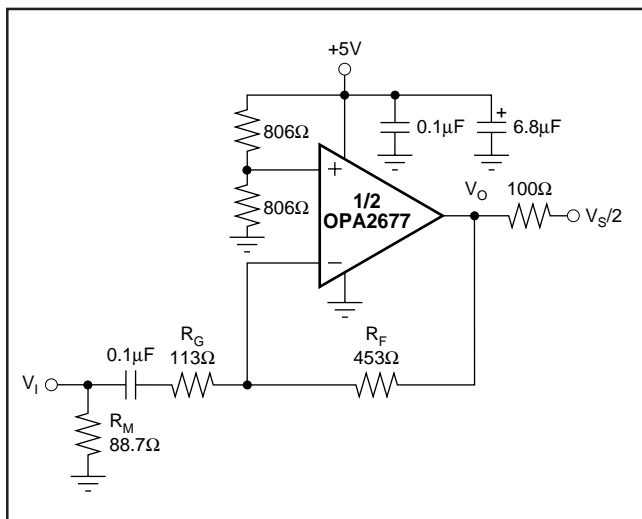


FIGURE 4. AC-Coupled,  $G = -4$ , Single-Supply, Specification and Test Circuit.

## DIFFERENTIAL INTERFACE APPLICATIONS

Dual op amps are particularly suitable to differential input to differential output applications. Typically, these fall into either Analog-to-Digital Converter (ADC) input interface or line driver applications. Two basic approaches to differential I/O are noninverting or inverting configurations. Since the output is differential, the signal polarity is somewhat meaningless—the noninverting and inverting terminology applies here to

where the input is brought into the OPA2677. Each has its advantages and disadvantages. Figure 5 shows a basic starting point for noninverting differential I/O applications.

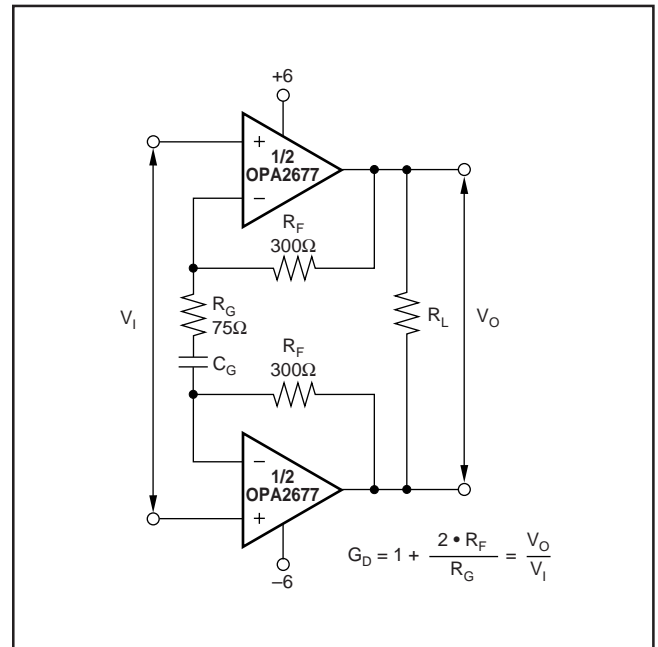


FIGURE 5. Noninverting Differential I/O Amplifier.

This approach provides for a source termination impedance that is independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the noninverting inputs without interacting with the gain setting. The differential signal gain for the circuit of Figure 5 is:

$$A_D = 1 + 2 \cdot R_F/R_G$$

Since the OPA2677 is a current feedback (CFB) amplifier, its bandwidth is principally controlled with the feedback resistor value; Figure 5 shows a value of 300Ω for the  $A_D = +9$  design. The differential gain, however, may be adjusted with considerable freedom using just the  $R_G$  resistor. In fact,  $R_G$  may be a reactive network providing a very isolated shaping to the differential frequency response.

Various combinations of single-supply or AC-coupled gain can also be delivered using the basic circuit of Figure 5. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1 since an equal DC voltage at each inverting node creates no current through  $R_G$ . This circuit does show a common-mode gain of 1 from input to output. The source connection should either remove this common-mode signal if undesired (using an input transformer can provide this function), or the common-mode voltage at the inputs can be used to set the output common-mode bias. If the low common-mode rejection of this circuit is a problem, the output interface may also be used to reject that common-mode. For instance, most modern differential input ADCs reject common-mode signals very well, while a line driver application through a transformer will also attenuate the common-mode signal through to the line.

## SINGLE-SUPPLY ADSL UPSTREAM DRIVER

Figure 6 shows an example of a single-supply ADSL upstream driver. The dual OPA2677 is configured as a differential gain stage to provide signal drive to the primary winding of the transformer (here, a step-up transformer with a turns ratio of 1:1.7). The main advantage of this configuration is the cancellation of all even harmonic distortion products. Another important advantage for ADSL is that each amplifier needs only to swing half of the total output required driving the load.

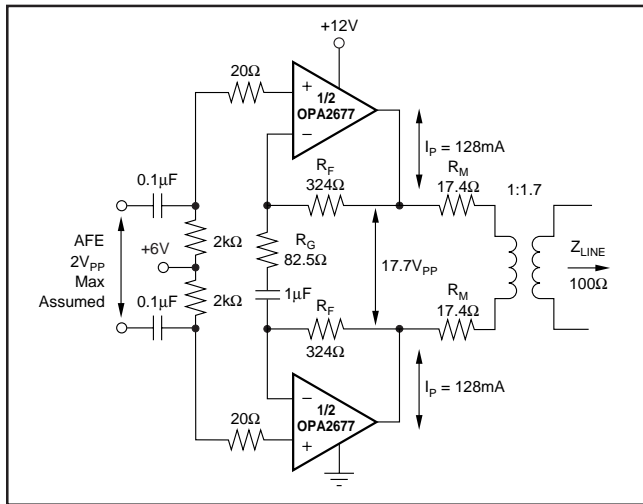


FIGURE 6. Single-Supply ADSL Upstream Driver.

The analog front end (AFE) signal is AC-coupled to the driver, and the noninverting input of each amplifier is biased to the mid-supply voltage (+6V in this case). In addition to providing the proper biasing to the amplifier, this approach also provides a high-pass filtering with a corner frequency, set here at 5kHz. As the upstream signal bandwidth starts at 26kHz, this high-pass filter does not generate any problem and has the advantage of filtering out unwanted lower frequencies.

The input signal is amplified with a gain set by the following equation:

$$G_D = 1 + \frac{2 \cdot R_F}{R_G} \quad (1)$$

With  $R_F = 324\Omega$  and  $R_G = 82.5\Omega$ , the gain for this differential amplifier is 8.85. This gain boosts the AFE signal, assumed to be a maximum of  $2V_{PP}$ , to a maximum of  $17.3V_{PP}$ .

Refer to the *Setting Resistor Values to Optimize Bandwidth* section for a discussion on which feedback resistor value to choose.

The two back-termination resistors ( $17.4\Omega$  each) added at each terminal of the transformer make the impedance of the modem match the impedance of the phone line, and also provide a means of detecting the received signal for the receiver. The value of these resistors ( $R_M$ ) is a function of the line impedance and the transformer turns ratio ( $n$ ), given by the following equation:

$$R_M = \frac{Z_{LINE}}{2n^2} \quad (2)$$

## OPA2677 HDSL2 UPSTREAM DRIVER

Figure 7 shows an HDSL2 implementation of a single-supply upstream driver.

The two designs differ by the values of their matching impedance, the load impedance, and the ratio turns of the transformers. All these differences are reflected in the higher peak current and thus, the higher maximum power dissipation in the output of the driver.

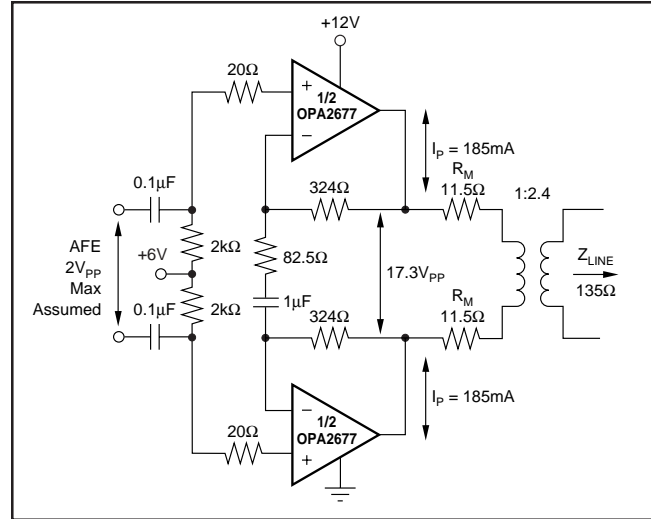


FIGURE 7. HDSL2 Upstream Driver.

## LINE DRIVER HEADROOM MODEL

The first step in a transformer-coupled, twisted-pair driver design is to compute the peak-to-peak output voltage from the target specifications. This is done using the following equations:

$$P_L = 10 \cdot \log \frac{V_{RMS}^2}{(1mW) \cdot R_L} \quad (3)$$

with  $P_L$  power at the load,  $V_{RMS}$  voltage at the load, and  $R_L$  load impedance; this gives the following:

$$V_{RMS} = \sqrt{(1mW) \cdot R_L \cdot 10^{\frac{P_L}{10}}} \quad (4)$$

$$V_P = \text{Crest Factor} \cdot V_{RMS} = C_F \cdot V_{RMS} \quad (5)$$

with  $V_P$  peak voltage at the load and  $C_F$  Crest Factor.

$$V_{LPP} = 2 \cdot C_F \cdot V_{RMS} \quad (6)$$

with  $V_{LPP}$ : peak-to-peak voltage at the load.

Consolidating Equations 3 through 6 allows expressing the required peak-to-peak voltage at the load as a function of the crest factor, the load impedance, and the power at the load.

Thus, 
$$V_{LPP} = 2 \cdot C_F \cdot \sqrt{(1mW) \cdot R_L \cdot 10^{\frac{P_L}{10}}} \quad (7)$$

This  $V_{LPP}$  is usually computed for a nominal line impedance and may be taken as a fixed design target.

The next step in the design is to compute the individual amplifier output voltage and currents as a function of  $V_{PP}$  on

the line and transformer turns ratio. As this turns ratio changes, the minimum allowed supply voltage changes along with it. The peak current in the amplifier output is given by:

$$\pm I_P = \frac{1}{2} \cdot \frac{2 \cdot V_{LPP}}{n} \cdot \frac{1}{4R_M} \quad (8)$$

with  $V_{PP}$  as defined in Equation 7, and  $R_M$  as defined in Equation 2 and shown in Figure 8.

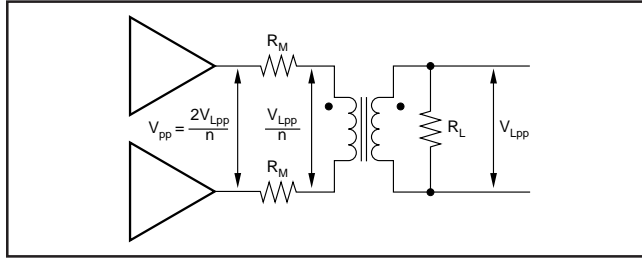


FIGURE 8. Driver Peak Output Voltage.

With the previous information available, it is now possible to select a supply voltage and the turns ratio desired for the transformer as well as calculate the headroom for the OPA2677.

The model, shown in Figure 9, can be described with the following set of equations:

- 1) As available output swing:

$$V_{PP} = V_{CC} - (V_1 + V_2) - I_P \cdot (R_1 + R_2) \quad (9)$$

- 2) Or as required supply voltage:

$$V_{CC} = V_{PP} + (V_1 + V_2) + I_P \cdot (R_1 + R_2) \quad (10)$$

The minimum supply voltage for a power and load requirement is given by Equation 10.

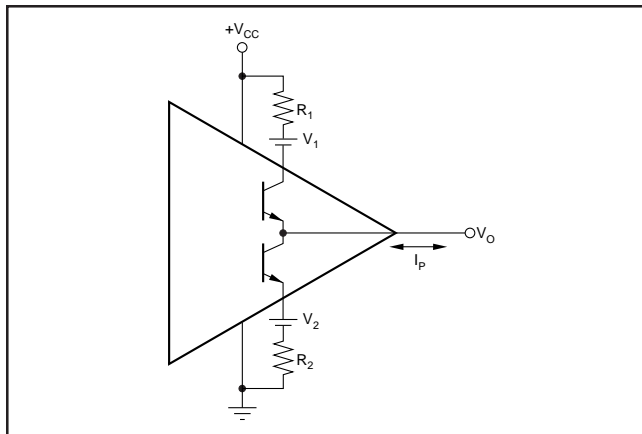


FIGURE 9. Line Driver Headroom Model.

$V_1$ ,  $V_2$ ,  $R_1$ , and  $R_2$  are given in Table I for both +12V and +5V operation.

	$V_1$	$R_1$	$V_2$	$R_2$
+5V	0.9V	5Ω	0.8V	5Ω
+12V	0.9V	2Ω	0.9V	2Ω

TABLE I. Line Driver Headroom Model Values.

## TOTAL DRIVER POWER FOR xDSL APPLICATIONS

The total internal power dissipation for the OPA2677 in an xDSL line driver application will be the sum of the quiescent power and the output stage power. The OPA2677 holds a relatively constant quiescent current versus supply voltage—giving a power contribution that is simply the quiescent current times the supply voltage used (the supply voltage will be greater than the solution given in Equation 10). The total output stage power may be computed with reference to Figure 10.

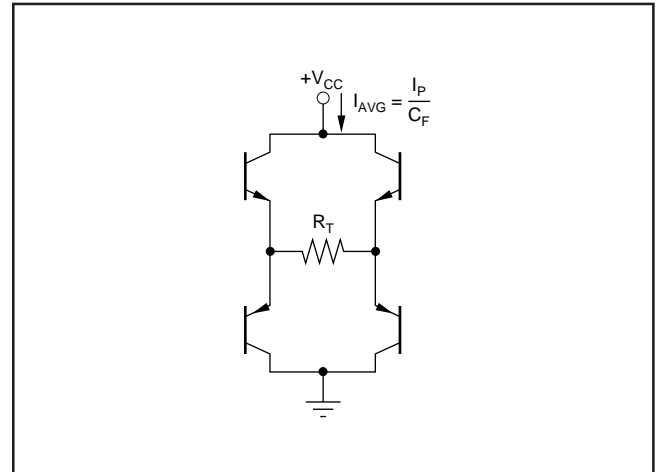


FIGURE 10. Output Stage Power Model.

The two output stages used to drive the load of Figure 8 can be seen as an H-Bridge in Figure 10. The average current drawn from the supply into this H-Bridge and load will be the peak current in the load given by Equation 8 divided by the crest factor (CF) for the xDSL modulation. This total power from the supply is then reduced by the power in  $R_T$  to leave the power dissipated internal to the drivers in the four output stage transistors. That power is simply the target line power used in Equation 3 plus the power lost in the matching elements ( $R_M$ ). In the examples here, a perfect match is targeted giving the same power in the matching elements as in the load. The output stage power is then set by Equation 11.

$$P_{OUT} = \frac{I_P}{C_F} \times V_{CC} - 2P_L \quad (11)$$

The total amplifier power is then:

$$P_{TOT} = I_q \times V_{CC} + \frac{I_P}{C_F} \times V_{CC} - 2P_L \quad (12)$$

For the ADSL CPE upstream driver design of Figure 6, the peak current is 128mA for a signal that requires a crest factor of 5.33 with a target line power of 13dBm into 100Ω (20mW). With a typical quiescent current of 18mA and a nominal supply voltage of +12V, the total internal power dissipation for the solution of Figure 6 will be:

$$P_{TOT} = 18\text{mA}(12\text{V}) + \frac{128\text{mA}}{5.33}(12\text{V}) - 2(20\text{mW}) = 464\text{mW} \quad (13)$$

## OPA2677T, HIGH OUTPUT LINE DRIVER

The OPA2677T, a 16-pin version of the OPA2677, is now available. The specifications for this product are identical to the OPA2677U, while the pinout has been defined to allow a direct replacement of the LT1207CS in +12V single supply xDSL modem designs. Though this product does not have several of the optional features pinned out in the LT1207CS, those features are generally not used in the target applications. Specifically, the LT1207CS provides for separate power enable lines that must be asserted low for the amplifiers to operate—those pins are no-connect pins on the OPA2677T. Also, the two channels of the LT1207CS provide for external compensation capacitors that are not used as compensation pins on the OPA2677T. Finally, the LT1207CS requires numerous power-supply connection pins, whereas the OPA2677T has reduced these to only 2 pins, while also using one of the LT1207 compensation pins as an internal jumper pin for the positive power supply. For a pinout and specification comparison, see Figure 11.

## DESIGN-IN TOOLS

### DEMONSTRATION BOARDS

Several PC boards are available to assist in the initial evaluation of circuit performance using the OPA2677 in the four package styles. These are available, free, as unpopulated PC boards delivered with descriptive documentation. The summary information for these units is shown in Table II.

Check the TI web site ([www.ti.com](http://www.ti.com)) to request any of these boards.

PRODUCT	PACKAGE	DEMO BOARD NUMBER	ORDERING NUMBER
OPA2677U	SO-8	DEM-OPA268xU	SBOU003
OPA2677H	PSO-8	DEM-OPA268xU	SBOU022
OPA2677T	SO-16	Not Available	Not Available

TABLE II. Demonstration Board Ordering Information.

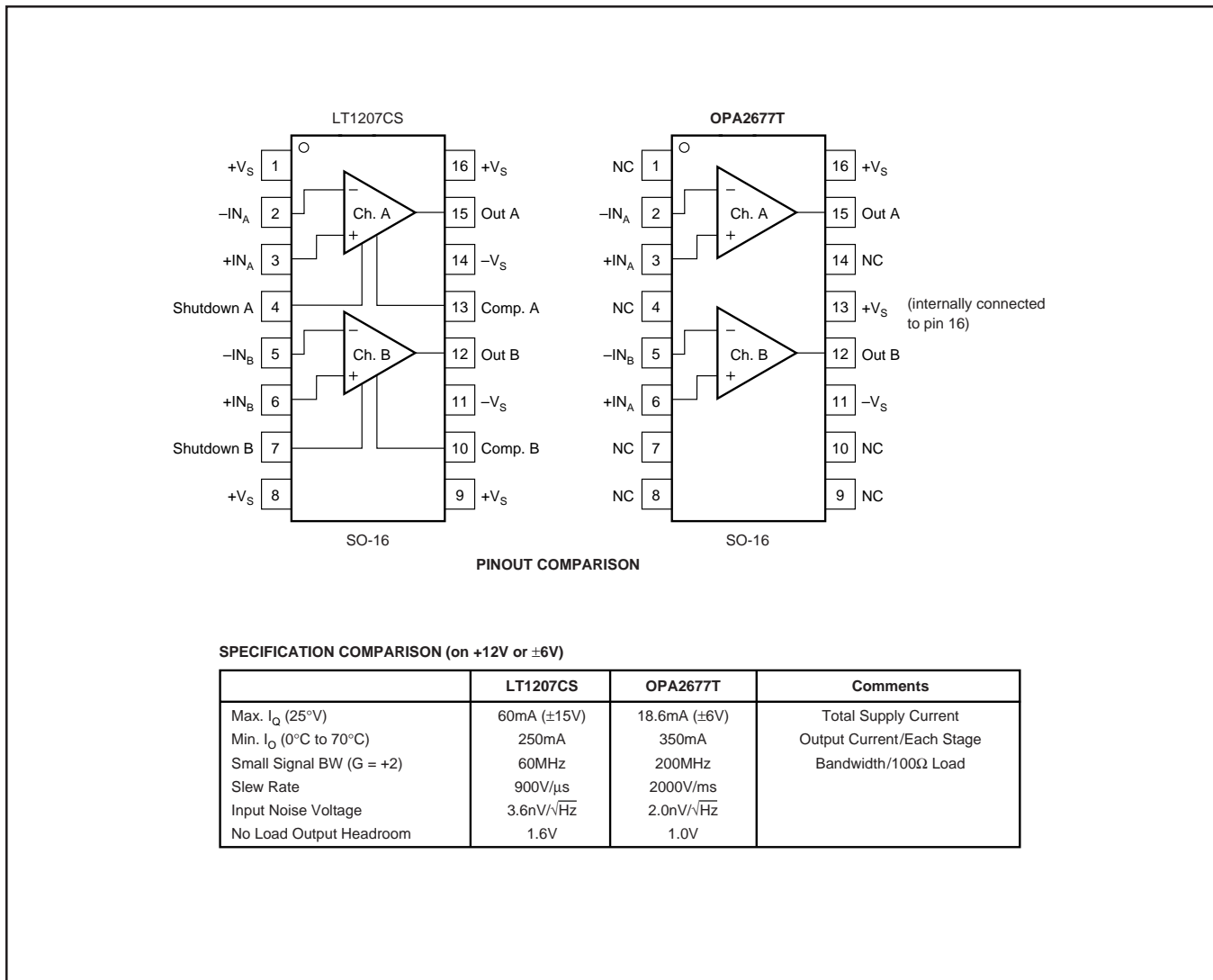


FIGURE 11. Pinout and Specification Comparison of the LT1207CS and OPA2677T.

## MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA2677 is available through the TI web site ([www.ti.com](http://www.ti.com)). This model does a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions, but does not do as well in predicting the harmonic distortion or dG/dP characteristics. This model does not attempt to distinguish between the package types in small-signal AC performance, nor does it attempt to simulate channel-to-channel coupling.

## OPERATING SUGGESTIONS

### SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

A current-feedback op amp like the OPA2677 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values, which is shown in the Typical Characteristics; the small-signal bandwidth decreases only slightly with increasing gain. These curves also show that the feedback resistor is changed for each gain setting. The resistor values on the inverting side of the circuit for a current-feedback op amp can be treated as frequency response compensation elements, whereas their ratios set the signal gain. Figure 12 shows the small-signal frequency response analysis circuit for the OPA2677.

The key elements of this current-feedback op amp model are:

- $\alpha$  → Buffer gain from the noninverting input to the inverting input
- $R_1$  → Buffer output impedance
- $i_{ERR}$  → Feedback error current signal
- $Z(s)$  → Frequency dependent open-loop transimpedance gain from  $i_{ERR}$  to  $V_O$

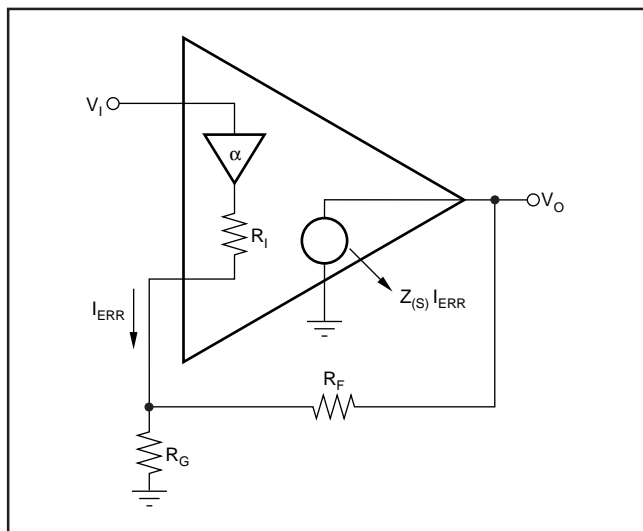


FIGURE 12. Current Feedback Transfer Function Analysis Circuit.

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It sets the CMRR, however, for a single op amp differential amplifier configuration. For a buffer gain  $\alpha < 1.0$ , the CMRR =  $-20 \cdot \log(1 - \alpha)$ dB.

$R_1$ , the buffer output impedance, is a critical portion of the bandwidth control equation. The OPA2677 inverting input resistor is typically 22Ω.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency dependent transimpedance gain. The Typical Characteristics show this open-loop transimpedance response, which is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Developing the transfer function for the circuit of Figure 12 gives Equation 14:

$$\frac{V_O}{V_I} = \frac{\alpha \left( 1 + \frac{R_F}{R_G} \right)}{1 + \frac{R_F + R_1 \left( 1 + \frac{R_F}{R_G} \right)}{Z(s)}} = \frac{\alpha \cdot NG}{1 + \frac{R_F + R_1 NG}{Z(s)}} \quad (14)$$

$$\left[ NG = \left( 1 + \frac{R_F}{R_G} \right) \right]$$

This is written in a loop-gain analysis format where the errors arising from a non-infinite open-loop gain are shown in the denominator. If  $Z(s)$  is infinite over all frequencies, the denominator of Equation 14 reduces to 1 and the ideal desired signal gain shown in the numerator is achieved. The fraction in the denominator of Equation 14 determines the frequency response. Equation 15 shows this as the loop-gain equation:

$$\frac{Z(s)}{R_F + R_1 NG} = \text{Loop Gain} \quad (15)$$

If  $20\log(R_F + NG \cdot R_1)$  is drawn on top of the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually,  $Z(s)$  rolls off to equal the denominator of Equation 15, at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier closed-loop frequency response given by Equation 14 starts to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation 15 may be controlled somewhat separately from the desired signal gain (or NG). The OPA2677 is internally compensated to give a maximally flat frequency response for  $R_F = 402\Omega$  at  $NG = 4$  on  $\pm 6V$  supplies. Evaluating the denominator of Equation 15 (which is the feedback transimpedance) gives an optimal target of 490Ω. As the signal gain changes, the contribution of the  $NG \cdot R_1$  term in the feedback transimpedance changes, but the total can be held constant by adjusting  $R_F$ . Equation 16 gives an approximate equation for optimum  $R_F$  over signal gain:

$$R_F = 490 - NG \cdot R_1 \quad (16)$$

As the desired signal gain increases, this equation eventually predicts a negative  $R_F$ . A somewhat subjective limit to this adjustment can also be set by holding  $R_G$  to a minimum value of  $20\Omega$ . Lower values load both the buffer stage at the input and the output stage if  $R_F$  gets too low—actually decreasing the bandwidth. Figure 13 shows the recommended  $R_F$  versus NG for both  $\pm 6V$  and a single  $+5V$  operation. The values for  $R_F$  versus gain shown here are approximately equal to the values used to generate the Typical Characteristics. They differ in that the optimized values used in the Typical Characteristics are also correcting for board parasitic not considered in the simplified analysis leading to Equation 16. The values shown in Figure 13 give a good starting point for designs where bandwidth optimization is desired.

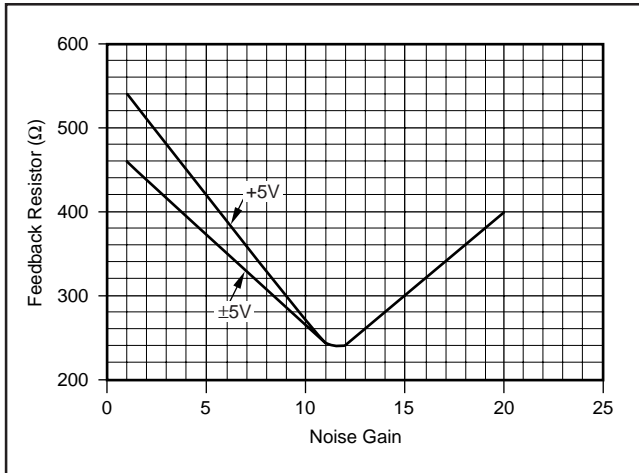


FIGURE 13. Feedback Resistor vs. Noise Gain.

The total impedance going into the inverting input may be used to adjust the closed-loop signal bandwidth. Inserting a series resistor between the inverting input and the summing junction increases the feedback impedance (denominator of Equation 15), decreasing the bandwidth. The internal buffer output impedance for the OPA2677 is slightly influenced by the source impedance looking out of the noninverting input terminal. High-source resistors have the effect of increasing  $R_i$ , decreasing the bandwidth. For those single-supply applications which develop a midpoint bias at the noninverting input through high-valued resistors, the decoupling capacitor is essential for power-supply ripple rejection, noninverting input noise current shunting, and to minimize the high-frequency value for  $R_i$  in Figure 12.

## INVERTING AMPLIFIER OPERATION

The OPA2677 is a general-purpose, wideband current-feedback op amp; most of the familiar op amp application circuits should be available to the designer. Those dual op amp applications that require considerable flexibility in the feedback element (for example, integrators, transimpedance, and some filters) should consider a unity-gain stable, voltage-feedback amplifier such as the OPA2822, because the feedback resistor is the compensation element for a current-feedback op amp. Wideband inverting operation (and espe-

cially summing) is particularly suited to the OPA2677. Figure 14 shows a typical inverting configuration where the I/O impedances and signal gain from Figure 1 are retained in an inverting circuit configuration.

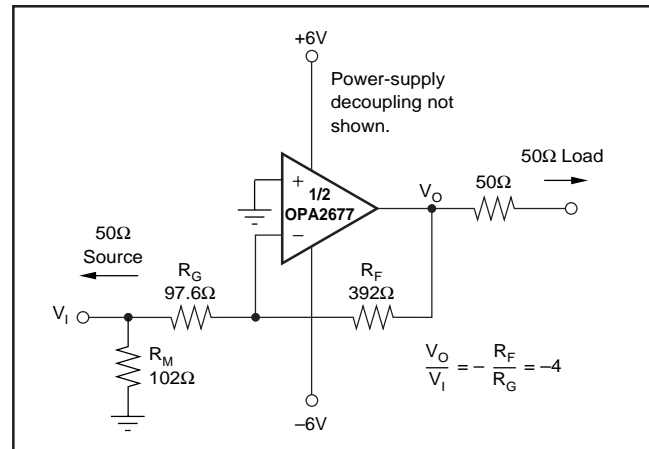


FIGURE 14. Inverting Gain of  $-4$  with Impedance Matching.

In the inverting configuration, two key design considerations must be noted. The first is that the gain resistor ( $R_G$ ) becomes part of the signal source input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PC board trace or other transmission line conductor), it is normally necessary to add an additional matching resistor to ground.  $R_G$ , by itself, is not normally set to the required input impedance since its value, along with the desired gain, will determine an  $R_F$ , which may be non-optimal from a frequency response standpoint. The total input impedance for the source becomes the parallel combination of  $R_G$  and  $R_M$ . The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and has a slight effect on the bandwidth through Equation 15. The values shown in Figure 13 have accounted for this by slightly decreasing  $R_F$  (from the optimum values) to re-optimize the bandwidth for the noise gain of Figure 13 ( $NG = 3.98$ ). In the example of Figure 14, the  $R_M$  value combines in parallel with the external  $50\Omega$  source impedance, yielding an effective driving impedance of  $50\Omega \parallel 102\Omega = 33.5\Omega$ . This impedance is added in series with  $R_G$  for calculating the noise gain—which gives  $NG = 3.98$ . This value, along with the inverting input impedance of  $22\Omega$ , are inserted into Equation 16 to get a feedback transimpedance nearly equal to the  $402\Omega$  optimum value. Note that the noninverting input in this bipolar supply inverting application is connected directly to ground. It is often suggested that an additional resistor be connected to ground on the noninverting input to achieve bias current error cancellation at the output. The input bias currents for a current-feedback op amp are not generally matched in either magnitude or polarity. Connecting a resistor to ground on the noninverting input of the OPA2677 in the circuit of Figure 14 actually provides additional gain for that input bias and noise currents, but does not decrease the output DC error since the input bias currents are not matched.

## OUTPUT CURRENT AND VOLTAGE

The OPA2677 provides output voltage and current capabilities that are unsurpassed in a low-cost dual monolithic op amp. Under no-load conditions at 25°C, the output voltage typically swings closer than 1V to either supply rail; tested at +25°C swing limit is within 1.1V of either rail. Into a 6Ω load (the minimum tested load), it delivers more than ±380mA continuous and > ±1.2A peak output current.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage times current (or V-I product) that is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot in the Typical Characteristics. The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA2677 output drive capabilities, noting that the graph is bounded by a safe operating area of 1W maximum internal power dissipation (in this case for 1 channel only). Superimposing resistor load lines onto the plot shows that the OPA2677 can drive ±4V into 10Ω or ±4.5V into 25Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±5.0V output swing capability, as shown in the Electrical Characteristics tables. The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Characteristics tables. As the output transistors deliver power, the junction temperatures increases, decreasing the  $V_{BE}$ S (increasing the available output voltage swing), and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications, since the output stage junction temperatures will be higher than the minimum specified operating ambient. To maintain maximum output stage linearity, no output short-circuit protection is provided. This is normally not a problem because most applications include a series-matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin (8-pin package), will in most cases, destroy the amplifier. If additional short-circuit protection is required, consider using the equivalent OPA2674 that includes output current limiting. Alternatively, a small series resistor may be included in the supply lines. Under heavy output loads this will reduce the available output voltage swing. A 5Ω series resistor in each power-supply lead will limit the internal power dissipation to less than 1W for an output short circuit while decreasing the available output voltage swing only 0.5V for up to 100mA desired load currents. Always place the 0.1μF power-supply decoupling capacitors after these supply current limiting resistors directly on the supply pins.

## DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an analog-to-digital (A/D) converter—including additional external capacitance that may be recommended to improve the A/D converter linearity. A high-speed, high open-loop gain amplifier such as the OPA2677 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested.

When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability. The Typical Characteristics show the recommended  $R_S$  vs Capacitive Load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2677. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2677 output pin (see the Board Layout Guidelines section).

## DISTORTION PERFORMANCE

The OPA2677 provides good distortion performance into a 100Ω load on ±6V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operation on a single +5V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 1), this is the sum of  $R_F + R_G$ , whereas in the inverting configuration it is just  $R_F$ . Also, providing an additional supply decoupling capacitor (0.01μF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Characteristics show the 2nd-harmonic increasing at a little less than the expected 2x rate whereas the 3rd-harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between it and the 2nd-harmonic

decreases less than the expected 6dB, whereas the difference between it and the 3rd-harmonic decreases by less than the expected 12dB. This also shows up in the 2-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low at low-output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For 2 tones centered at 20MHz, with 10dBm/tone into a matched 50Ω load (that is, 2V<sub>PP</sub> for each tone at the load, which requires 8V<sub>PP</sub> for the overall 2-tone envelope at the output pin), the Typical Characteristics show 63dBc difference between the test-tone power and the 3rd-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies.

## NOISE PERFORMANCE

Wideband current-feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA2677 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (24pA/√Hz) is significantly lower than earlier solutions whereas the input voltage noise (2.0nV/√Hz) is lower than most unity-gain stable, wideband voltage-feedback op amps. This low input voltage noise is achieved at the price of higher noninverting input current noise (16pA/√Hz). As long as the AC source impedance looking out of the noninverting node is less than 100Ω, this current noise does not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 15 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

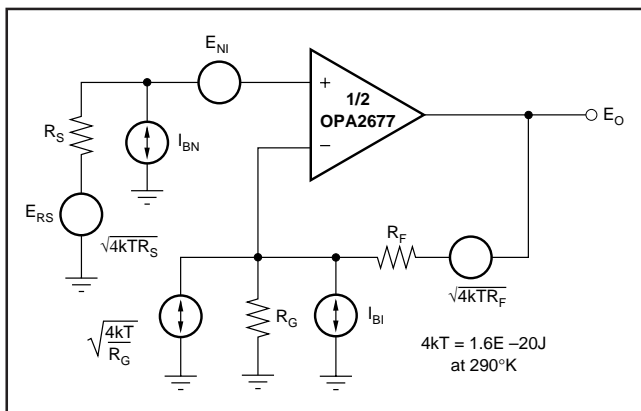


FIGURE 15. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 17 shows the general form for the output noise voltage using the terms shown in Figure 14.

$$E_O = \sqrt{\left( E_{NI}^2 + (I_{BN} \cdot R_S)^2 + 4kTR_S + (I_{BI} \cdot R_F)^2 + 4kTR_F NG \right)} \quad (17)$$

Dividing this expression by the noise gain ( $NG = (1 + R_F/R_G)$ ) gives the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 18.

$$E_N = \sqrt{\left( E_{NI}^2 + (I_{BN} \cdot R_S)^2 + 4kTR_S + \left( \frac{I_{BI} \cdot R_F}{NG} \right)^2 + \frac{4kTR_F}{NG} \right)} \quad (18)$$

Evaluating these two equations for the OPA2677 circuit and component values (see Figure 1) gives a total output spot noise voltage of 13.5nV/√Hz and a total equivalent input spot noise voltage of 3.3nV/√Hz. This total input referred spot noise voltage is higher than the 2.0nV/√Hz specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. If the feedback resistor is reduced in high-gain configurations (as suggested previously), the total input referred voltage noise given by Equation 18 approaches just the 2.0nV/√Hz of the op amp. For example, going to a gain of +10 using  $R_F = 298\Omega$  gives a total input referred noise of 2.3nV/√Hz.

## DIFFERENTIAL NOISE PERFORMANCE

As the OPA2677 is used as a differential driver in xDSL applications, it is important to analyze the noise in such a configuration. Figure 16 shows the op amp noise model for the differential configuration.

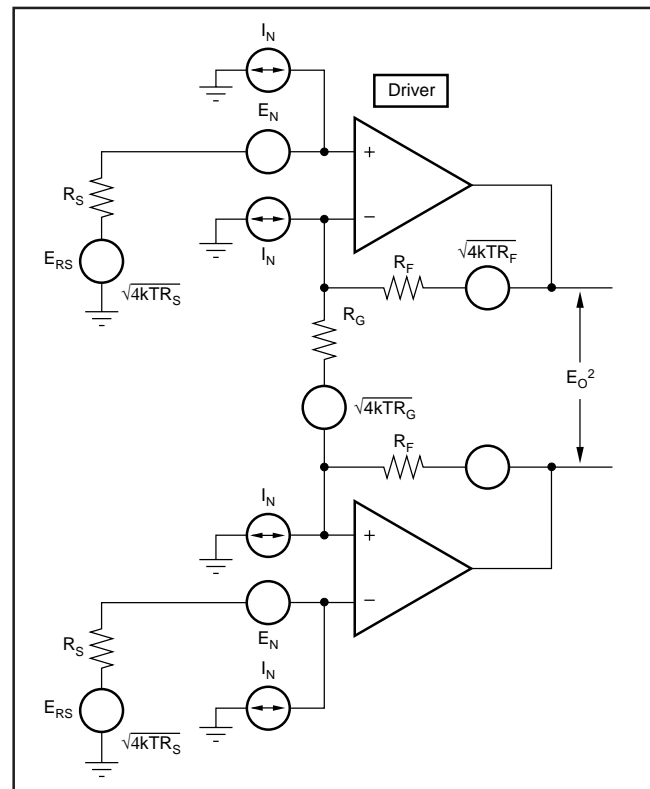


FIGURE 16. Differential Op Amp Noise Analysis Model.

As a reminder, the differential gain is expressed as:

$$G_D = 1 + \frac{2 \cdot R_F}{R_G} \quad (19)$$

The output noise can be expressed as shown below:

$$e_O = \sqrt{2 \cdot G_D^2 \cdot (e_N^2 + (i_N \cdot R_S)^2 + 4kTR_S) + 2(i_{iR_F})^2 + 2(4kTR_F G_D)} \quad (20)$$

Dividing this expression by the differential noise gain ( $G_D = (1 + 2R_F/R_G)$ ) gives the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 21.

$$(21)$$

$$e_O = \sqrt{2 \cdot (e_N^2 + (i_N \cdot R_S)^2 + 4kTR_S) + 2 \left( \frac{i_{iR_F}}{G_D} \right)^2 + 2 \left( \frac{4kTR_F}{G_D} \right)}$$

Evaluating these equations for the OPA2677 ADSL circuit and component values of Figure 6 gives a total output spot noise voltage of  $31.8 \text{ nV}/\sqrt{\text{Hz}}$  and a total equivalent input spot noise voltage of  $3.6 \text{ nV}/\sqrt{\text{Hz}}$ .

In order to minimize the output noise due to the noninverting input bias current noise, it is recommended to keep the noninverting source impedance as low as possible.

## DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp such as the OPA2677 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The Electrical Characteristics show an input offset voltage comparable to high-speed, voltage-feedback amplifiers; however, the two input bias currents are somewhat higher and are unmatched. While bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output DC offset for wideband current-feedback op amps. Because the two input bias currents are unrelated in both magnitude and polarity, matching the input source impedance to reduce error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst-case  $+25^\circ\text{C}$  input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$$V_{\text{OFF}} = \pm (NG \cdot V_{\text{OS(MAX)}}) + (I_{\text{BN}} \cdot R_S/2 \cdot NG) \pm (I_{\text{BI}} \cdot R_F)$$

where NG = noninverting signal gain

$$= \pm (4 \cdot 4.5 \text{ mV}) + (30 \mu\text{A} \cdot 25 \Omega \cdot 4) \pm (402 \Omega \cdot 30 \mu\text{A})$$

$$= \pm 18 \text{ mV} + 3 \text{ mV} \pm 12.06 \text{ mV}$$

$$V_{\text{OFF}} = -29.06 \text{ mV to } +35.06 \text{ mV}$$

## THERMAL ANALYSIS

Due to the high output power capability of the OPA2677, heat-sinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature sets the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed  $175^\circ\text{C}$ . Operating junction temperature ( $T_J$ ) is given by  $T_A + P_D \cdot \theta_{JA}$ . The total internal

power dissipation ( $P_D$ ) is the sum of quiescent power ( $P_{DQ}$ ) and additional power dissipation in the output stage ( $P_{DL}$ ) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part.  $P_{DL}$  depends on the required output signal and load, but for a grounded resistive load,  $P_{DL}$  is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition,  $P_{DL} = V_S^2 / (4 \cdot R_L)$  where  $R_L$  includes feedback network loading. Note that it is the power in the output stage and not into the load that determines internal power dissipation. As a worst-case example, compute the maximum  $T_J$  using an OPA2677 SO-8 in the circuit of Figure 1 operating at the maximum specified ambient temperature of  $+85^\circ\text{C}$  with both outputs driving a grounded  $20 \Omega$  load to  $+2.5 \text{ V}$ .

$$P_D = 12 \text{ V} \cdot 18 \text{ mA} + 2 \cdot [6^2 / (4 \cdot (20 \Omega \parallel 534 \Omega))] = 882 \text{ mW}$$

$$\text{Maximum } T_J = +85^\circ\text{C} + (0.83 \cdot 125^\circ\text{C/W}) = 170^\circ\text{C}$$

This absolute worst-case condition exceeds specified maximum junction temperature. This extreme case is not normally encountered. Where high internal power dissipation is anticipated, consider the thermal slug package version.

## BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA2677 requires careful attention to board layout parasitic and external component types. Recommendations that optimize performance include:

**a) Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

**b) Minimize the distance** ( $< 0.25''$ ) from the power-supply pins to high-frequency  $0.1 \mu\text{F}$  decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections (on pins 4 and 7) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves 2nd-harmonic distortion performance. Larger ( $2.2 \mu\text{F}$  to  $6.8 \mu\text{F}$ ) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These can be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

**c) Careful selection and placement of external components preserve the high-frequency performance of the OPA2677.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high-frequency performance.

Again, keep leads and PC board trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Although the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing the value reduces the bandwidth, whereas decreasing it gives a more peaked frequency response. The 402Ω feedback resistor used in the Typical Characteristics at a gain of +4 on ±6V supplies is a good starting point for design. Note that a 511Ω feedback resistor, rather than a direct short, is recommended for the unity-gain follower application. A current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability.

**d) Connections to other wideband devices** on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set  $R_S$  from the plot of Recommended  $R_S$  vs Capacitive Load. Low parasitic capacitive loads (< 5pF) may not need an  $R_S$  because the OPA2677 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board; in fact, a higher impedance environment improves distortion (see the distortion versus load plots). With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2677 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device.

This total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2677 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of  $R_S$  vs Capacitive

Load. However, this does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

**e) Socketing a high-speed part like the OPA2677 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2677 directly onto the board.

**f) Use the  $-V_S$  plane to conduct heat out** of the PSO-8 power packages (OPA2677H). This package attaches the die directly to a metal slug in the bottom, which should be soldered to the board. This slug needs to be connected electrically to the same voltage plane so the most negative supply applied to the OPA2677 (in Figure 6, this would be ground), which must have a minimum area of 2" x 2" (50mm x 50mm) to produce the  $\theta_{JA}$  values in the specifications table. More details can be found in the data sheets that accompany the PSO-8 demo board described in the Demonstration Board section of this data sheet.

## INPUT AND ESD PROTECTION

The OPA2677 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices and are reflected in the absolute maximum ratings table. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 17.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2677), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, since high values degrade both noise performance and frequency response.

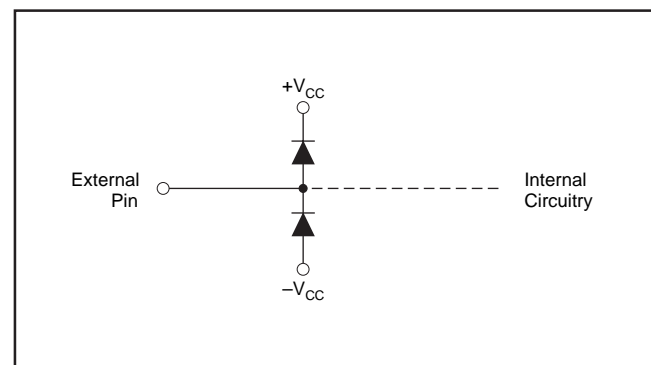
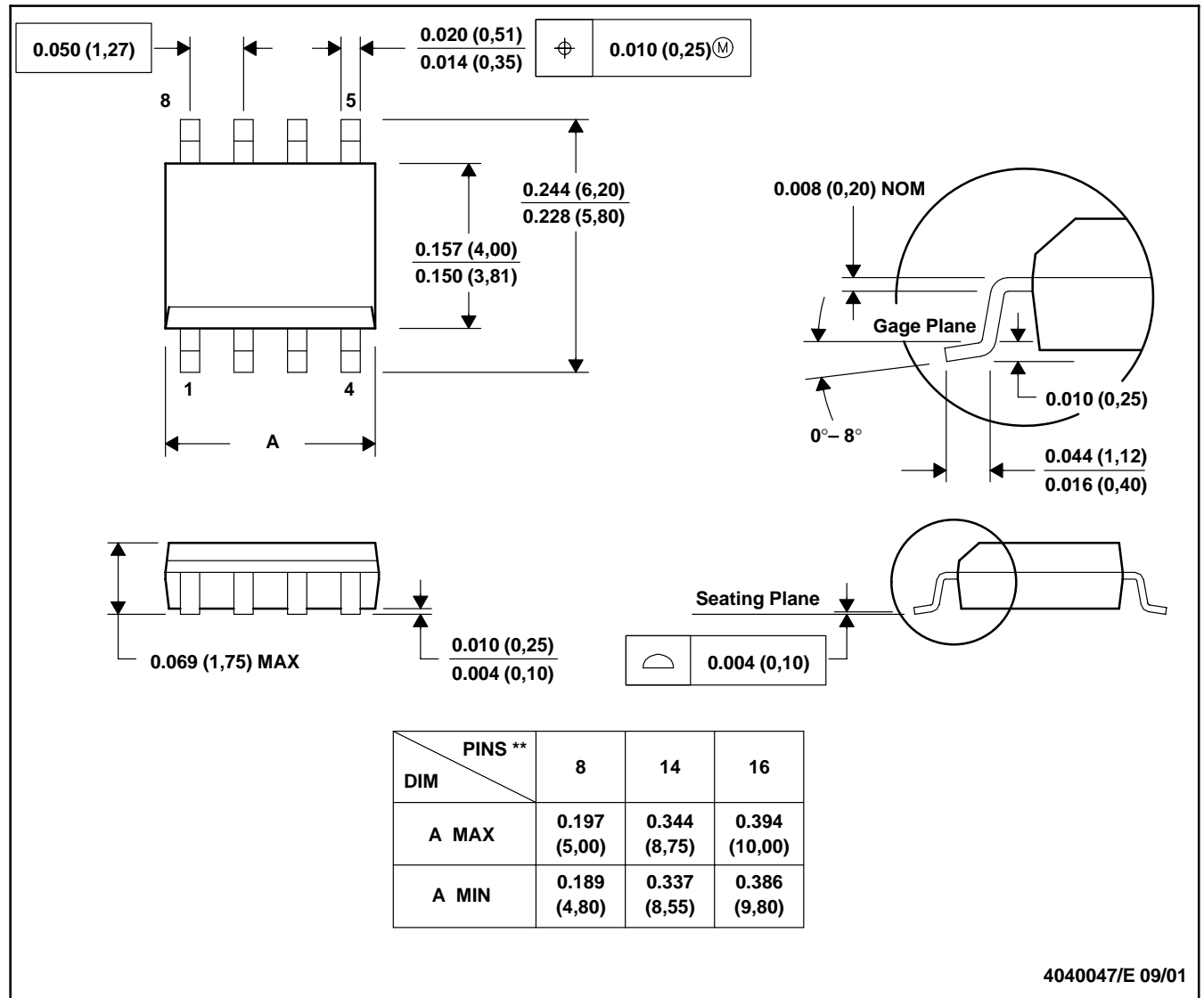


FIGURE 17. Internal ESD Protection.

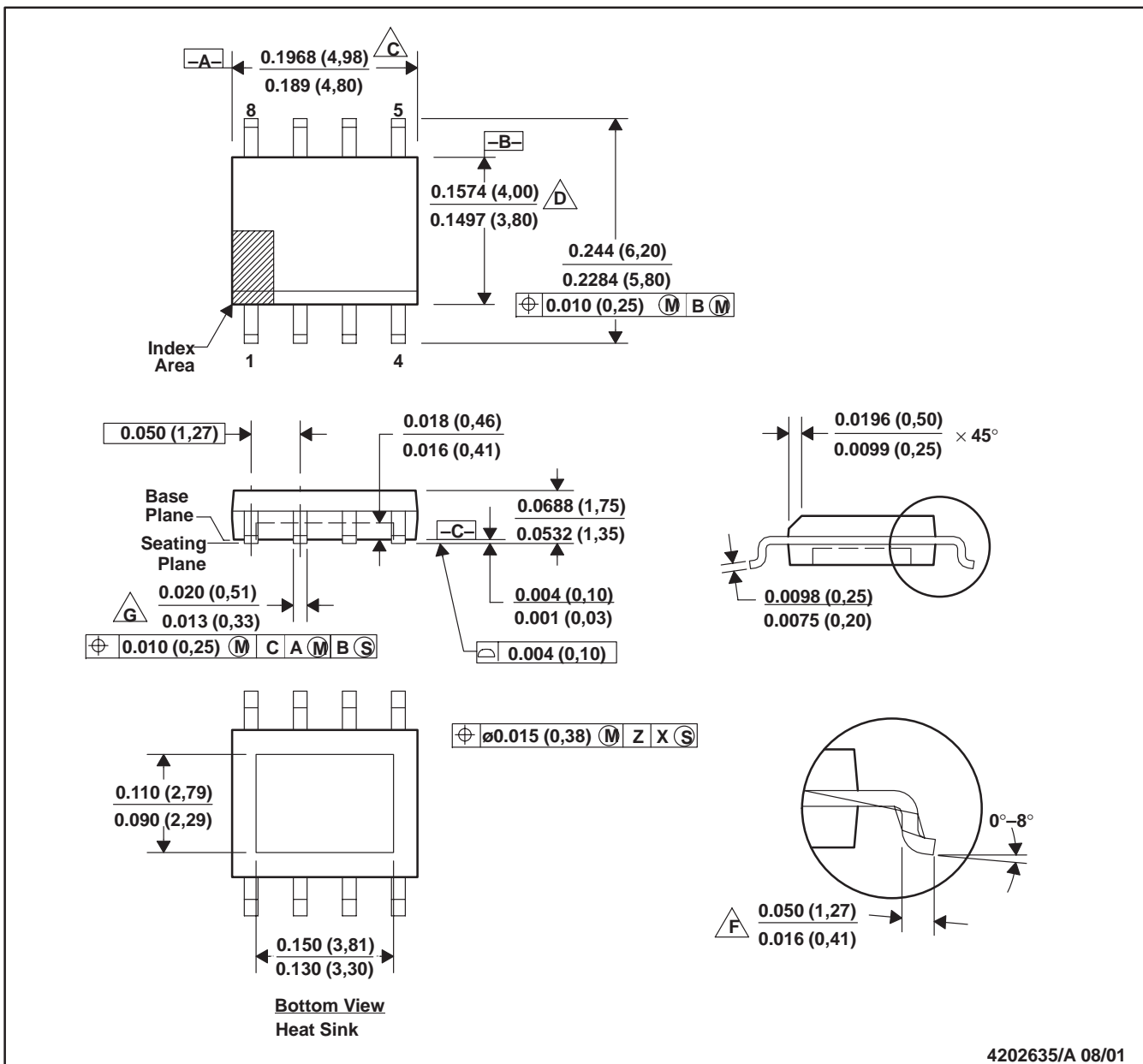
D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.006 (0,15) per side.  
 D. Body width dimension does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 (0,25) per side.  
 E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.  
 F. Lead dimension is the length of terminal for soldering to a substrate.  
 G. The lead width, as measured 0.014 (0,36) or greater above the seating plane, shall not exceed a maximum value of 0.024 (0,61).  
 H. Lead-to-lead coplanarity shall be less than 0.004 (0,10) from Seating Plane.  
 I. Falls within JEDEC MS-012-AA.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
OPA2677H	ACTIVE	HSOP	DTJ	8	100	None	Call TI	Level-3-220C-168 HR
OPA2677H/2K5	ACTIVE	HSOP	DTJ	8	2500	None	Call TI	Level-3-220C-168 HR
OPA2677T	ACTIVE	SOIC	D	16	48	None	CU SNPB	Level-3-260C-168 HR
OPA2677T/2K5	ACTIVE	SOIC	D	16	2500	None	CU SNPB	Level-3-260C-168 HR
OPA2677U	ACTIVE	SOIC	D	8	100	None	CU NIPDAU	Level-3-220C-168 HR
OPA2677U/2K5	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-3-220C-168 HR
OPA2677U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2677UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

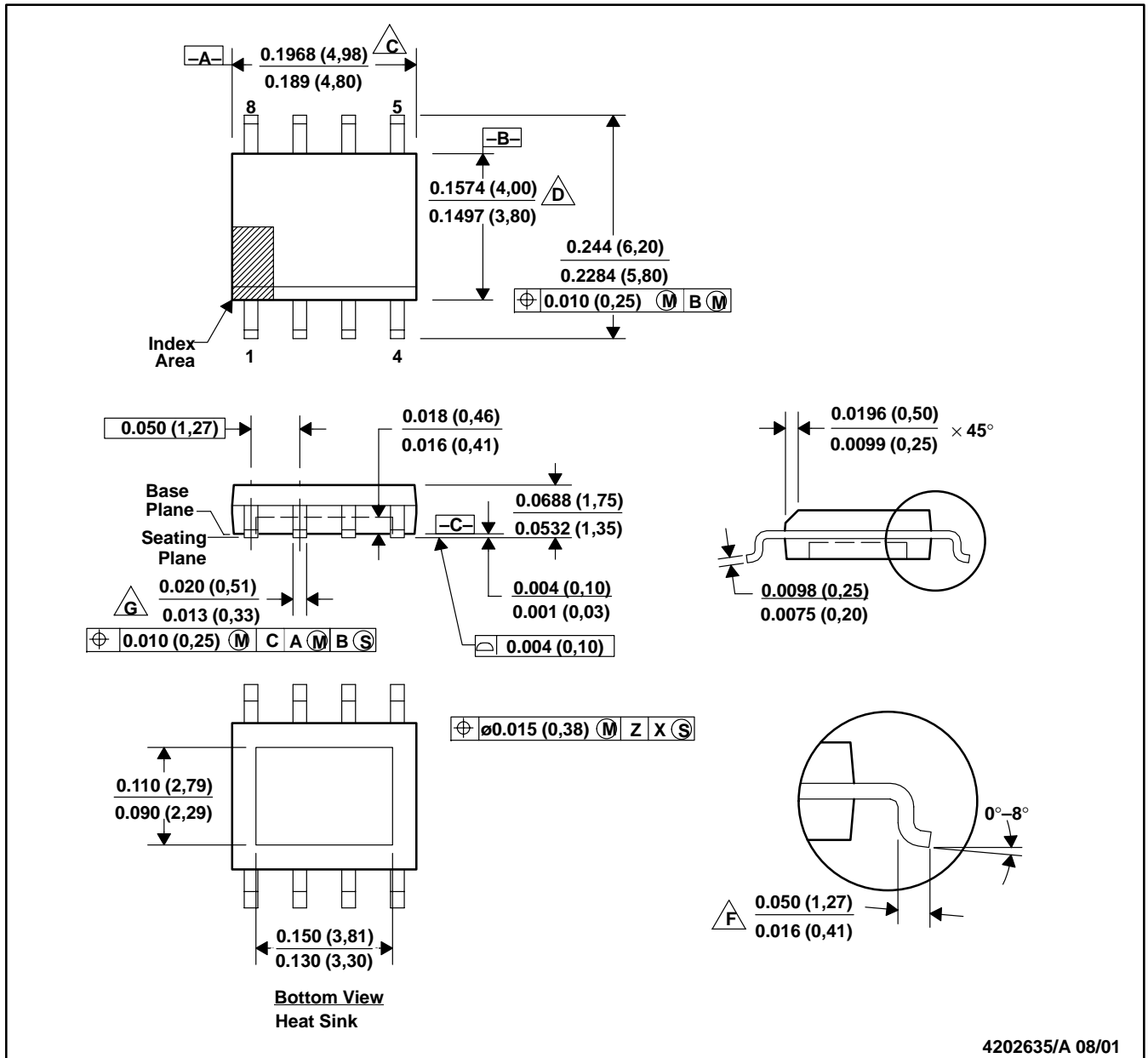
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DTJ (R-PDSO-G8)

PLASTIC SMALL-OUTLINE

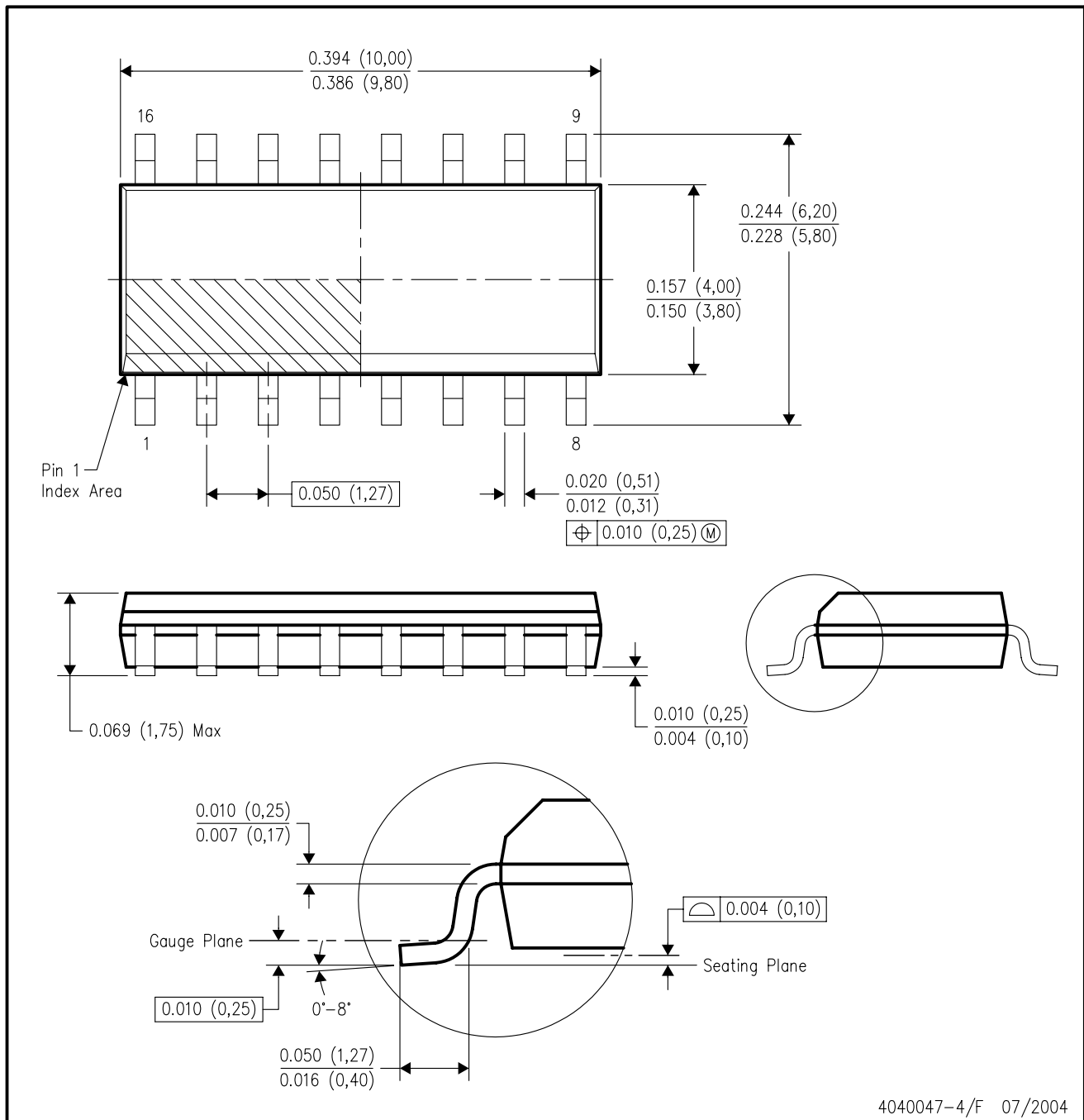


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.006 (0,15) per side.  
 D. Body width dimension does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 (0,25) per side.  
 E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.  
 F. Lead dimension is the length of terminal for soldering to a substrate.

- G. The lead width, as measured 0.014 (0,36) or greater above the seating plane, shall not exceed a maximum value of 0.024 (0,61).  
 H. Lead-to-lead coplanarity shall be less than 0.004 (0,10) from Seating Plane.  
 I. Falls within JEDEC MS-012-AA.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

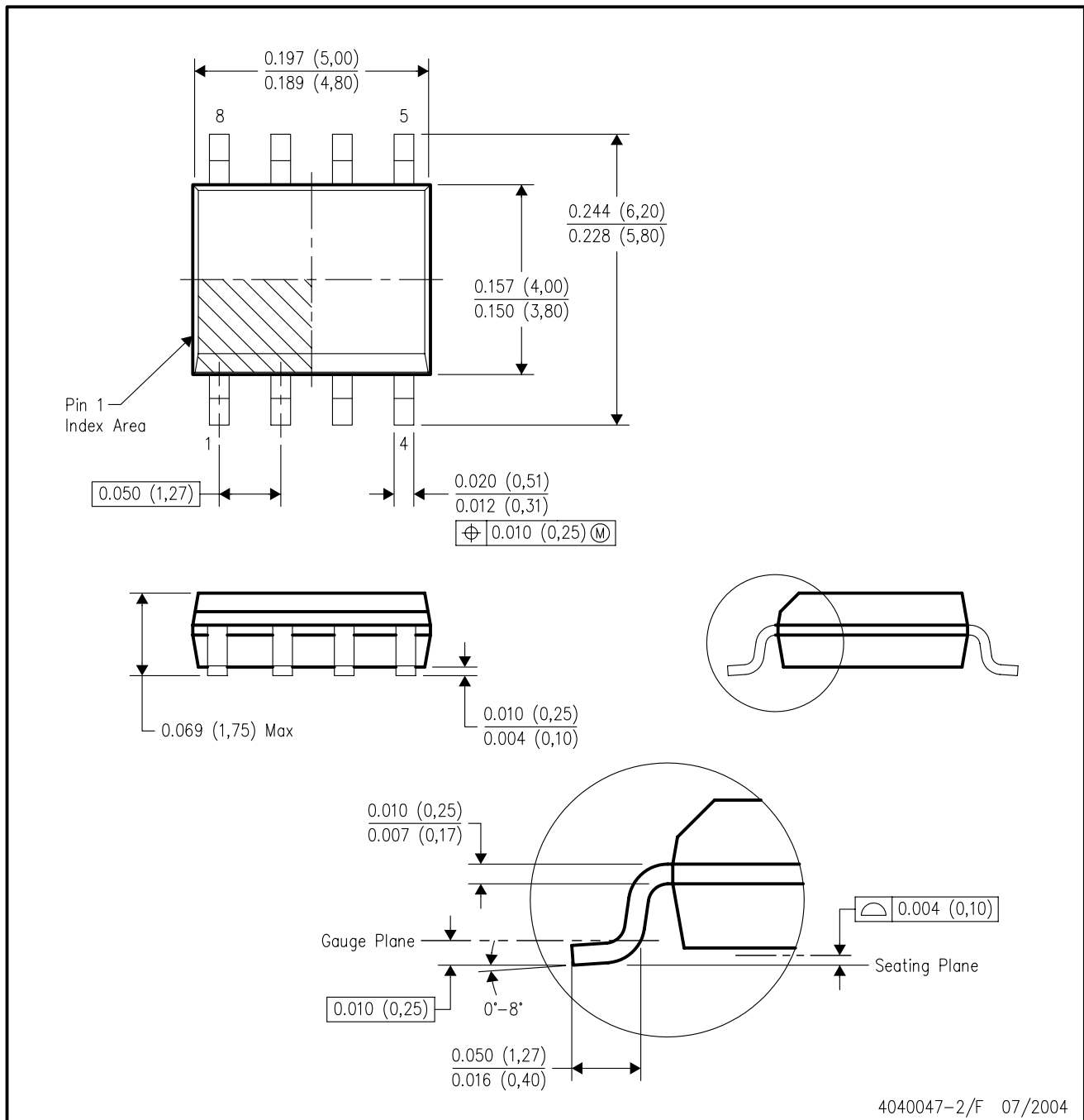


4040047-4/F 07/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AC.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AA.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265