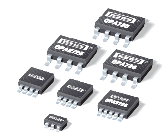
Burr-Brown Products from Texas Instruments



OPA725, OPA2725
OPA726, OPA2726

SBOS278B − SEPTEMBER 2003 − REVISED JANUARY 2004

Very Low Noise, High-Speed, 12V CMOS Operational Amplifier

FEATURES

- BANDWIDTH: 20MHz
- SLEW RATE: 30V/μs
- FAST 16-BIT SETTLING TIME
- LOW NOISE: 6nV/√Hz (typ) at 100kHz
- EXCELLENT CMRR, PSRR, and A_{OL}
- RAIL-TO-RAIL OUTPUT
- CM RANGE INCLUDES GND
- THD+N: 0.0003% (typ) at 1kHz
- QUIESCENT CURRENT: 5.5mA/ch (max)
- SUPPLY VOLTAGE: 4V to 12V
- SHUTDOWN MODE (OPAx726): 6μA/ch

APPLICATIONS

- OPTICAL NETWORKING
- TRANSIMPEDANCE AMPLIFIERS
- INTEGRATORS
- ACTIVE FILTERS
- A/D CONVERTER BUFFERS
- I/V CONVERTER FOR DACs
- PORTABLE AUDIO
- PROCESS CONTROL
- TEST EQUIPMENT

OPA725 RELATED PRODUCTS

FEATURES	PRODUCT
10MHz, 16V, 16V/μs, 8.5nV/√Hz at 1kHz	TLC080
8MHz, 36V, FET Input, 20V/μs, 8.5nV/√Hz at 1kHz	OPA132
100MHz, 5.5V, Precision Transimpedance Amplifier	OPA380
500MHz, ±5V, FET Input, 290V/μs, 7nV/√Hz at 100kHz	OPA656
7MHz, 12V, RRIO, 10V/μs, 30nV/√Hz at 10kHz	OPA743
16-Bit, 250kSPS, 4-Channel, Parallel Output ADC	ADS8342

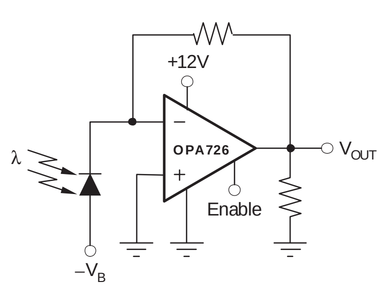
DESCRIPTION

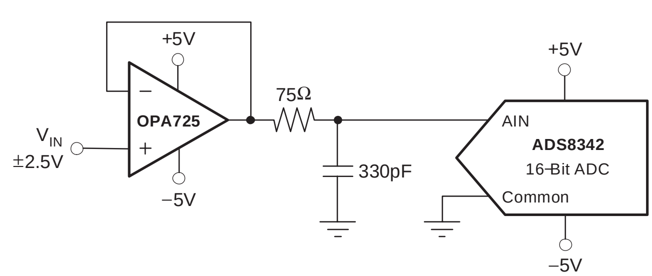
The OPA725 and OPA726 series op amps use a state-of-the-art 12V analog CMOS process, and combine outstanding ac performance with low bias current and excellent CMRR, PSRR, and A_{OL}. The 20MHz Gain-Bandwidth (GBW) Product is achieved by using a proprietary and patent-pending output stage design. These characteristics allow excellent 16-bit settling times for driving 16-bit Analog-to-Digital converters (ADCs).

Excellent ac characteristics, such as 20MHz GBW, 30V/μs slew rate and 0.0003% THD+N make the OPA725 and OPA726 well-suited for communication, high-end audio, and active filter applications. With a bias current of less than 200pA, they are well-suited for use as transimpedance (I/V-conversion) amplifiers for monitoring optical power in ONET applications.

The OPA725 and OPA726 op amps can be used in single-supply applications from 4V up to 12V, or dual-supply from ±2V to ±6V. The output swings to within 150mV of the rails, maximizing dynamic range. The shutdown versions (OPAx726) reduce the quiescent current to less than 6μA and feature a reference pin for easy shutdown operation with standard CMOS logic in dual-supply applications.

The OPA725 (single) is available in SOT23-5 and SO-8 packages, and the OPA2725 (dual) is available in MSOP-8 and SO-8 packages. The OPA726 (single with shutdown) is available in MSOP-8 and SO-8. The OPA2726 (dual with shutdown) is available in MSOP-10. All versions are specified for operation from −40°C to +125°C.





ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Non-Shutdown						
OPA725	SOT23-5	DBV	−40°C to +125°C	OALI	OPA725AIDBVT	Tape and Reel, 250
″	″	″	″	″	OPA725AIDBVR	Tape and Reel, 3000
OPA725	SO-8	D	−40°C to +125°C	OPA725A	OPA725AID	Rails, 100
″	″	″	″	″	OPA725AIDR	Tape and Reel, 2500
OPA2725	SO-8	D	−40°C to +125°C	OPA2725A	OPA2725AID	Rails, 100
″	″	″	″	″	OPA2725AIDR	Tape and Reel, 2500
OPA2725	MSOP-8	DGK	−40°C to +125°C	BGM	OPA2725AIDGKT	Tape and Reel, 250
″	″	″	″	″	OPA2725AIDGKR	Tape and Reel, 2500
Shutdown						
OPA726	SO-8	D	−40°C to +125°C	OPA726A	OPA726AID	Rails, 100
″	″	″	″	″	OPA726AIDR	Tape and Reel, 2500
OPA726	MSOP-8	DGK	−40°C to +125°C	BHC	OPA726AIDGKT	Tape and Reel, 250
″	″	″	″	″	OPA726AIDGKR	Tape and Reel, 2500
OPA2726	MSOP-10	DGS	−40°C to +125°C	BHB	OPA2726AIDGST	Tape and Reel, 250
″	″	″	″	″	OPA2726AIDGSR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this datasheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+13.2V
Signal Input Terminals, Voltage(2)	−0.5V to (V+) + 0.5V
Current(2)	±10mA
Output Short Circuit(3)	Continuous
Operating Temperature	−55°C to +125°C
Storage Termperature	−55°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
ESD Rating (Human Body Model)	1000 V

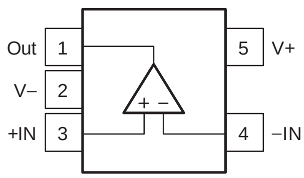
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

(3) Short-circuit to ground, one amplifier per package.

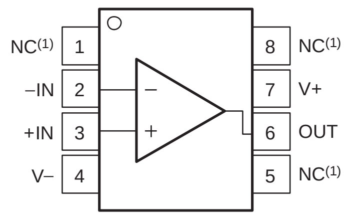
PIN CONFIGURATIONS

OPA725



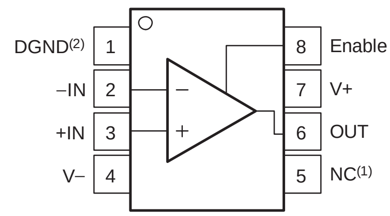
SOT23−5

OPA725



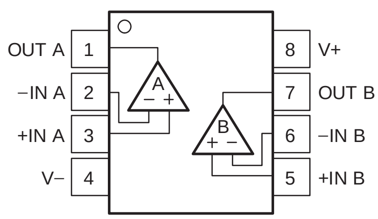
SO−8

OPA726



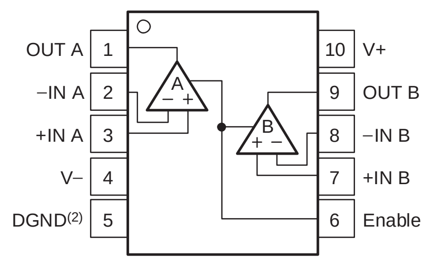
SO−8, MSOP−8

OPA2725



SO−8, MSOP−8

OPA2726



MSOP−10

(1) NC denotes no internal connection.
(2) DGND = reference voltage for Enable Reference pin. Voltage on this pin will be the voltage to which the Enable Reference pin is referenced.

ELECTRICAL CHARACTERISTICS: V_S = +4V to +12V or V_S = ±2V to ±6V

Boldface limits apply over the specified temperature range, **T_A = −40°C to +125°C.**

At T_A = +25°C, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		CONDITIONS	OPA725, OPA726, OPA2725, OPA2726			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}					
OPA725, OPA726		V_S = ±6V, V_{CM} = 0V		1.2	3	mV
OPA2725, OPA2726		V_S = ±6V, V_{CM} = 0V		1.5	5	mV
Drift	**dV_{OS}/dT**			**4**		**μV/°C**
vs Power Supply	PSRR	V_S = ±2V to ±6V, V_{CM} = V−		30	100	μV/V
Over Temperature		**V_S = ±2V to ±6V, V_{CM} = V−**			**150**	**μV/V**
Channel Separation, DC				1		μV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			30	200	pA
Over Temperature			See Typical Characteristics			
Input Offset Current	I_{OS}			10	50	pA
NOISE						
Input Voltage Noise, f = 0.1Hz to 10Hz	e_n	V_S = ±6V, V_{CM} = 0V		10		μV_{PP}
Input Voltage Noise Density, f = 10kHz	e_n	V_S = ±6V, V_{CM} = 0V		10		nV/√Hz
Input Voltage Noise Density, f = 100kHz	e_n	V_S = ±6V, V_{CM} = 0V		6		nV/√Hz
Input Current Noise Density, f = 1kHz	i_n	V_S = ±6V, V_{CM} = 0V		2.5		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−)		(V+) − 2	V
Common-Mode Rejection Ratio	CMRR	(V−) ≤ V_{CM} ≤ (V+) − 2V	88	94		dB
Over Temperature		**(V−) ≤ V_{CM} ≤ (V+) − 2V**	**84**			**dB**
		(V−) ≤ V_{CM} ≤ (V+) − 3V	94	100		dB
Over Temperature		**(V−) ≤ V_{CM} ≤ (V+) − 3V**	**84**			**dB**
INPUT IMPEDANCE						
Differential				10^{11} ∥ 5		Ω ∥ pF
Common-Mode				10^{11} ∥ 4		Ω ∥ pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}					
OPA725, OPA726		R_L = 100kΩ, 0.15V < V_O < (V+) − 0.15V	110	120		dB
Over Temperature		**R_L = 100kΩ, 0.15V < V_O < (V+) − 0.15V**	**100**			**dB**
OPA2725, OPA2726		R_L = 100kΩ, 0.175V < V_O < (V+) − 0.175V	110	120		dB
Over Temperature		**R_L = 100kΩ, 0.175V < V_O < (V+) − 0.175V**	**100**			**dB**
OPA725, OPA726		R_L = 1kΩ, 0.25V < V_O < (V+) − 0.25V	106	116		dB
Over Temperature		**R_L = 1kΩ, 0.25V < V_O < (V+) − 0.25V**	**96**			**dB**
OPA2725, OPA2726		R_L = 2kΩ, 0.25V < V_O < (V+) − 0.25V	106	116		dB
Over Temperature		**R_L = 2kΩ, 0.25V < V_O < (V+) − 0.25V**	**96**			**dB**
FREQUENCY RESPONSE		C_L = 20pF				
Gain-Bandwidth Product	GBW			20		MHz
Slew Rate	SR	G = +1		30		V/μs
Settling Time, 0.1%	t_S	V_S = ±6V, 5V Step, G = +1		350		ns
0.01%		V_S = ±6V, 5V Step, G = +1		450		ns
Overload Recovery Time		V_{IN} • Gain > V_S		50		ns
Total Harmonic Distortion + Noise	THD+N	V_S = ±6V, V_{OUT} = $2V_{RMS}$, R_L = 600Ω, G = +1, f = 1kHz		0.0003		%

ELECTRICAL CHARACTERISTICS: V_S = +4V to +12V or V_S = ±2V to ±6V (continued)

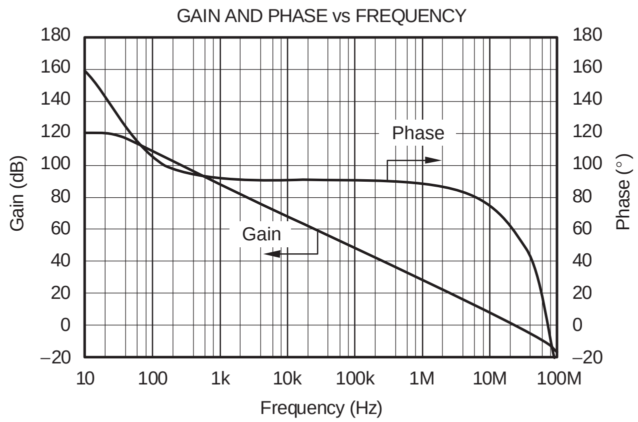
Boldface limits apply over the specified temperature range, **T_A = −40°C to +125°C.**

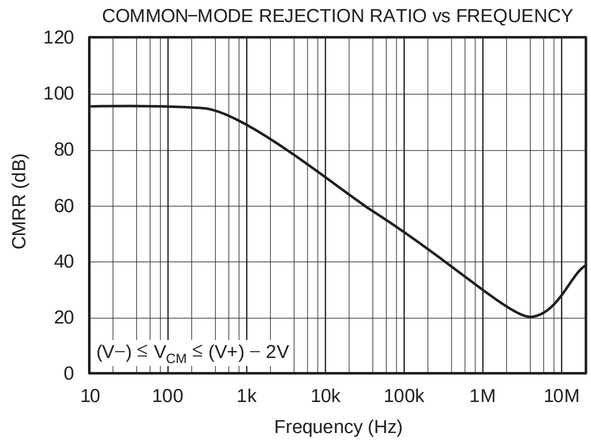
At T_A = +25°C, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

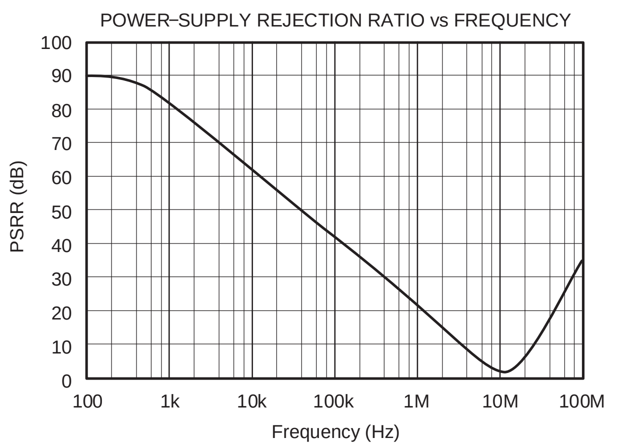
PARAMETER		CONDITIONS	OPA725, OPA726, OPA2725, OPA2726 MIN	TYP	MAX	UNIT
OUTPUT						
Voltage Output Swing from Rail						
OPA725, OPA726		R_L = 100kΩ, A_{OL} > 110dB		100	150	mV
Over Temperature		**R_L = 100kΩ, A_{OL} > 100dB**			**150**	**mV**
OPA2725, OPA2726		R_L = 100kΩ, A_{OL} > 110dB		125	175	mV
Over Temperature		**R_L = 100kΩ, A_{OL} > 100dB**			**175**	**mV**
OPA725, OPA726		R_L = 1kΩ, A_{OL} > 106dB		200	250	mV
Over Temperature		**R_L = 1kΩ, A_{OL} > 96dB**			**250**	**mV**
OPA2725, OPA2726		R_L = 2kΩ, A_{OL} > 106dB		200	250	mV
Over Temperature		**R_L = 2kΩ, A_{OL} > 96dB**			**250**	**mV**
Output Current	I_{OUT}	$\lvert V_S - V_{OUT} \rvert$ < 1V		40		mA
Short-Circuit Current	I_{SC}			±55		mA
Capacitive Load Drive	C_{LOAD}			See Typical Characteristics		
Open-Loop Output Impedance		f = 1MHz, I_O = 0		40		Ω
ENABLE/SHUTDOWN (OPAx726)						
t_{OFF}				5		µs
t_{ON}				30		µs
Enable Reference (DGND) Voltage Range	V_{DGND}		V−		(V+) − 2	V
V_L (shutdown)					< V_{DGND} +0.8V	V
V_H (amplifier is active)			> V_{DGND} +2V			V
Input Disable Current		Ref Pin = Enable Pin = V−		5		µA
I_{QSD} (per amplifier)				6	15	µA
POWER SUPPLY						
Specified Voltage Range	V_S		4		12	V
Operating Voltage Range	V_S			3.5 to 13.2		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		4.3	5.5	mA
Over Temperature					**6**	**mA**
TEMPERATURE RANGE						
Specified Range			−40		125	°C
Operating Range			−55		125	°C
Storage Range			−55		150	°C
Thermal Resistance	θ_{JA}					
SOT23-5				200		°C/W
MSOP-8, MSOP-10, SO-8				150		°C/W

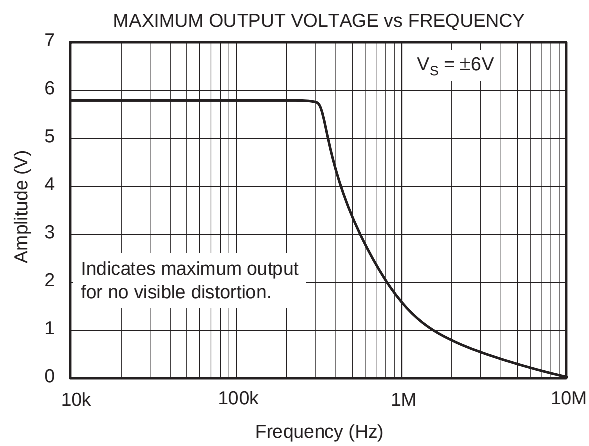
TYPICAL CHARACTERISTICS

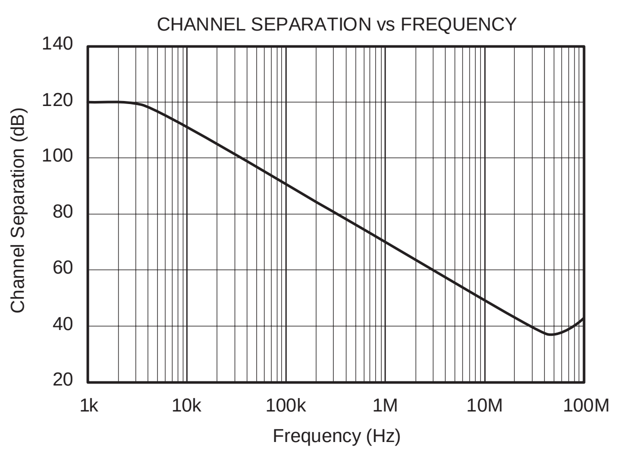
At T_A = +25°C, V_S = ±6V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

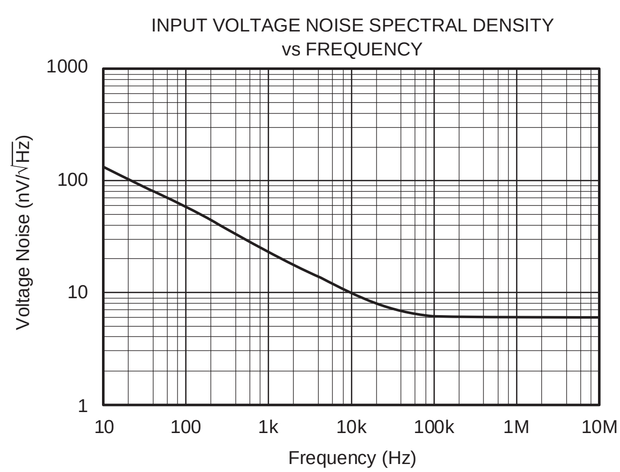






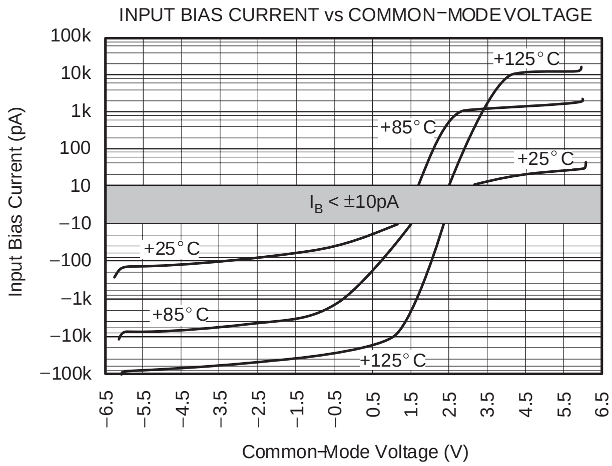


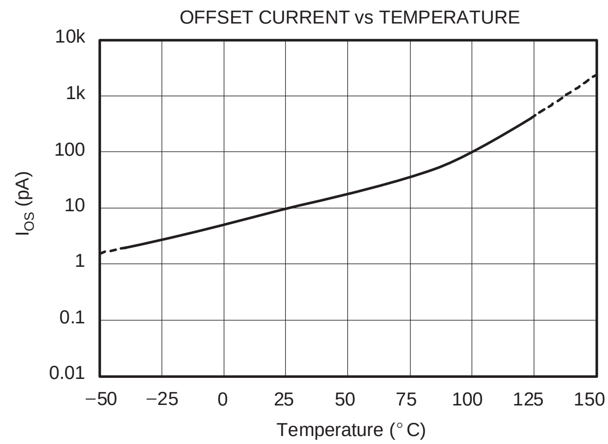


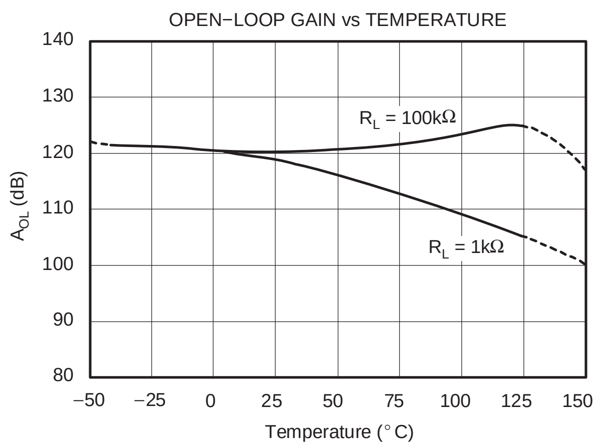


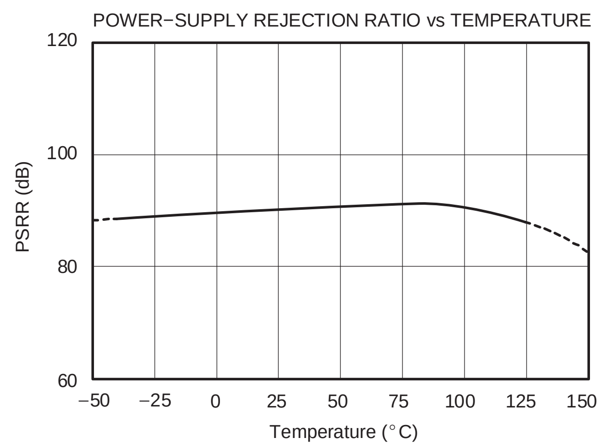
TYPICAL CHARACTERISTICS (continued)

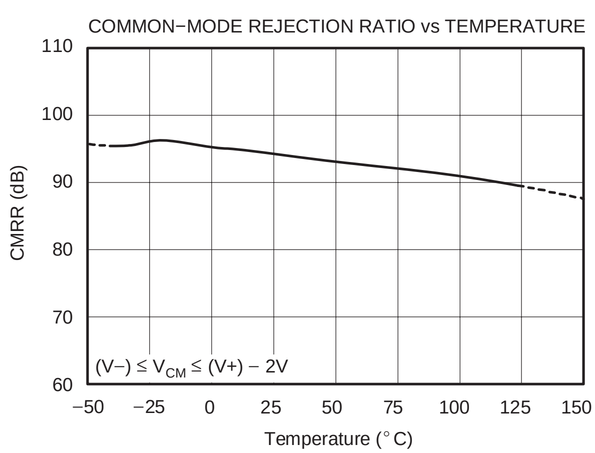
At T_A = +25°C, V_S = ±6V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

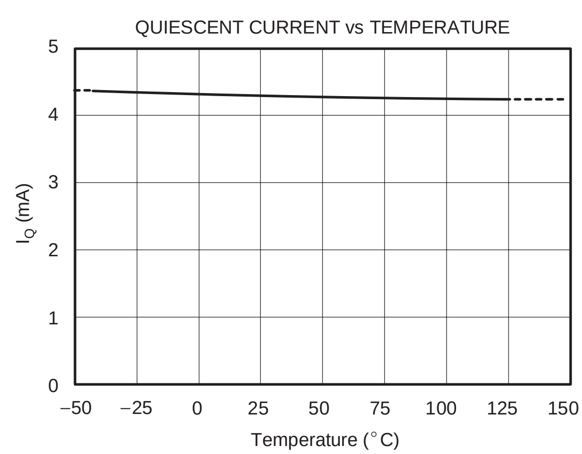






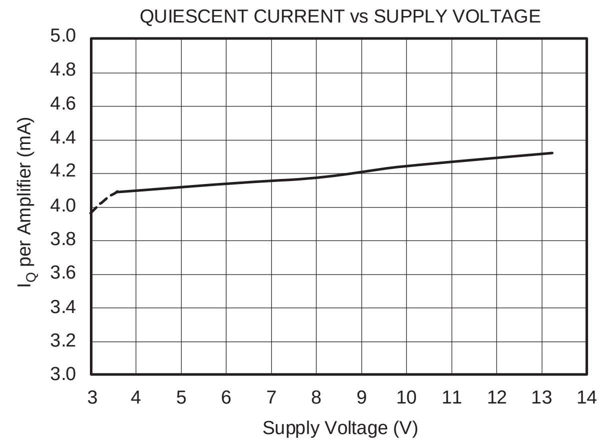


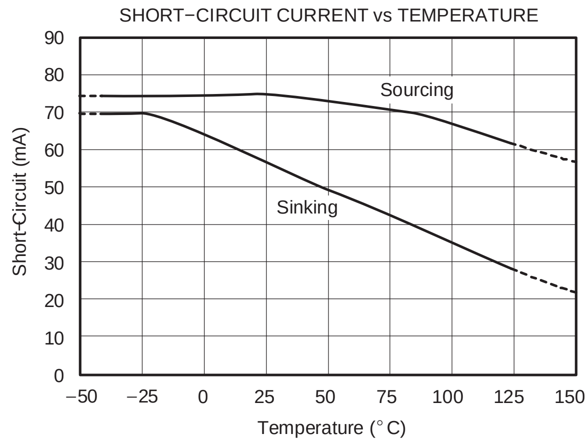


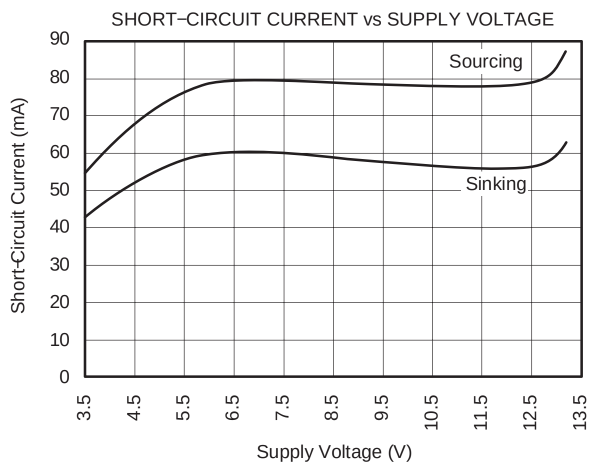


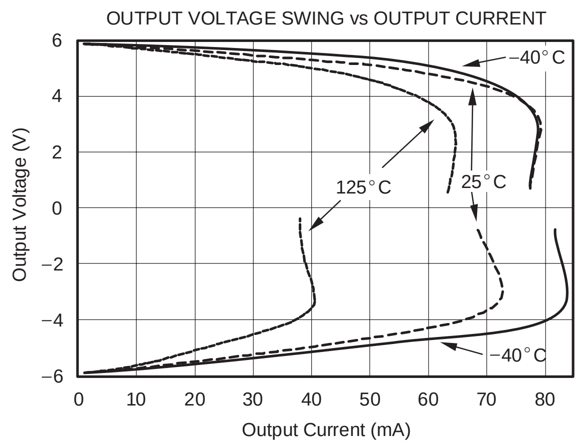
TYPICAL CHARACTERISTICS (continued)

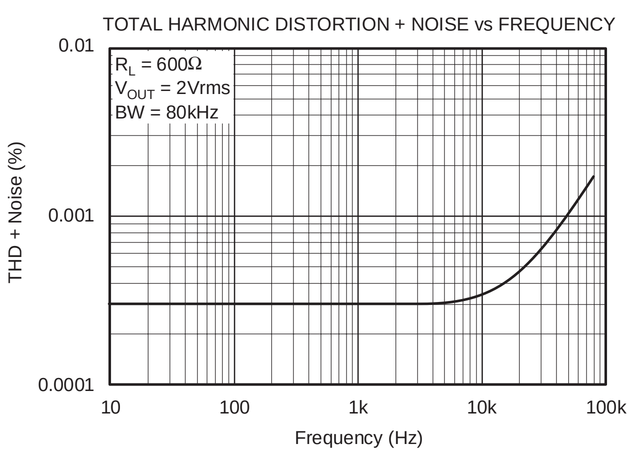
At T_A = +25°C, V_S = ±6V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

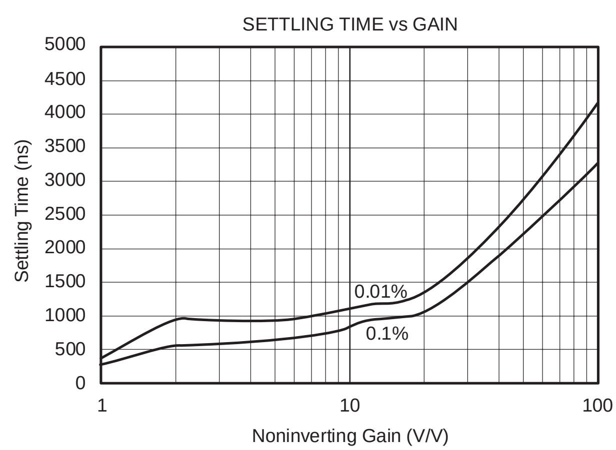








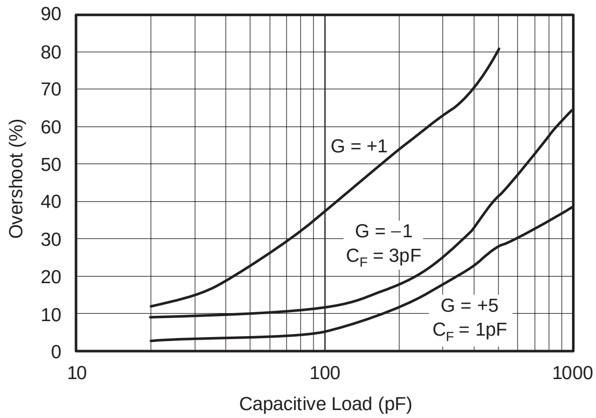




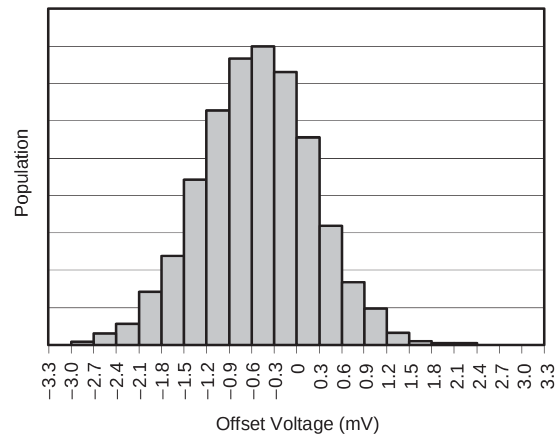
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±6V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

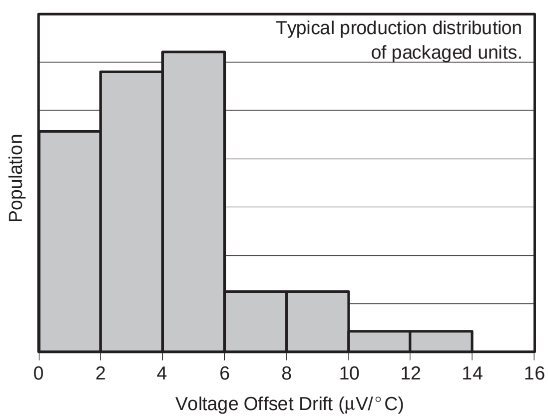
SMALL−SIGNAL OVERSHOOT vs CAPACITIVE LOAD



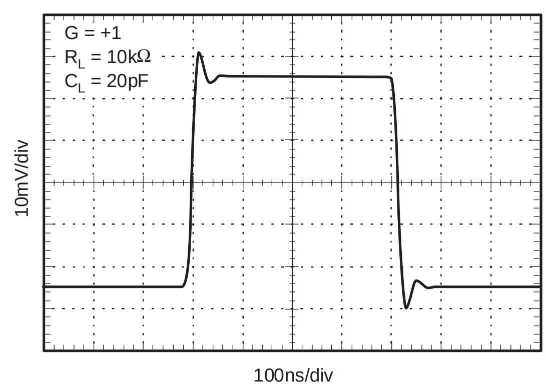
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



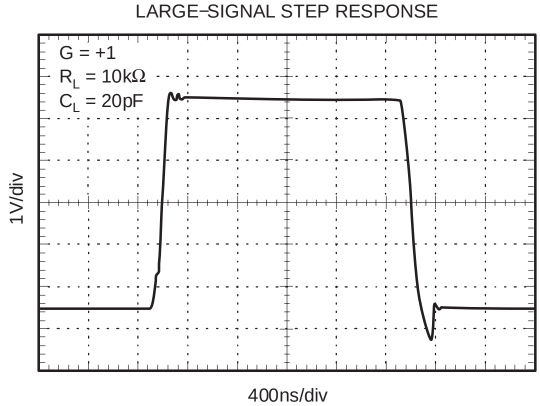
VOLTAGE OFFSET DRIFT PRODUCTION DISTRIBUTION



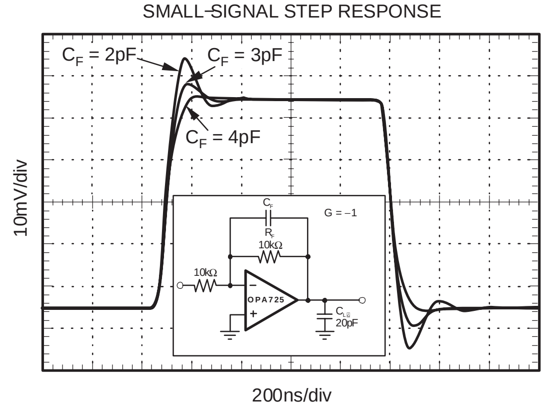
SMALL−SIGNAL STEP RESPONSE



LARGE−SIGNAL STEP RESPONSE



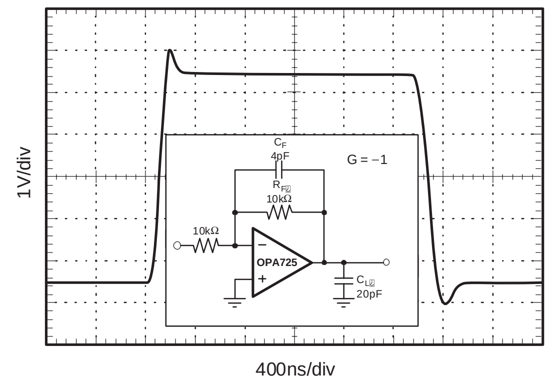
SMALL−SIGNAL STEP RESPONSE



TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±6V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

LARGE−SIGNAL STEP RESPONSE



APPLICATIONS INFORMATION

OPA725 and OPA726 series 20MHz CMOS op amps have a fast slew rate, low noise, and excellent PSRR, CMRR, and A_{OL}. These op amps can operate on typically 4.3mA quiescent current from a single (or split) supply in the range of 4V to 12V (±2V to ±6V), making them highly versatile and easy to use. They are stable in a unity-gain configuration.

Power-supply pins should be bypassed with 1nF ceramic capacitors in parallel with 1µF tantalum capacitors.

OPERATING VOLTAGE

OPA725 series op amps are specified from 4V to 12V supplies over a temperature range of −40°C to +125°C. They will operate well in ±5V or +5V to +12V power-supply systems. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

ENABLE/SHUTDOWN

OPA725 series op amps require approximately 4.3mA quiescent current. The enable/shutdown feature of the OPA726 allows the op amp to be shut off to reduce this current to approximately 6µA.

The enable/shutdown input is referenced to the Enable Reference Pin, DGND (see Pin Configurations). This pin can be connected to logic ground in dual-supply op amp configurations to avoid level-shifting the enable logic signal, as shown in Figure 1.

The Enable Reference Pin voltage, V_{DGND}, must not exceed (V+) − 2V. It may be set as low as V−. The amplifier is enabled when the Enable Pin voltage is greater than V_{DGND} + 2V. The amplifier is disabled (shutdown) if the Enable Pin voltage is less than V_{DGND} + 0.8V. The Enable Pin is connected to internal pull-up circuitry and will enable the device if left unconnected.

COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPA725 and OPA726 series extends from V− to (V+) − 2V.

Common-mode rejection is excellent throughout the input voltage range from V− to (V+) − 3V. CMRR decreases somewhat as the common-mode voltage extends to (V+) − 2V, but remains very good and is tested throughout this range. See the Electrical Characteristics table for details.

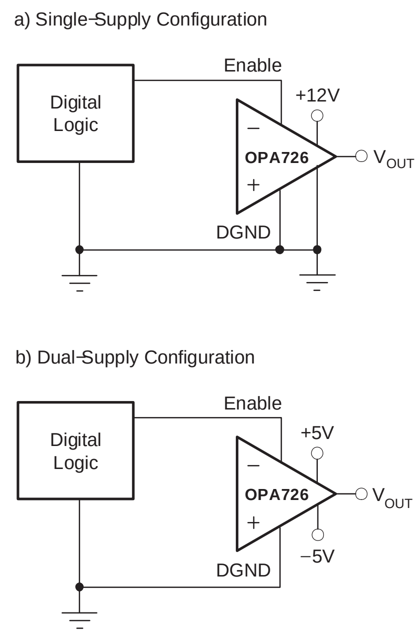


Figure 1. Enable Reference Pin Connection for Single- and Dual-Supply Configurations

INPUT OVER-VOLTAGE PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than approximately 300mV. Momentary voltages greater than 300mV beyond the power supply can be tolerated if the current is limited to 10mA. This is easily accomplished with an input resistor in series with the op amp, as shown in Figure 2. The OPA725 series features no phase inversion when the inputs extend beyond supplies, if the input is current limited.

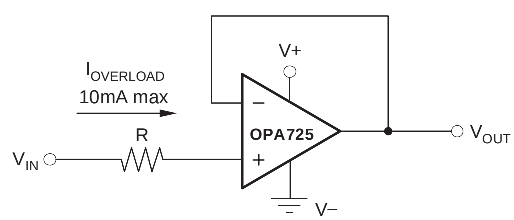


Figure 2. Input Current Protection for Voltages Exceeding the Supply Voltage

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving heavy loads connected to any point between V+ and V−. For light resistive loads (> 100kΩ), the output voltage can swing to 150mV (175mV for dual) from the supply rail, while still maintaining excellent linearity (A_{OL} > 110dB). With 1kΩ (2kΩ for dual) resistive loads, the output is specified to swing to within 250mV from the supply rails with excellent linearity (see the Typical Characteristics curve *Output Voltage Swing vs Output Current*).

CAPACITIVE LOAD AND STABILITY

Capacitive load drive is dependent upon gain and the overshoot requirements of the application. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads (see the Typical Characteristics curve *Small-Signal Overshoot vs Capacitive Load*).

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10Ω to 20Ω resistor inside the feedback loop, as shown in Figure 3. This reduces ringing with large capacitive loads while maintaining DC accuracy.

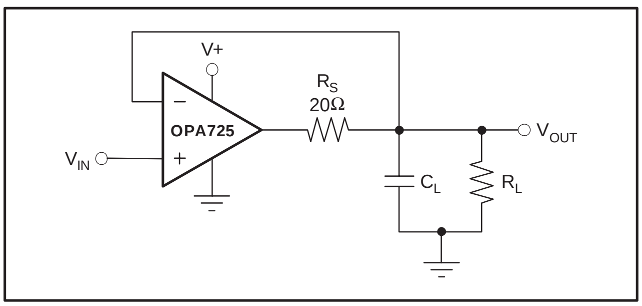


Figure 3. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive

DRIVING FAST 16-BIT ADCs

The OPA725 series is optimized for driving fast 16-bit ADCs such as the ADS8342. The OPA725 op amps buffer the converter input capacitance and resulting charge injection, while providing signal gain. Figure 4 shows the OPA725 in a single-ended method of interfacing to the ADS8342 16-bit, 250kSPS, 4-channel ADC with an input range of ±2.5V. The OPA725 has demonstrated excellent settling time to the 16-bit level within the 600ns acquisition time of the ADS8342. The RC filter, shown in Figure 4, has been carefully tuned for best noise and settling performance. It may need to be adjusted for different op amp configurations. Please refer to the ADS8342 data sheet (available for download at www.ti.com) for additional information on this product.

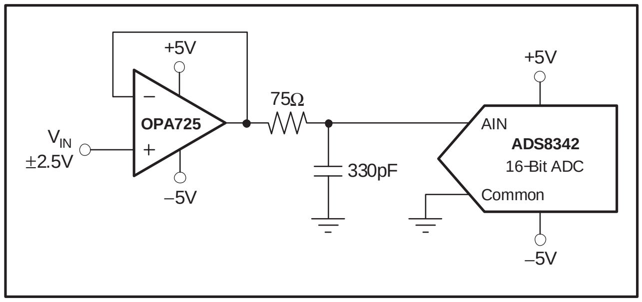
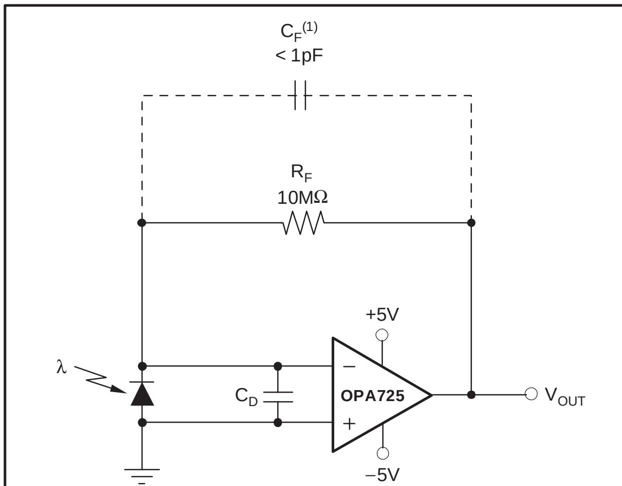


Figure 4. OPA725 Driving an ADC

TRANSIMPEDANCE AMPLIFIER

Wide bandwidth, low input bias current, and low input voltage and current noise make the OPA725 an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 5, are the expected diode capacitance (C_D), which should include the parasitic input common-mode and differential-mode input capacitance (4pF + 5pF for the OPA725); the desired transimpedance gain (R_F); and the GBW for the OPA725 (20MHz). With these three variables set, the feedback capacitor value (C_F) can be set to control the frequency response. C_F includes the stray capacitance of R_F, which is 0.2pF for a typical surface-mount resistor.



NOTE: (1) C_F is optional to prevent gain peaking. It includes the stray capacitance of R_F.

Figure 5. Dual-Supply Transimpedance Amplifier

To achieve a maximally-flat, 2nd-order Butterworth frequency response, the feedback pole should be set to:

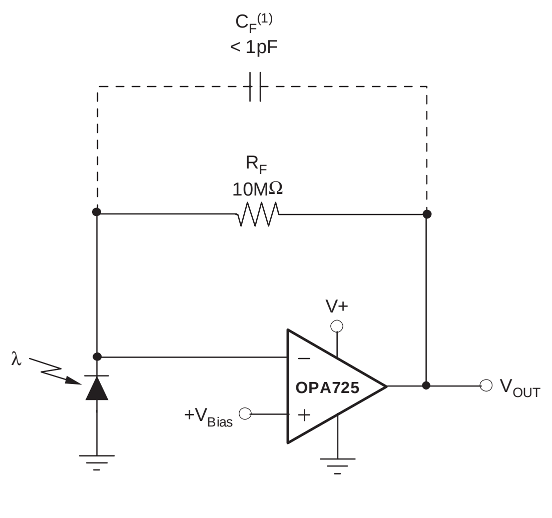
$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBW}{4\pi R_F C_D}} \qquad (1)$$

Bandwidth is calculated by:

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi R_F C_D}}\,Hz \qquad (2)$$

For even higher transimpedance bandwidth, the high-speed CMOS OPA354 (100MHz GBW), OPA300 (180 MHz GBW), OPA355 (200MHz GBW), or OPA656, OPA657 (400MHz GBW) may be used.

For single-supply applications, the +IN input can be biased with a positive dc voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail. (Refer to Figure 6.) This bias voltage also appears across the photodiode, providing a reverse bias for faster operation.



NOTE: (1) C_F is optional to prevent gain peaking. It includes the stray capacitance of R_F.

Figure 6. Single-Supply Transimpedance Amplifier

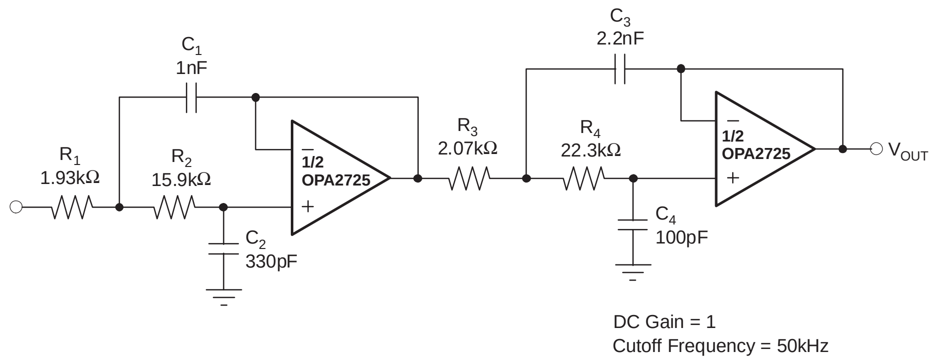
For additional information, refer to Application Bulletin SBOA055, *Compensate Transimpedance Amplifiers Intuitively*, available for download at www.ti.com.

OPTIMIZING THE TRANSIMPEDANCE CIRCUIT

To achieve the best performance, components should be selected according to the following guidelines:

1. For lowest noise, select R_F to create the total required gain. Using a lower value for R_F and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by R_F increases with the square-root of R_F, whereas the signal increases linearly. Therefore, signal-to-noise ratio is improved when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to be amplified (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce its capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the R_F to limit bandwidth, even if not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

For additional information, refer to the Application Bulletins *Noise Analysis of FET Transimpedance Amplifiers* (SBOA060), and *Noise Analysis for High-Speed Op Amps* (SBOA066), available for download at the TI web site.



NOTE: FilterPro is a low-pass filter design program available for download at no cost from TI's web site (www.ti.com). The program can be used to determine component values for other cutoff frequencies or filter types.

Figure 7. Four-Pole Butterworth Sallen-Key Low-Pass Filter

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
OPA2725AID	ACTIVE	SOIC	D	8	100	None	CU NIPDAU	Level-3-240C-168 HR
OPA2725AIDGKR	ACTIVE	MSOP	DGK	8	2500	None	CU NIPDAU	Level-1-240C-UNLIM
OPA2725AIDGKT	ACTIVE	MSOP	DGK	8	250	None	CU NIPDAU	Level-1-240C-UNLIM
OPA2725AIDR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-3-240C-168 HR
OPA2726AIDGSR	ACTIVE	MSOP	DGS	10	2500	None	CU NIPDAU	Level-1-240C-UNLIM
OPA2726AIDGST	ACTIVE	MSOP	DGS	10	250	None	CU NIPDAU	Level-1-240C-UNLIM
OPA725AID	ACTIVE	SOIC	D	8	100	None	CU NIPDAU	Level-3-240C-168 HR
OPA725AIDBVR	ACTIVE	SOT-23	DBV	5	3000	None	CU NIPDAU	Level-1-240C-UNLIM
OPA725AIDBVT	ACTIVE	SOT-23	DBV	5	250	None	CU NIPDAU	Level-1-240C-UNLIM
OPA725AIDR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-3-240C-168 HR
OPA726AID	ACTIVE	SOIC	D	8	100	None	CU NIPDAU	Level-3-240C-168 HR
OPA726AIDGKR	ACTIVE	MSOP	DGK	8	2500	None	CU NIPDAU	Level-2-240C-1 YEAR
OPA726AIDGKT	ACTIVE	MSOP	DGK	8	250	None	CU NIPDAU	Level-2-240C-1 YEAR
OPA726AIDR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-3-240C-168 HR

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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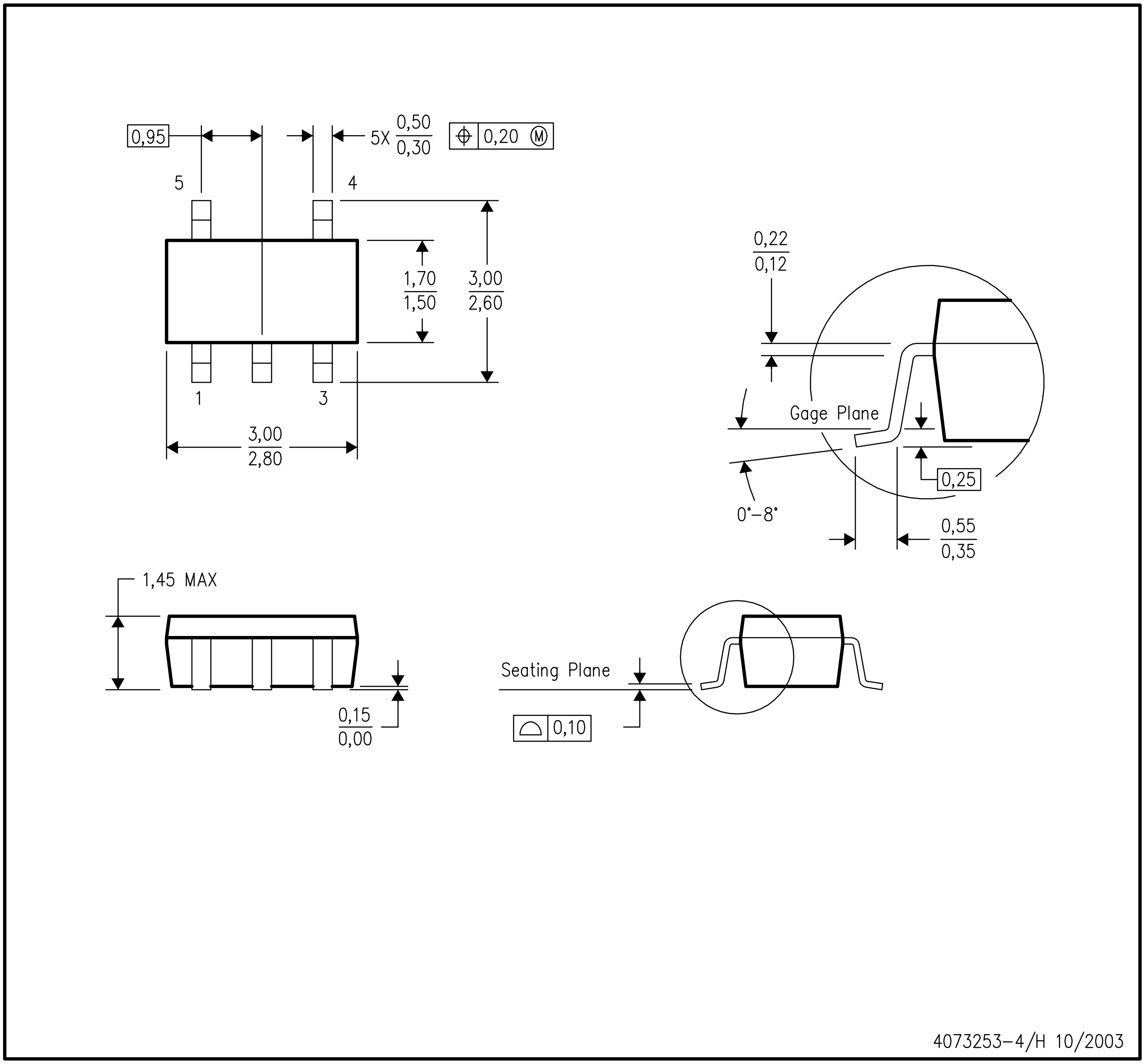
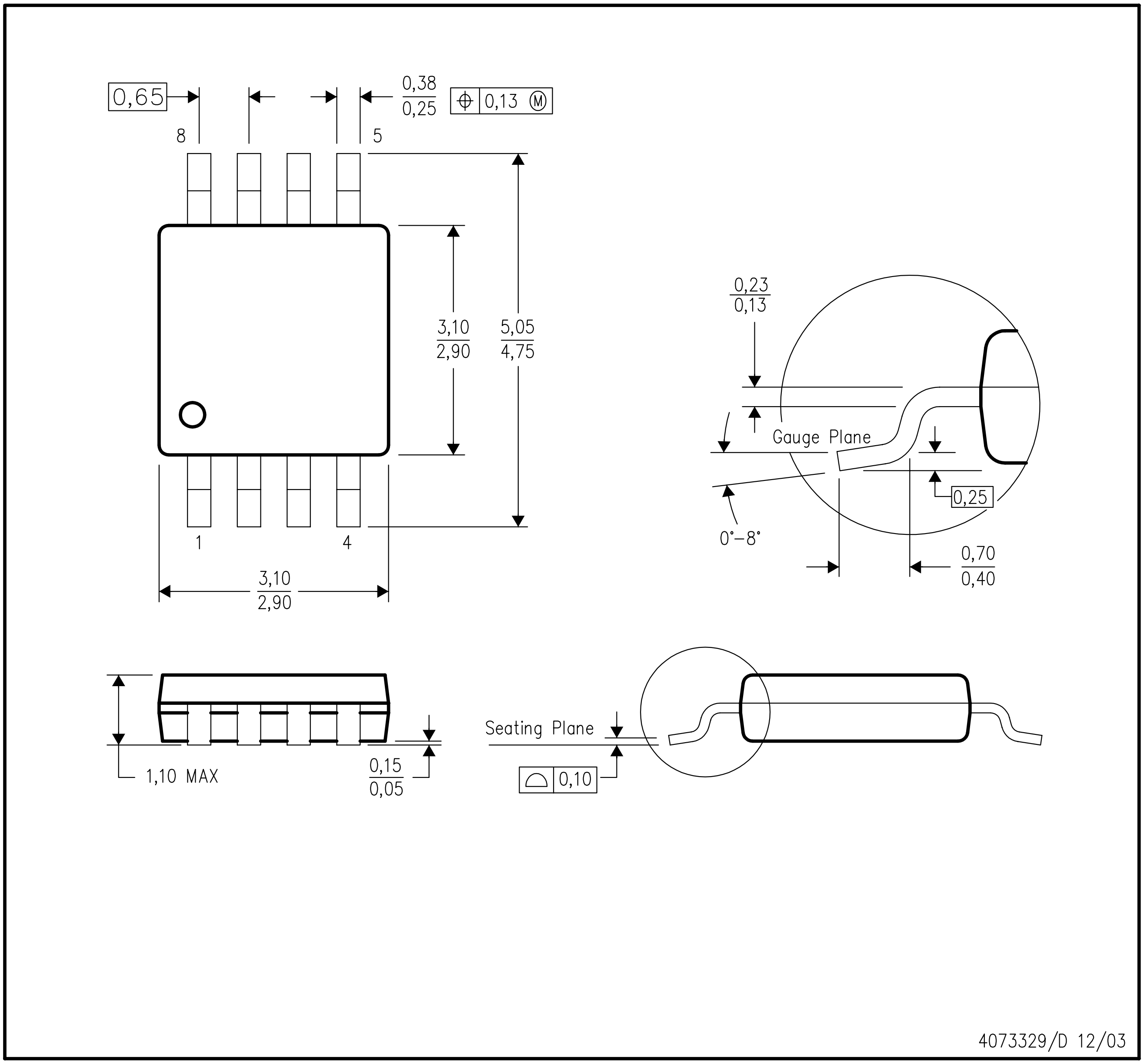
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



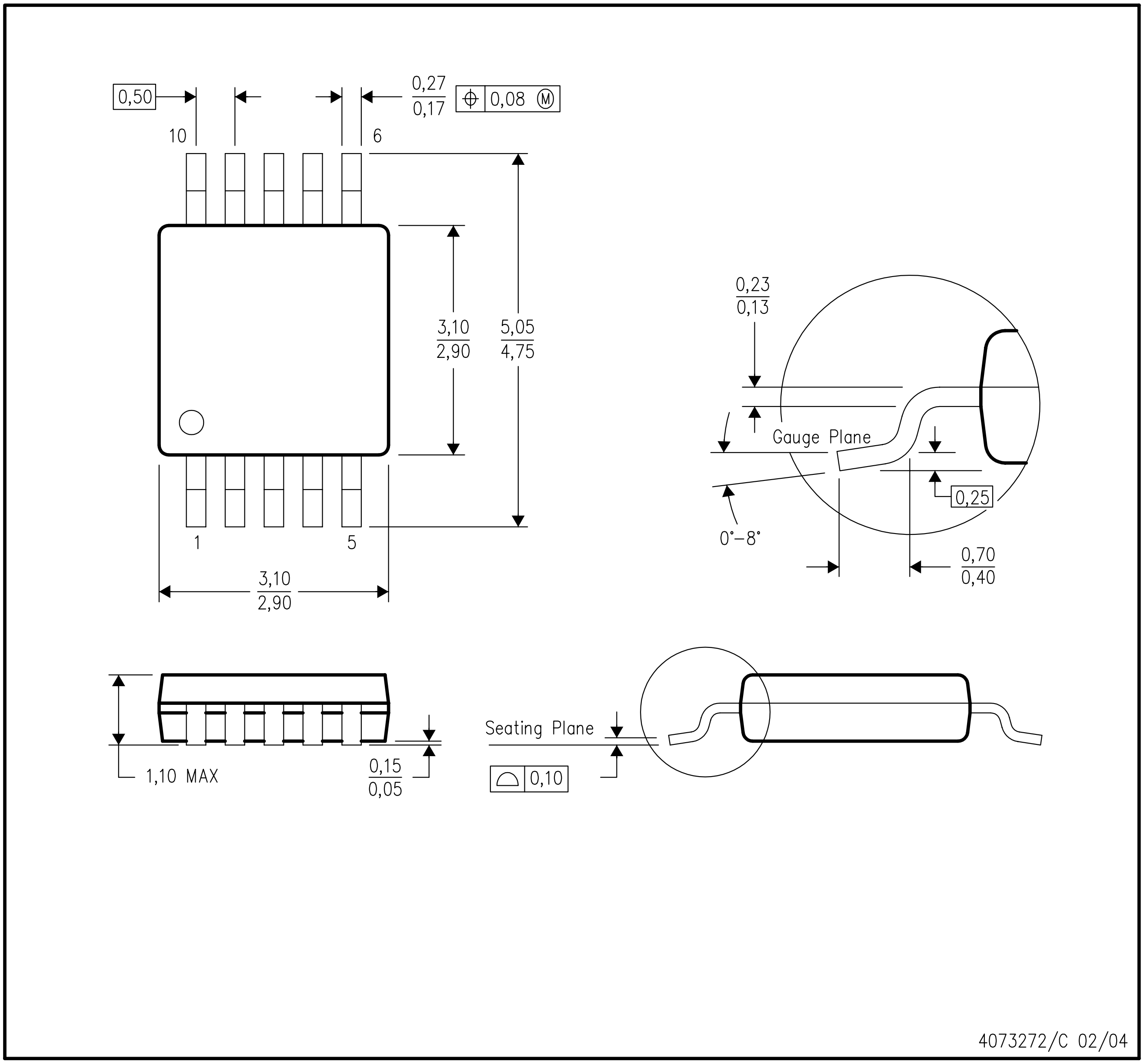
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-178 Variation AA.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



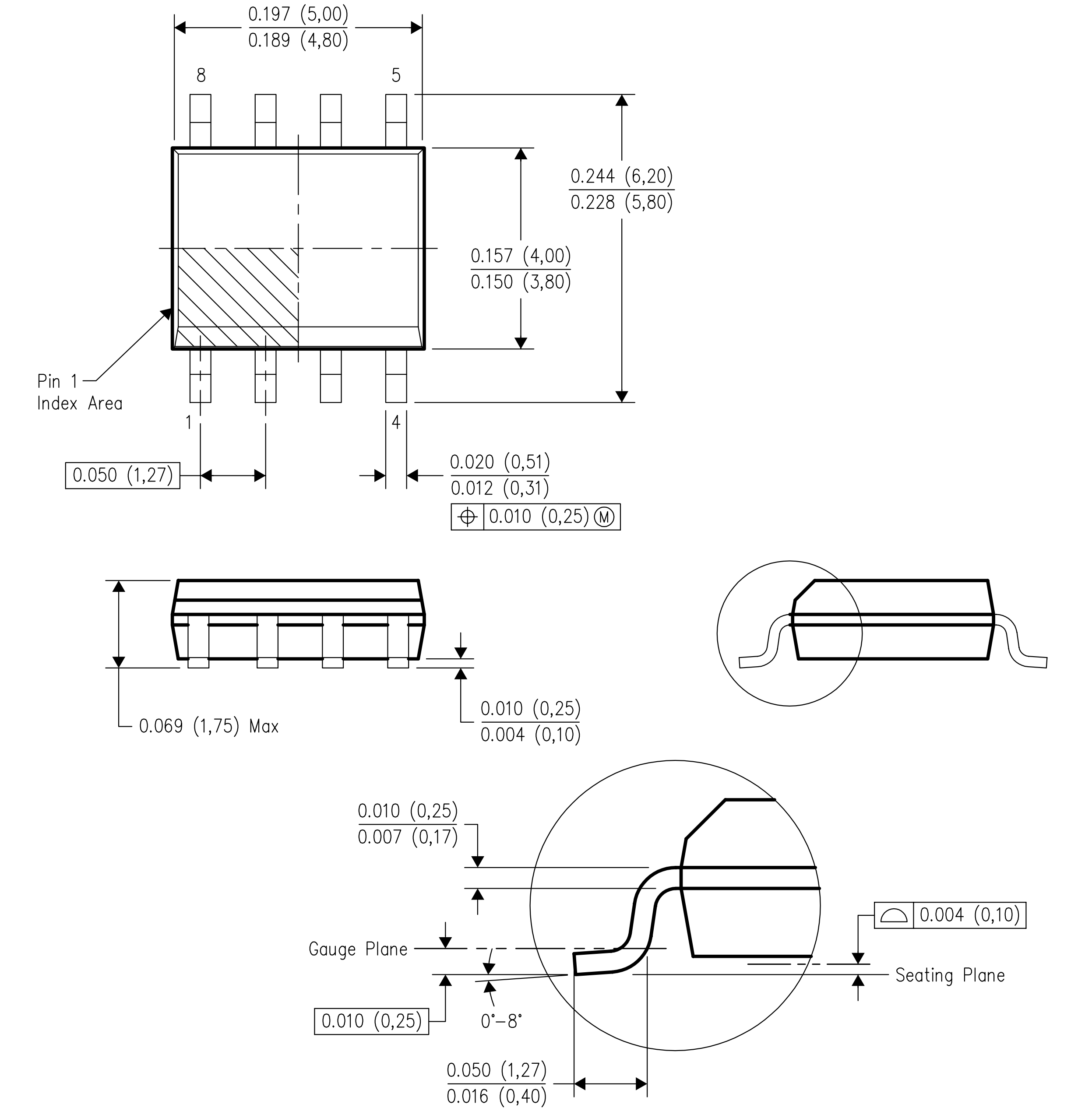
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation AA.

DGS (S-PDSO-G10) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation BA.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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