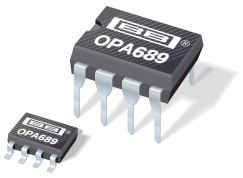
BURR-BROWN®



OPA689

For most current data sheet and other product information, visit www.burr-brown.com

Wideband, High Gain VOLTAGE LIMITING AMPLIFIER

FEATURES

- HIGH LINEARITY NEAR LIMITING
- FAST RECOVERY FROM OVERDRIVE: 2.4ns
- LIMITING VOLTAGE ACCURACY: ±15mV
- –3dB BANDWIDTH (G = +6): 280MHz
- STABLE FOR G ≥ +4
- SLEW RATE: 1600V/μs
- ±5V AND +5V SUPPLY OPERATION
- LOW GAIN VERSION: OPA688

APPLICATIONS

- TRANSIMPEDANCE WITH FAST OVERDRIVE RECOVERY
- FAST LIMITING ADC INPUT DRIVER
- LOW PROP DELAY COMPARATOR
- NON-LINEAR ANALOG SIGNAL PROCESSING
- DIFFERENCE AMPLIFIER
- IF LIMITING AMPLIFIER
- AM SIGNAL GENERATION

DESCRIPTION

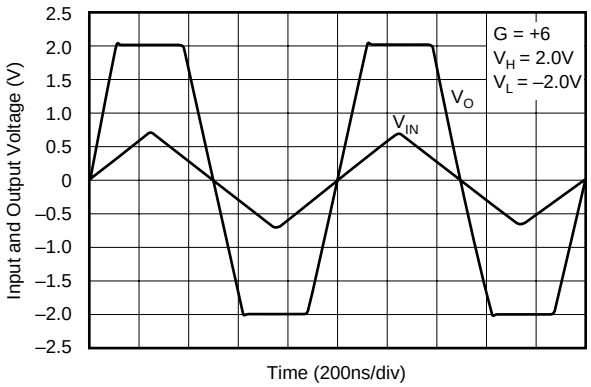
The OPA689 is a wideband, voltage feedback op amp that offers bipolar output voltage limiting, and is stable for gains ≥ +4. Two buffered limiting voltages take control of the output when it attempts to drive beyond these limits. This new output limiting architecture holds the limiter offset error to ±15mV. The op amp operates linearly to within 30mV of the limits.

The combination of narrow nonlinear range and low limiting offset allows the limiting voltages to be set within 100mV of the desired linear output range. A fast 2.4ns recovery from limiting ensures that overdrive signals will be transparent to the signal channel. Implementing the limiting function at the output, as opposed to the input, gives the specified limiting accuracy for any gain, and allows the OPA689 to be used in all standard op amp applications.

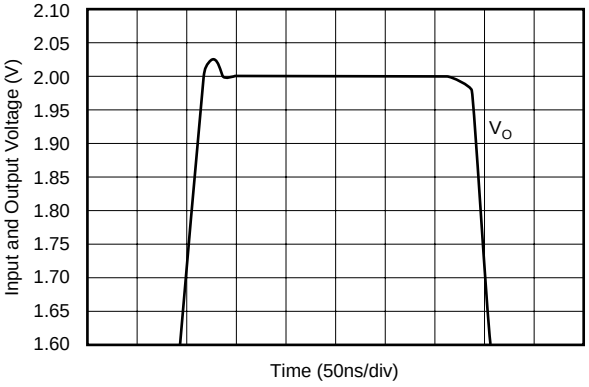
Non-linear analog signal processing circuits will benefit from the OPA689's sharp transition from linear operation to output limiting. The quick recovery time supports high speed applications.

The OPA689 is available in an industry-standard pinout in PDIP-8 and SO-8 packages. For lower gain applications requiring output limiting with fast recovery, consider the OPA688.

LIMITED OUTPUT RESPONSE



DETAIL OF LIMITED OUTPUT VOLTAGE



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS — V_S = ±5V

G = +6, R_L = 500Ω, R_F = 750Ω, V_H = $-V_L$ = 2V, (Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA689U, P TYP +25°C	GUARANTEED[1] +25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ MAX	TEST LEVEL[2]
AC PERFORMANCE (see Fig. 1)								
Small Signal Bandwidth	V_O < 0.5Vp-p							
	G = +6	280	220	210	200	MHz	Min	B
	G = +12	90	—	—	—	MHz	Typ	C
	G = –6	220	—	—	—	MHz	Typ	C
Gain Bandwidth Product (G ≥ +20)	V_O < 0.5Vp-p	720	490	460	430	MHz	Min	B
Gain Peaking	V_O < 0.5Vp-p, G = +4	8	—	—	—	dB	Typ	C
0.1dB Gain Flatness Bandwidth	V_O < 0.5Vp-p	110	—	—	—	MHz	Typ	C
Large Signal Bandwidth	V_O = 2Vp-p	290	185	175	170	MHz	Min	B
Step Response								
Slew Rate	2V Step	1600	1300	1250	950	V/µs	Min	B
Rise/Fall Time	0.5V Step	1.2	1.8	1.9	2.4	ns	Max	B
Settling Time: 0.05%	2V Step	7	—	—	—	ns	Typ	C
Spurious Free Dynamic Range	f = 5MHz, V_O = 2Vp-p	61	57	53	48	dB	Min	B
Differential Gain	NTSC, PAL, R_L = 500Ω	0.02	—	—	—	%	Typ	C
Differential Phase	NTSC, PAL, R_L = 500Ω	0.01	—	—	—	°	Typ	C
Input Noise Density								
Voltage Noise	f ≥ 1MHz	4.6	5.3	6.0	6.1	nV/√Hz	Max	B
Current Noise	f ≥ 1MHz	2.0	2.5	2.9	3.6	pA/√Hz	Max	B
DC PERFORMANCE (V_{CM} = 0V)								
Open-Loop Voltage Gain (A_{OL})	V_O = ±0.5V	56	**50**	48	47	dB	Min	A
Input Offset Voltage		±1	**±5**	±6	±7	mV	Max	A
Average Drift		—	—	±14	±14	µV/°C	Max	B
Input Bias Current[3]		+8	**±12**	±13	±20	µA	Max	A
Average Drift		—	—	–60	–90	nA/°C	Max	B
Input Offset Current		±0.3	**±2**	±3	±4	µA	Max	A
Average Drift		—	—	±10	±10	nA/°C	Max	B
INPUT								
Common-Mode Rejection Ratio	Input Referred, V_{CM} = ±0.5V	60	**53**	52	50	dB	Min	A
Common-Mode Input Range[4]		±3.3	±3.2	±3.2	±3.1	V	Min	A
Input Impedance								
Differential-Mode		0.4 || 1	—	—	—	MΩ || pF	Typ	C
Common-Mode		1 || 1	—	—	—	MΩ || pF	Typ	C
OUTPUT	V_H = $-V_L$ = 4.3V							
Output Voltage Range	R_L ≥ 500Ω	±4.1	**±3.9**	±3.9	±3.8	V	Min	A
Current Output, Sourcing		105	**90**	85	80	mA	Min	A
Sinking		–85	**–70**	–65	–60	mA	Min	A
Closed-Loop Output Impedance	G = +4, f < 100kHz	0.8	—	—	—	Ω	Typ	C
POWER SUPPLY								
Operating Voltage, Specified		±5	—	—	—	V	Typ	C
Maximum		—	**±6**	±6	±6	V	Max	A
Quiescent Current, Maximum		15.8	**17**	19	20	mA	Max	A
Minimum		15.8	**14**	12.8	11	mA	Min	A
Power Supply Rejection Ratio	$+V_S$ = 4.5V to 5.5V							
+PSR (Input Referred)		65	**58**	57	55	dB	Min	A
OUTPUT VOLTAGE LIMITERS								
Default Limit Voltage	Limiter Pins Open	±3.3	**±3.0**	±3.0	±2.9	V	Min	A
Minimum Limiter Separation (V_H – V_L)		200	200	200	200	mV	Min	B
Maximum Limit Voltage		—	±4.3	±4.3	±4.3	V	Max	B
Limiter Input Bias Current Magnitude[5]	V_O = 0							
Maximum		54	**65**	68	70	µA	Max	A
Minimum		54	**35**	34	31	µA	Min	A
Average Drift		—	—	40	45	nA/°C	Max	B
Limiter Input Impedance		2 || 1	—	—	—	MΩ || pF	Typ	C
Limiter Feedthrough[6]	f = 5MHz	–60	—	—	—	dB	Typ	C
DC Performance in Limit Mode	V_{IN} = ±0.7V							
Limiter Offset Voltage	(V_O – V_H) or (V_O – V_L)	±15	**±35**	±40	±40	mV	Max	A
Op Amp Input Bias Current Shift[3]		3	—	—	—	µA	Typ	C

SPECIFICATIONS — V_S = ±5V (cont.)

G = +6, R_L = 500Ω, R_F = 750Ω, V_H = –V_L = 2V, (Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA689U, P						TEST LEVEL[2]
		TYP	GUARANTEED[1]					
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ MAX	
OUTPUT VOLTAGE LIMITERS (CONT)								
AC Performance in Limit Mode								
Limiter Small Signal Bandwidth	V_{IN} = ±0.7V, V_O < 0.02Vp-p	450	—	—	—	MHz	Typ	C
Limiter Slew Rate[7]		100	—	—	—	V/µs	Typ	C
Limited Step Response								
Overshoot	V_{IN} = 0 to ±0.7V Step	250	—	—	—	mV	Typ	C
Recovery Time	V_{IN} = ±0.7V to 0 Step	2.4	2.8	3.0	3.2	ns	Max	B
Linearity Guardband[8]	f = 5MHz, V_O = 2Vp-p	30	—	—	—	mV	Typ	C
THERMAL CHARACTERISTICS								
Temperature Range	Specification: P, U	–40 to +85	—	—	—	°C	Typ	C
Thermal Resistance								
P 8-Pin DIP		100	—	—	—	°C/W	Typ	C
U 8-Pin SO-8		125	—	—	—	°C/W	Typ	C

NOTES: (1) Junction Temperature = Ambient Temperature for low temperature limit and 25°C guaranteed specifications. Junction Temperature = Ambient Temperature + 23°C at high temperature limit guaranteed specifications. (2) TEST LEVELS: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value for information only. (3) Current is considered positive out of node. (4) CMIR tested as < 3dB degradation from minimum CMRR at specified limits. (5) I_{VH} (V_H bias current) is positive, and I_{VL} (V_L bias current) is negative, under these conditions. See Note 3 and Figures 1 and 7. (6) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0. (7) V_H slew rate conditions are: V_{IN} = +0.7V, G = +6, V_L = –2V, V_H = step between 2V and 0V. V_L slew rate conditions are similar. (8) Linearity Guardband is defined for an output sinusoid (f = 1MHz, V_O = 2Vpp) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 8).

SPECIFICATIONS — V_S = +5V

G = +6, R_F = 750Ω, R_L = 500Ω tied to V_{CM} = 2.5V, V_L = V_{CM} –1.2V, V_H = V_{CM} +1.2V, (Figure 2 for AC performance only), unless otherwise noted.

		OPA689U, P						
		TYP	GUARANTEED[1]					
PARAMETER	CONDITIONS	+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ MAX	TEST LEVEL[2]
AC PERFORMANCE (see Fig. 2)								
Small Signal Bandwidth	V_O < 0.5Vp-p							
	G = +6	210	180	160	150	MHz	Min	B
	G = +12	70	—	—	—	MHz	Typ	C
	G = –6	180	—	—	—	MHz	Typ	C
Gain Bandwidth Product (G ≥ +20)	V_O < 0.5Vp-p	440	330	310	300	MHz	Min	B
Gain Peaking	V_O < 0.5Vp-p, G = +4	4	—	—	—	dB	Typ	B
0.1dB Gain Flatness Bandwidth	V_O < 0.5Vp-p	35	—	—	—	MHz	Typ	C
Large Signal Bandwidth	V_O = 2Vp-p	175	150	140	125	MHz	Min	B
Step Response								
Slew Rate	2V Step	1600	1300	1250	950	V/µs	Min	B
Rise/Fall Time	0.5V Step	1.9	2.1	2.2	2.6	ns	Max	B
Settling Time: 0.05%	2V Step	7	—	—	—	ns	Typ	C
Spurious Free Dynamic Range	f = 5MHz, V_O = 2Vp-p	59	55	51	46	dB	Min	B
Input Noise								
Voltage Noise Density	f ≥ 1MHz	4.6	5.3	6.0	6.1	nV/√Hz	Max	B
Current Noise Density	f ≥ 1MHz	2.0	2.5	2.9	3.6	pA/√Hz	Max	B
DC PERFORMANCE								
Open-Loop Voltage Gain (A_{OL})	V_O = ±0.5V	56	**50**	48	47	dB	Min	A
Input Offset Voltage		±1	**±5**	±6	±8	mV	Max	A
Average Drift		—	—	±14	±14	µV/°C	Max	B
Input Bias Current[3]		+8	**±12**	±13	±20	µA	Max	A
Average Drift		—	—	–60	–90	nA/°C	Max	B
Input Offset Current		±0.3	**±2**	±3	±4	µA	Max	A
Average Drift		—	—	±10	±10	nA/°C	Max	B
INPUT								
Common-Mode Rejection Ratio	Input Referred, V_{CM} ±0.5V	58	**51**	50	48	dB	Min	A
Common-Mode Input Range[4]		V_{CM} ±0.8	V_{CM} ±0.7	V_{CM} ±0.7	V_{CM} ±0.6	V	Min	A
Input Impedance								
Differential-Mode		0.4 || 1	—	—	—	MΩ || pF	Typ	C
Common-Mode		1 || 1	—	—	—	MΩ || pF	Typ	C
OUTPUT	V_H = V_{CM} + 1.8V, V_L = V_{CM} – 1.8V							
Output Voltage Range	R_L ≥ 500Ω	V_{CM} ±1.6	**V_{CM} ±1.4**	V_{CM} ±1.4	V_{CM} ±1.3	V	Min	A
Current Output, Sourcing		70	**60**	55	50	mA	Min	A
Sinking		–60	**–50**	–45	–40	mA	Min	A
Closed-Loop Output Impedance	G = +4, f < 100kHz	0.8	—	—	—	Ω	Typ	C
POWER SUPPLY								
Operating Voltage, Specified		5	—	—	—	V	Typ	C
Maximum		—	12	12	12	V	Max	A
Quiescent Current, Maximum		13	**15**	15	16	mA	Max	A
Minimum		13	**11**	10	9	mA	Min	A
Power Supply Rejection Ratio	V_S = 4.5V to 5.5V							
+PSR (Input Referred)		65	—	—	—	dB	Typ	C
OUTPUT VOLTAGE LIMITERS								
Default Limiter Voltage	Limiter Pins Open	V_{CM} ±0.9	**V_{CM} ±0.6**	V_{CM} ±0.6	V_{CM} ±0.6	V	Min	A
Minimum Limiter Separation (V_H – V_L)		200	200	200	200	mV	Min	B
Maximum Limit Voltage		—	V_{CM} ±1.8	V_{CM} ±1.8	V_{CM} ±1.8	V	Max	B
Limiter Input Bias Current Magnitude[5]	V_O = 2.5V							
Maximum		35	**65**	75	85	µA	Max	A
Minimum		35	**0**	0	0	µA	Min	A
Average Drift		—	—	30	50	nA/°C	Max	B
Limiter Input Impedance		2 || 1	—	—	—	MΩ || pF	Typ	C
Limiter Isolation[6]	f = 5MHz	–60	—	—	—	dB	Typ	C
DC Performance in Limit Mode	V_{IN} = V_{CM} ±0.4V							
Limiter Voltage Accuracy	(V_O – V_H) or (V_O – V_L)	±15	**±35**	±40	±40	mV	Max	A
Op Amp Bias Current Shift[3]		5	—	—	—	µA	Typ	C
AC Performance in Limit Mode								
Limiter Small Signal Bandwidth	V_{IN} = ±0.4V, V_O < 0.02Vp-p	300	—	—	—	MHz	Typ	C
Limiter Slew Rate[7]		20	—	—	—	V/µs	Typ	C
Limited Step Response								
Overshoot	V_{IN} = V_{CM} to V_{CM} ±0.4V Step	55	—	—	—	mV	Typ	C
Recovery Time	V_{IN} = V_{CM} ±0.4V to V_{CM} Step	15	—	—	—	ns	Typ	C
Linearity Guardband[8]	f = 5MHz, V_O = 2Vp-p	30	—	—	—	mV	Typ	C

SPECIFICATIONS — V_S = +5V (cont.)

G = +6, R_F = 750Ω, R_L = 500Ω tied to V_{CM} = 2.5V, V_L = V_{CM} –1.2V, V_H = V_{CM} +1.2V, (Figure 2 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA689U, P						
		TYP	GUARANTEED[1]					
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ MAX	TEST LEVEL[2]
THERMAL CHARACTERISTICS								
Temperature Range	Specification: P, U	–40 to +85	—	—	—	°C	Typ	C
Thermal Resistance								
P 8-Pin DIP		100	—	—	—	°C/W	Typ	C
U 8-Pin SO-8		125	—	—	—	°C/W	Typ	C

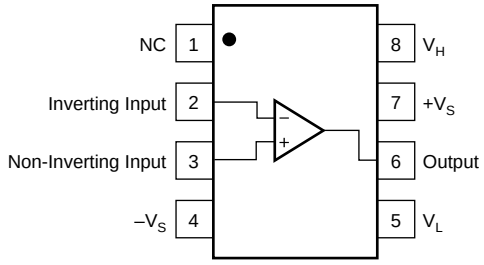
NOTES: (1) Junction Temperature = Ambient Temperature for low temperature limit and 25°C guaranteed specifications. Junction Temperature = Ambient Temperature + 23°C at high temperature limit guaranteed specifications. (2) TEST LEVELS: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value for information only. (3) Current is considered positive out of node. (4) CMIR tested as < 3dB degradation from minimum CMRR at specified limits. (5) I_{VH} (V_H bias current) is negative, and I_{VL} (V_L bias current) is positive, under these conditions. See Note 3 and Figures 2 and 7. (6) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0. (7) V_H slew rate conditions are: V_{IN} = V_{CM} +0.4V, G = +6, V_L = V_{CM} –1.2V, V_H = step between V_{CM} +1.2V and V_{CM}. V_L slew rate conditions are similar. (8) Linearity Guardband is defined for an output sinusoid (f = 5MHz, V_O = V_{CM} ±1Vp-p) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 8).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±6.5V
Internal Power Dissipation	See Thermal Characteristics
Input Voltage Range	±V_S
Differential Input Voltage	±V_S
Limiter Voltage Range	±(V_S – 0.7V)
Storage Temperature Range: P, U	–40°C to +125°C
Lead Temperature (DIP, soldering, 10s)	+300°C
(SO-8, soldering, 3s)	+260°C
Junction Temperature	+175°C

ABSOLUTE MAXIMUM RATINGS

Top View **DIP-8, SO-8**



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

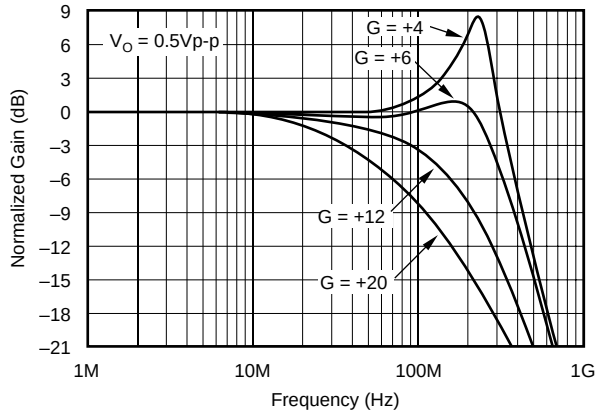
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
OPA689P	DIP-8	006	–40°C to +85°C	OPA689P	OPA689P	Rails
OPA689U	SO-8 Surface Mount	182	–40°C to +85°C	OPA689U	OPA689U	Rails
"	"	"	"	"	OPA689U/2K5	Tape and Reel

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "OPA689U/2K5" will get a single 2500-piece Tape and Reel.

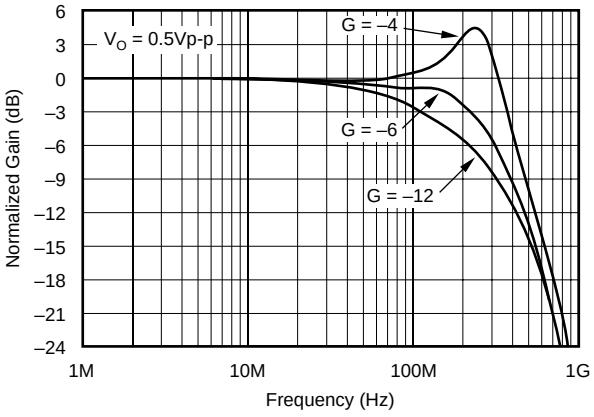
TYPICAL PERFORMANCE CURVES— $V_S = \pm 5V$

G = +6, R_L = 500Ω, R_F = 750Ω, $V_H = -V_L$ = 2V, (Figure 1 for AC performance only), unless otherwise noted.

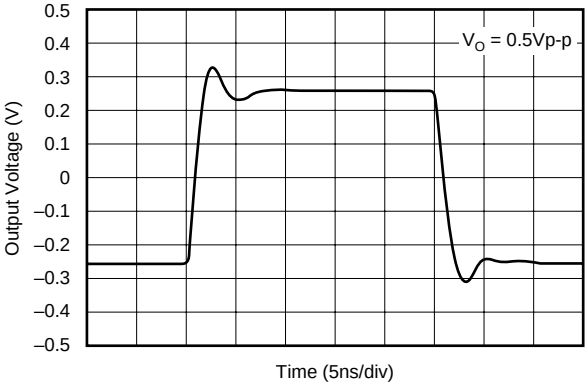
NON-INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



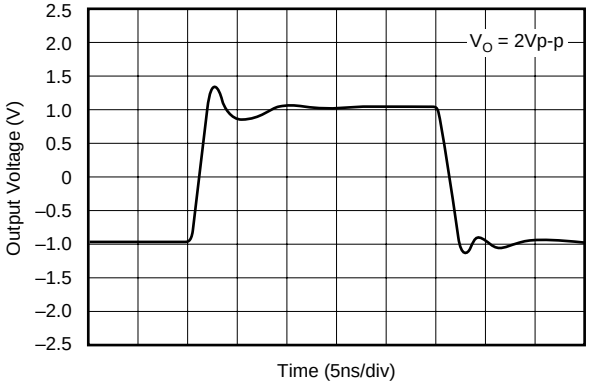
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



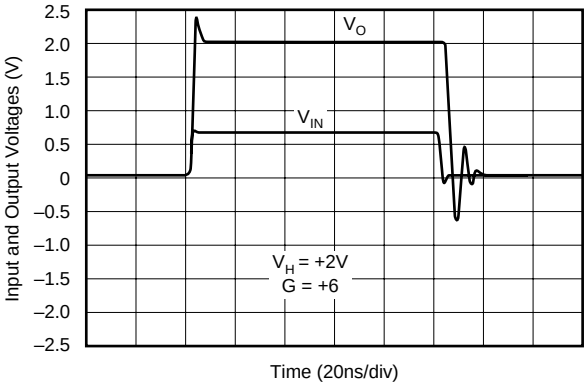
SMALL-SIGNAL PULSE RESPONSE



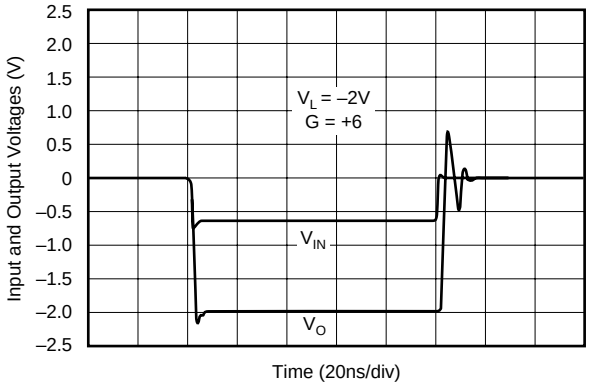
LARGE-SIGNAL PULSE RESPONSE



V_H—LIMITED PULSE RESPONSE



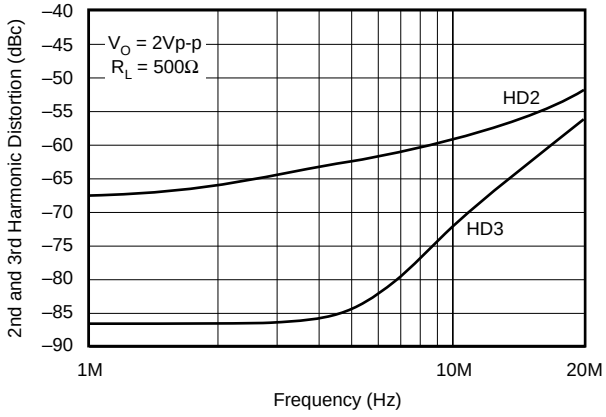
V_L—LIMITED PULSE RESPONSE



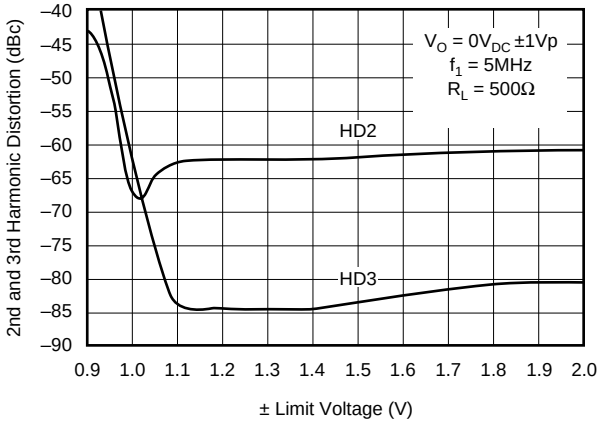
TYPICAL PERFORMANCE CURVES— V_S = ±5V (cont.)

G = +6, R_L = 500Ω, R_F = 750Ω, V_H = –V_L = 2V, (Figure 1 for AC performance only), unless otherwise noted.

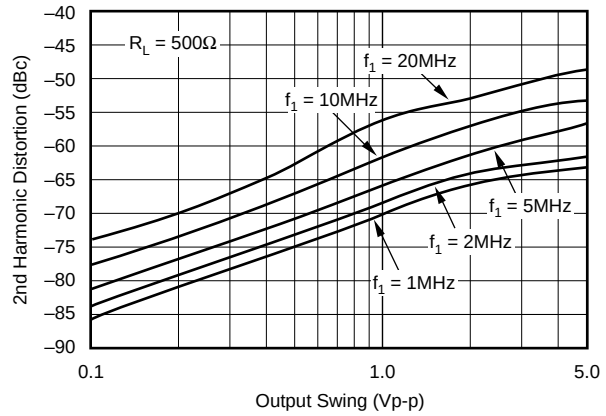
HARMONIC DISTORTION vs FREQUENCY



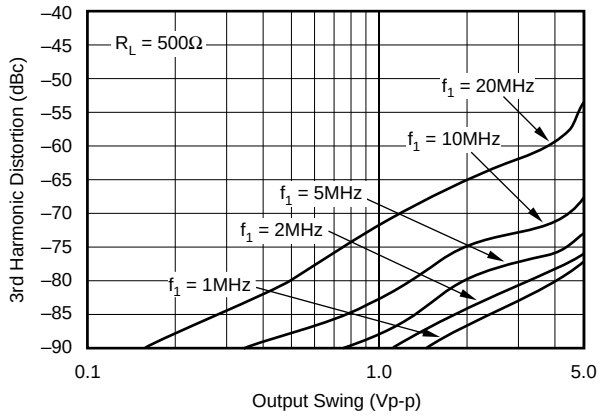
HARMONIC DISTORTION NEAR LIMIT VOLTAGES



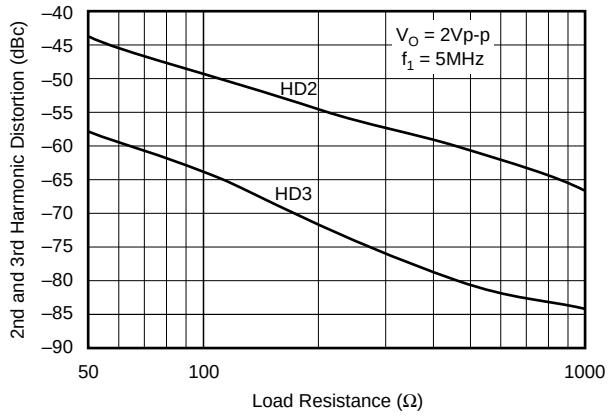
2ND HARMONIC DISTORTION vs OUTPUT SWING



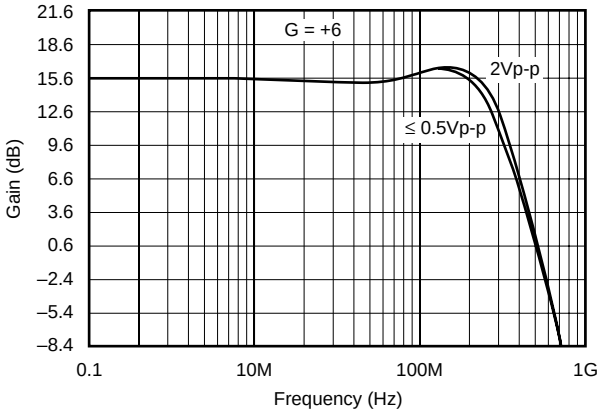
3RD HARMONIC DISTORTION vs OUTPUT SWING



HARMONIC DISTORTION vs LOAD RESISTANCE



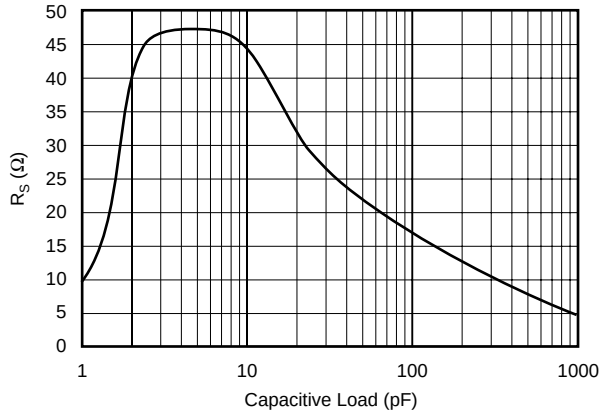
LARGE SIGNAL FREQUENCY RESPONSE



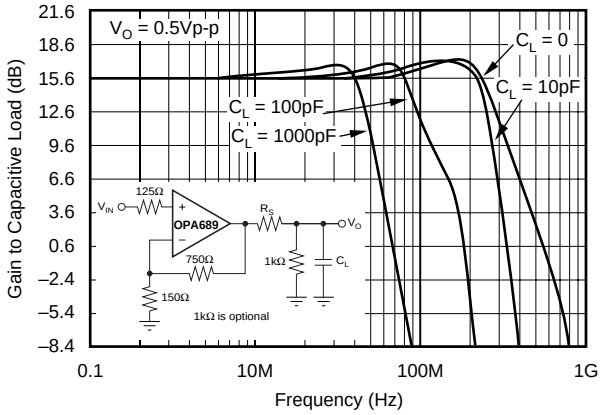
TYPICAL PERFORMANCE CURVES— V_S = ±5V (cont.)

G = +6, R_L = 500Ω, R_F = 750Ω, V_H = –V_L = 2V, (Figure 1 for AC performance only), unless otherwise noted.

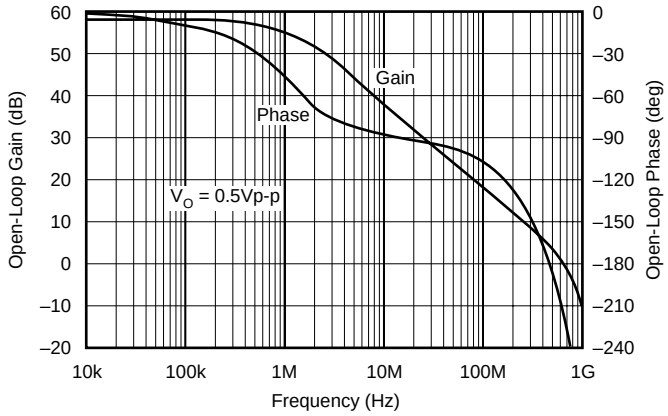
R_S vs CAPACITIVE LOAD



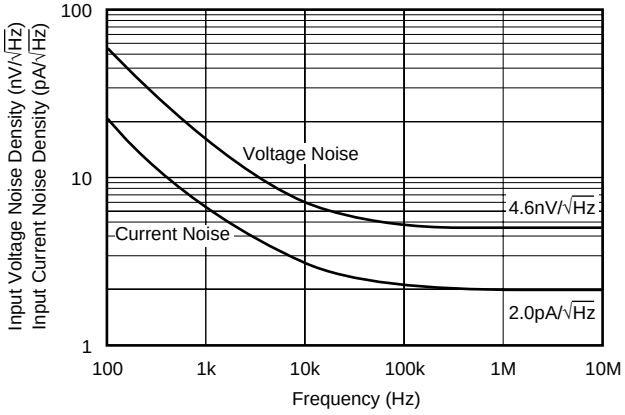
FREQUENCY RESPONSE vs CAPACITIVE LOAD



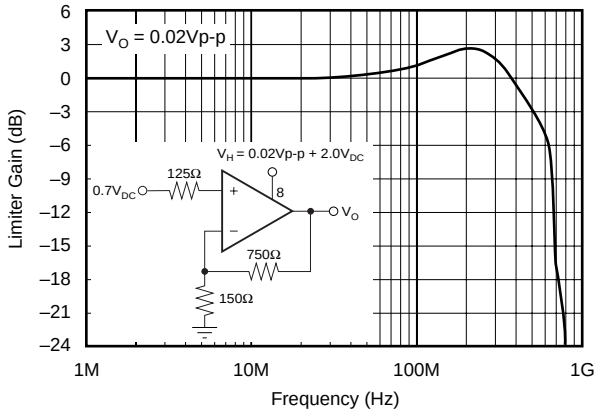
OPEN-LOOP FREQUENCY RESPONSE



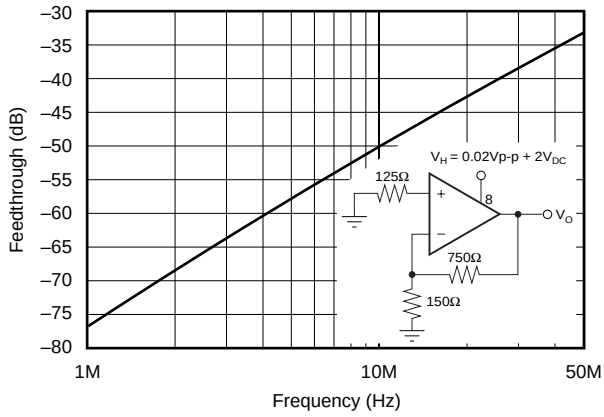
INPUT NOISE DENSITY



LIMITER SMALL-SIGNAL FREQUENCY RESPONSE



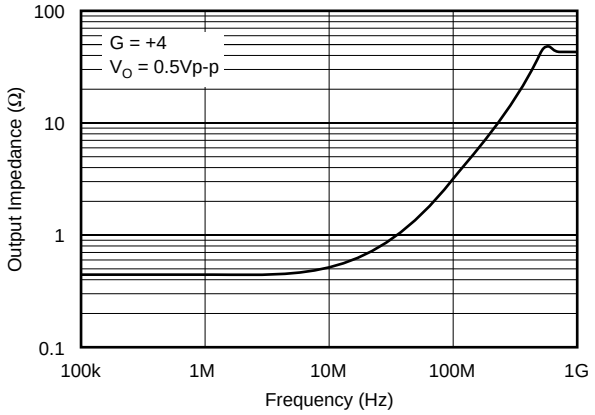
LIMITER FEEDTHROUGH



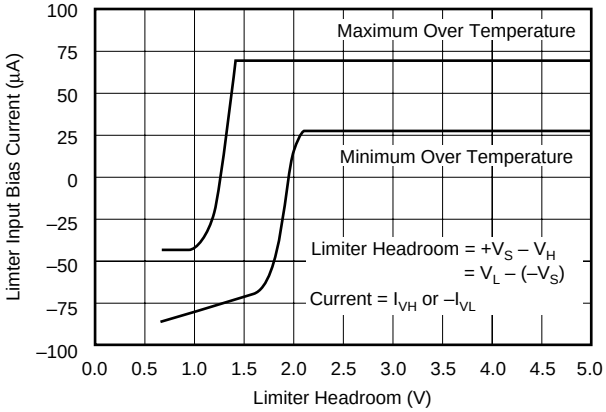
TYPICAL PERFORMANCE CURVES— V_S = ±5V (cont.)

G = +6, R_L = 500Ω, R_F = 750Ω, V_H = –V_L = 2V, (Figure 1 for AC performance only), unless otherwise noted.

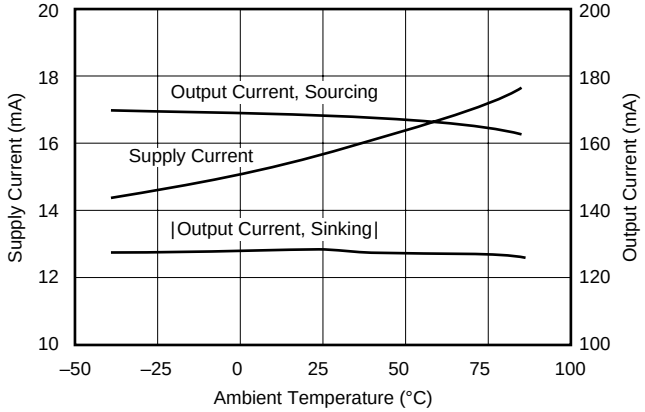
CLOSED-LOOP OUTPUT IMPEDANCE



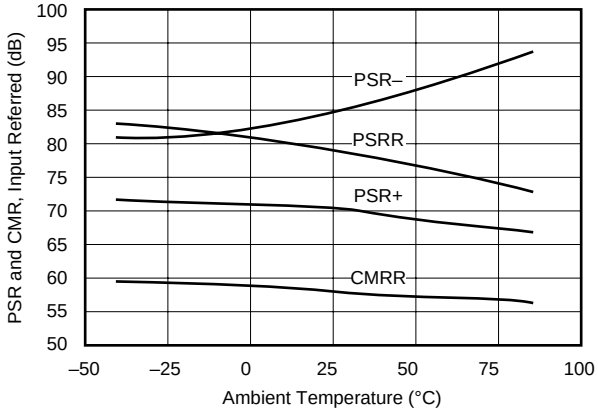
LIMITER INPUT BIAS CURRENT vs BIAS VOLTAGE



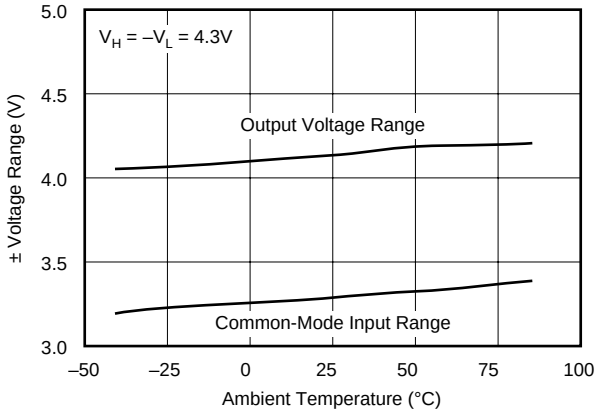
SUPPLY AND OUTPUT CURRENTS vs TEMPERATURE



PSR AND CMR vs TEMPERATURE



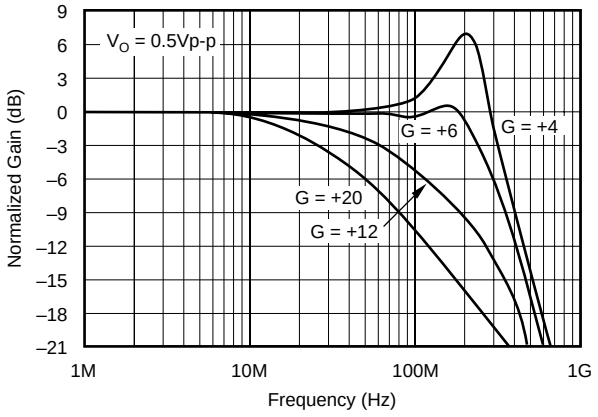
VOLTAGE RANGES vs TEMPERATURE



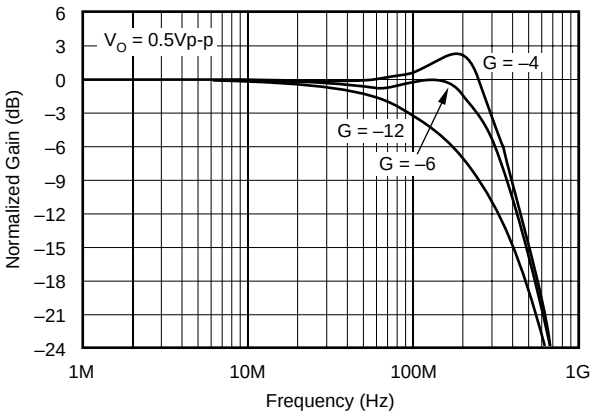
TYPICAL PERFORMANCE CURVES— V_S = +5V

G = +6, R_F = 402Ω, R_L = 500Ω tied to V_{CM} = 2.5V, $V_L = V_{CM}$ –1.2V, $V_H = V_{CM}$ +1.2V, (Figure 2 for AC performance only), unless otherwise noted.

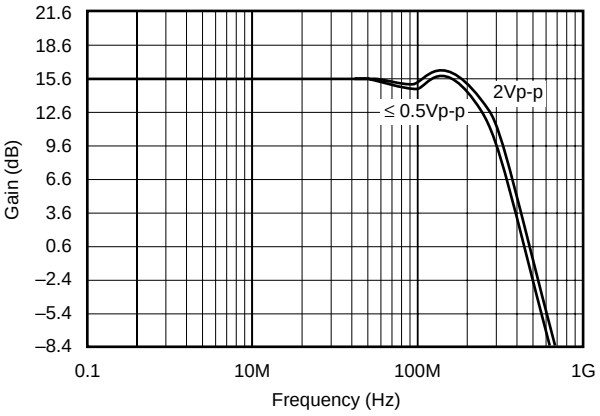
NON-INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



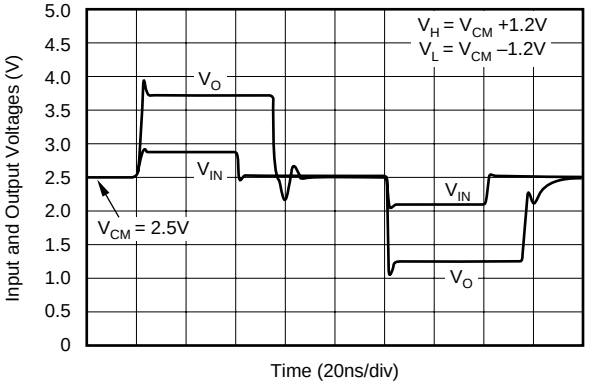
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



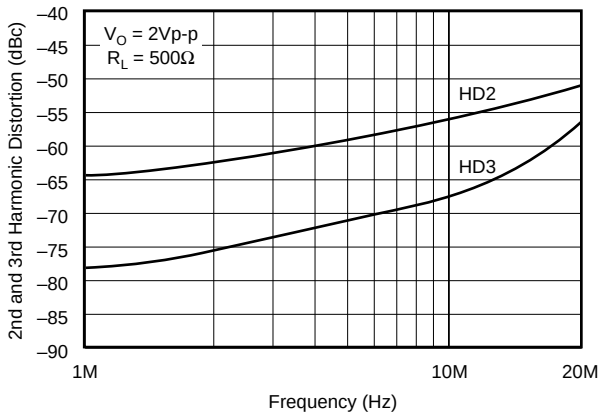
LARGE-SIGNAL FREQUENCY RESPONSE



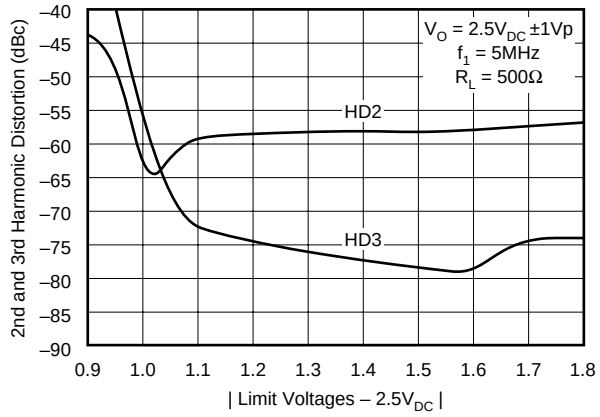
V_H AND V_H—LIMITED PULSE RESPONSE



HARMONIC DISTORTION vs FREQUENCY



HARMONIC DISTORTION NEAR LIMIT VOLTAGES



TYPICAL APPLICATIONS

DUAL SUPPLY, NON-INVERTING AMPLIFIER

Figure 1 shows a non-inverting gain amplifier for dual supply operation. This circuit was used for AC characterization of the OPA689, with a 50Ω source, which it matches, and a 500Ω load. The power supply bypass capacitors are shown explicitly in Figures 1 and 2, but will be assumed in the other figures. The limiter voltages (V_H and V_L) and their bias currents (I_{VH} and I_{VL}) have the polarities shown.

SINGLE SUPPLY, NON-INVERTING AMPLIFIER

Figure 2 shows an AC coupled, non-inverting gain amplifier for single supply operation. This circuit was used for AC characterization of the OPA689, with a 50Ω source, which it matches, and a 500Ω load. The power supply bypass capacitors are shown explicitly in Figures 1 and 2, but will be assumed in the other figures. The limiter voltages (V_H and V_L) and their bias currents (I_{VH} and I_{VL}) have the polarities shown. Notice that the single supply circuit can use 3 resistors to set V_H and V_L, where the dual supply circuit usually uses 4 to reference the limit voltages to ground.

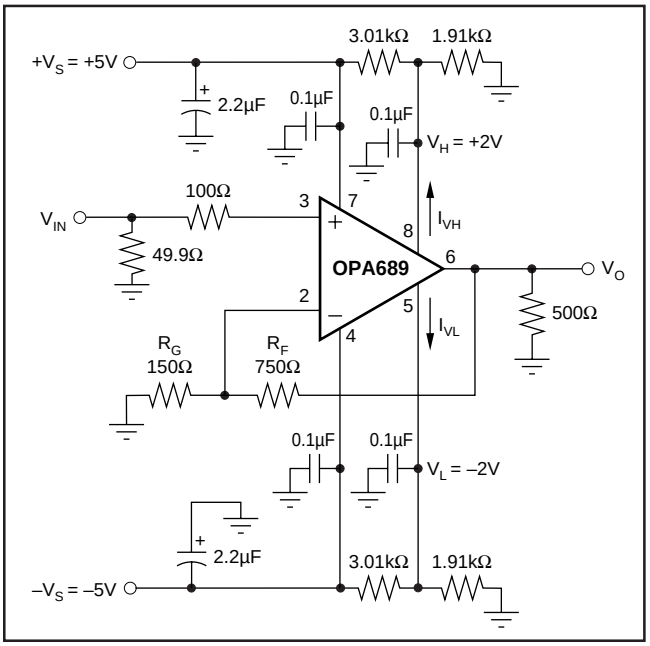


FIGURE 1. DC-Coupled, Dual Supply Amplifier.

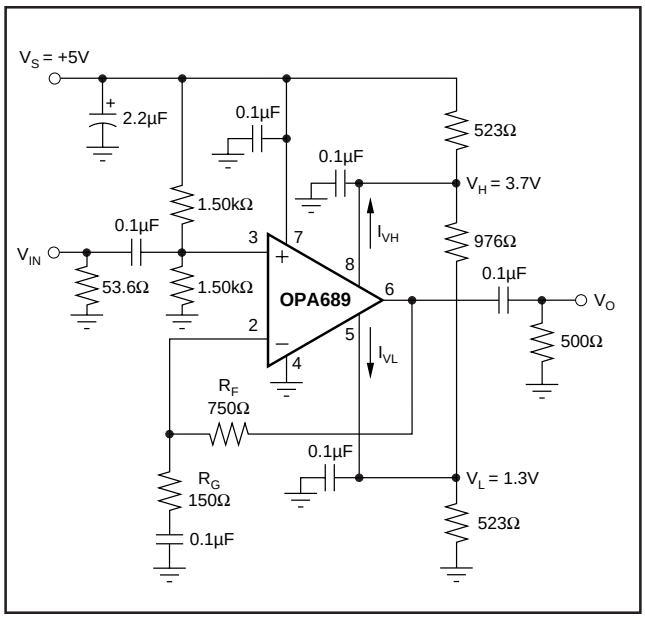


FIGURE 2. AC-Coupled, Single Supply Amplifier.

LOW DISTORTION, ADC INPUT DRIVER

The circuit in Figure 3 shows an inverting, low distortion ADC driver that operates on single supply. The converter's internal references bias the op amp input. The 4.0pF and 18pF capacitors form a compensation network that allows

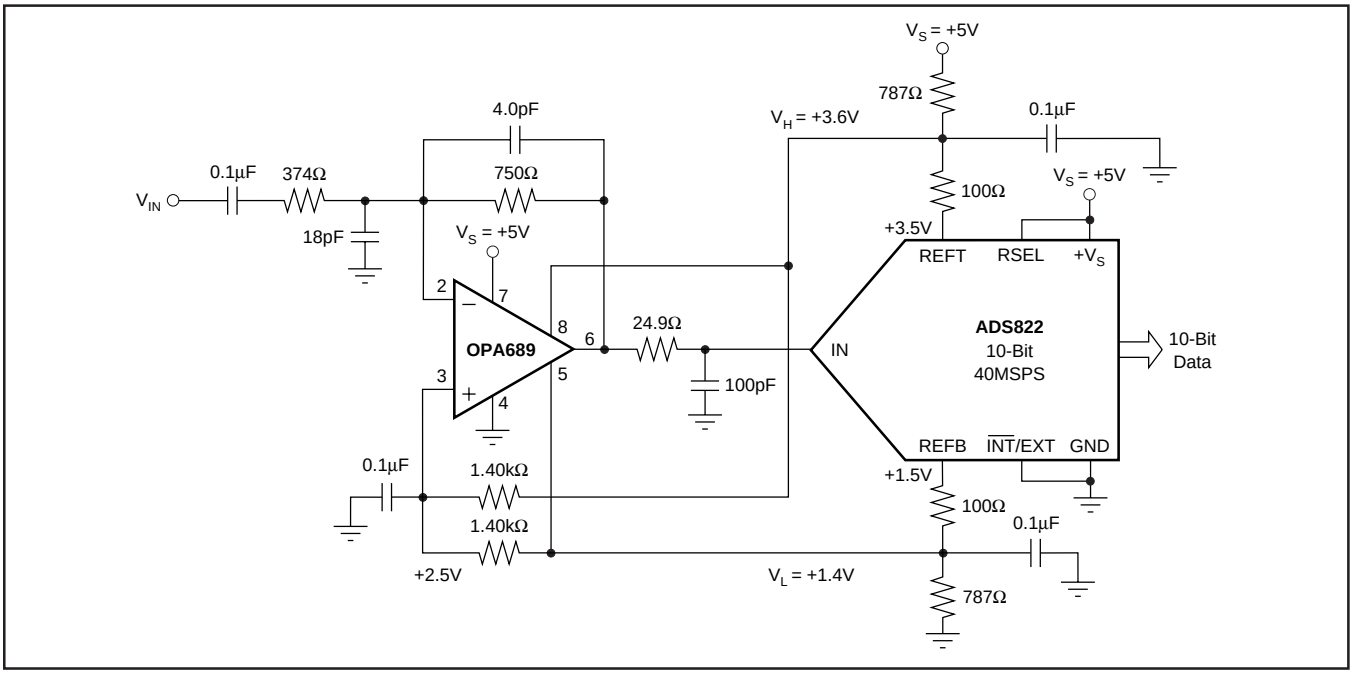


FIGURE 3. Low Distortion, Limiting ADC Input Driver.

the OPA689 to have a flat frequency response at a gain of –2. This increases the loop gain of the op amp feedback network, which reduces the distortion products below their specified values.

PRECISION HALF WAVE RECTIFIER

Figure 4 shows a half wave rectifier with outstanding precision and speed. V_H will default to a voltage between 3.1 and 3.8V if left open, while the negative limit is set to ground.

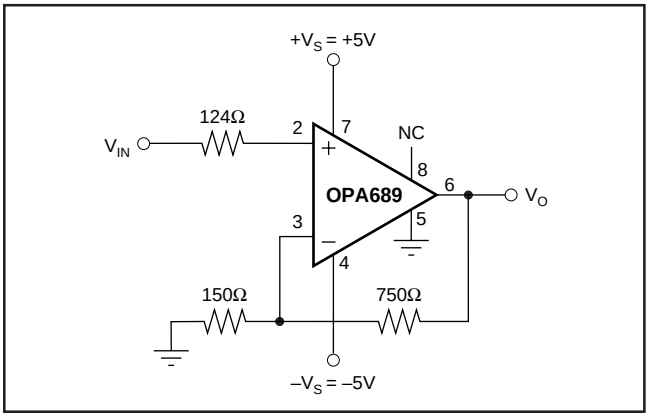


FIGURE 4. Precision Half Wave Rectifier.

VERY HIGH SPEED COMPARATOR

Figure 5 shows a very high speed comparator with hysterisis. The output level are precisely defined, and the recovery time is exceptional. The output voltage swings between 0.5V and 3.5V to provide a logic level output that switches as V_{IN} crosses V_{REF}.

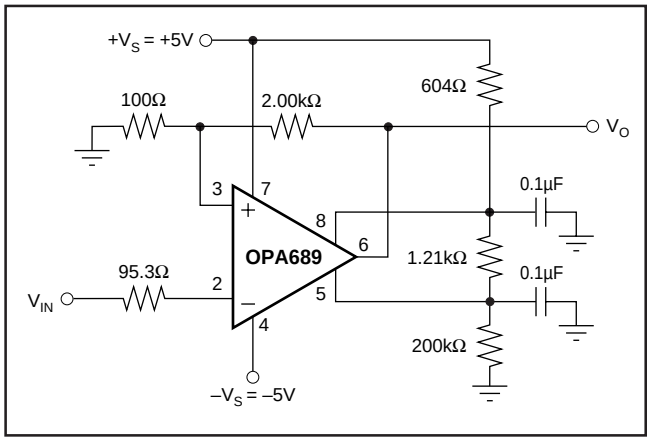


FIGURE 5. Very High Speed Comparator.

TRANSIMPEDANCE AMPLIFIER

Figure 6 shows a transimpedance amplifier that has exceptional overdrive characteristics. The feedback capacitor (C_F) stabilizes the circuit for the assumed diode capacitance (C_D).

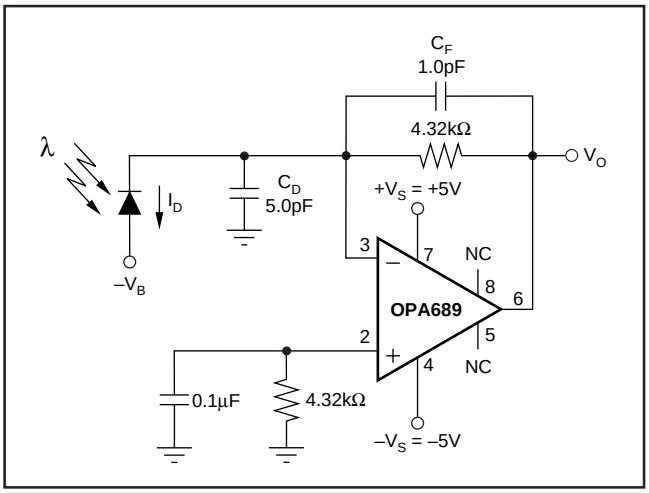


FIGURE 6. Transimpedance Amplifier.

DESIGN-IN TOOLS

APPLICATIONS SUPPORT

The Burr-Brown Applications Department is available for design assistance at phone number 1-800-548-6132 (US/Canada only). The Burr-Brown Internet web page (http://www.burr-brown.com) has the latest data sheets and other design aids.

DEMONSTRATION BOARDS

Two PC boards are available to assist in the initial evaluation of circuit performance of the OPA689 in both package styles. These will be available as an unpopulated PCB with descriptive documentation. See the board literature for more information. The summary information for these boards is shown below:

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
OPA689P	8-Pin DIP	DEM-OPA68xP	MKT-350
OPA689U	8-Pin SO-8	DEM-OPA68xU	MKT-351

Contact the Burr-Brown Applications Department for availability of these boards.

SPICE MODELS

Computer simulation of circuit performance using SPICE is often useful when analyzing analog circuit or system performance. This is particularly true for high speed amplifier circuits where parasitic capacitance and inductance can have a major effect on frequency response.

SPICE models are available through the Burr-Brown web site (www.burr-brown.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion, temperature effects, or different gain and phase characteristics. These models do not distinquish between the AC performance of different package types.

OPERATING INFORMATION

THEORY OF OPERATION

The OPA689 is a voltage feedback op amp that is stable for gains ≥ +4. The output voltage is limited to a range set by the limiter pins (5 and 8). When the input tries to overdrive the output, the limiters take control of the output buffer. This avoids saturating any parts in the signal path, gives quick overdrive recovery, and gives consistent limiter accuracy for any gain.

This part is de-compensated (stable for gains ≥ +4). This gives greater bandwidth, higher slew rate, and lower noise than the unity gain stable companion part OPA688.

The limiters have a very sharp transition from the linear region of operation to output limiting. This allows the limiter voltages to be set very near (<100 mV) the desired signal range. The distortion performance is also very good near the limiter voltages.

CIRCUIT LAYOUT

Achieving optimum performance with the high frequency OPA689 requires careful attention to layout design and component selection. Recommended PCB layout techniques and component selection criteria are:

a) **Minimize parasitic capacitance to any ac ground** for all of the signal I/O pins. Open a window in the ground and power planes around the signal I/O pins, and leave the ground and power planes unbroken elsewhere.

b) **Provide a high quality power supply.** Use linear regulators, ground plane, and power planes, to provide power. Place high frequency 0.1µF decoupling capacitors < 0.2" away from each power supply pin. Use wide, short traces to connect to these capacitors to the ground and power planes. Also use larger (2.2µF to 6.8µF) high frequency decoupling capacitors to bypass lower frequencies. They may be somewhat further from the device, and be shared among several adjacent devices.

c) **Place external components close** to the OPA689. This minimizes inductance, ground loops, transmission line effects and propagation delay problems. Be extra careful with the feedback (R_F), input and output resistors.

d) **Use high frequency components** to minimize parasitic elements. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter layout. Metal film or carbon composition axially-leaded resistors can also provide good performance when their leads are as short as possible. Never use wire-wound resistors for high frequency applications. Remember that most potentiometers have large parasitic capacitances and inductances.

Multilayer ceramic chip capacitors work best and take up little space. Monolithic ceramic capacitors also work very well. Use RF type capacitors with low ESR and ESL. The large power pin bypass capacitors (2.2µF to 6.8µF) should be tantalum for better high frequency and pulse performance.

e) **Choose low resistor values** to minimize the time constant set by the resistor and its parasitic parallel capacitance. Good metal film or surface mount resistors have approximately 0.2pF parasitic parallel capacitance. For resistors > 1.5kΩ, this adds a pole and/or zero below 500MHz.

Make sure that the output loading is not too heavy. The recommended 750Ω feedback resistor is a good starting point in your design.

f) **Use short direct traces to other wideband devices** on the board. Short traces act as a lumped capacitive load. Wide traces (50 to 100 mils) should be used. Estimate the total capacitive load at the output, and use the series isolation resistor recommended in the *R_S vs Capacitive Load* plot. Parasitic loads < 2pF may not need the isolation resistor.

g) **When long traces are necessary,** use transmission line design techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω transmission line is not required on board—a higher characteristic impedance will help reduce output loading. Use a matching series resistor at the output of the op amp to drive a transmission line, and a matched load resistor at the other end to make the line appear as a resistor. If the 6dB of attenuation that the matched load produces is not acceptable, and the line is not too long, use the series resistor at the source only. This will isolate the op amp output from the reactive load presented by the line, but the frequency response will be degraded.

Multiple destination devices are best handled as separate transmission lines, each with its own series source and shunt load terminations. Any parasitic impedances acting on the terminating resistors will alter the transmission line match, and can cause unwanted signal reflections and reactive loading.

h) **Do not use sockets** for high speed parts like the OPA689. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network. Best results are obtained by soldering the part onto the board. If socketing for DIP prototypes is desired, high frequency flush mount pins (e.g., McKenzie Technology #710C) can give good results.

POWER SUPPLIES

The OPA689 is nominally specified for operation using either ±5V supplies or a single +5V supply. The maximum specified total supply voltage of 13V allows reasonable tolerances on the supplies. Higher supply voltages can break down internal junctions, possibly leading to catastrophic failure. Single supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow design of non-standard or single supply operation circuits. Figure 2 shows one approach to single-supply operation.

ESD PROTECTION

ESD damage is known to damage MOSFET devices, but any semiconductor device is vulnerable to ESD damage. This is particularly true for very high speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are required when handling the OPA689.

OUTPUT LIMITERS

The output voltage is linearly dependent on the input(s) when it is between the limiter voltages V_H (pin 8) and V_L (pin 5). When the output tries to exceed V_H or V_L, the corresponding limiter buffer takes control of the output voltage and holds it at V_H or V_L.

Because the limiters act on the output, their accuracy does not change with gain. The transition from the linear region of operation to output limiting is sharp—the desired output signal can safely come to within 30mV of V_H or V_L. Distortion performance is also good over the same range.

The limiter voltages can be set to within 0.7V of the supplies ($V_L \geq -V_S + 0.7V$, $V_H \leq +V_S - 0.7V$). They must also be at least 200mV apart ($V_H - V_L \geq 0.2V$).

When pins 5 and 8 are left open, V_H and V_L go to the Default Voltage Limit; the minimum values are in the spec table. Looking at Figure 7 for the zero bias current case will show the expected range of (V_S – default limit voltages) = headroom).

When the limiter voltages are more than 2.1V from the supplies ($V_L \geq -V_S + 2.1V$ or $V_H \leq +V_S - 2.1V$), you can use simple resistor dividers to set V_H and V_L (see Figure 1). Make sure you include the Limiter Input Bias Currents (Figure 7) in the calculations (i.e., $I_{VL} \approx -50\mu A$ out of pin 5, and $I_{VH} \approx +50\mu A$ out of pin 8). For good limiter voltage accuracy, run at least 1mA quiescent bias current through these resistors.

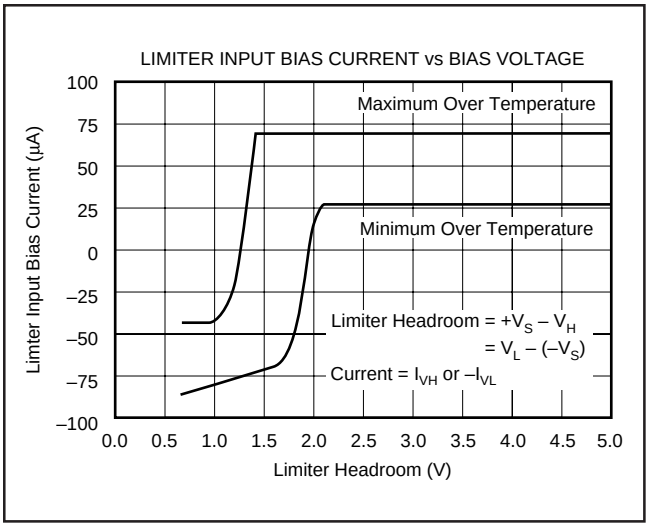


FIGURE 7. Limiter Bias Current vs Limiter Voltage.

When the limiter voltages need to be within 2.1V of the supplies ($V_L \leq -V_S + 2.1V$ or $V_H \geq +V_S - 2.1V$), use low impedance voltage sources to set V_H and V_L to minimize errors due to bias current uncertainty. This will typically be the case for single supply operation (V_S = +5V). Figure 2 runs 2.5mA through the resistive divider that sets V_H and V_L. This keeps errors due to I_{VH} and I_{VL} < ±1% of the target limit voltages.

The limiters' DC accuracy depends on attention to detail. The two dominant error sources can be improved as follows:

- Power supplies, when used to drive resistive dividers that set V_H and V_L, can contribute large errors (e.g., (5%). Using a more accurate source, or bypassing pins 5 and 8 with good capacitors, will improve limiter PSRR.
- The resistor tolerances in the resistive divider can also dominate. Use 1% resistors.

Other error sources also contribute, but should have little impact on the limiters' DC accuracy:

- Reduce offsets caused by the Limiter Input Bias Currents. Select the resistors in the resistive divider(s) as described above.
- Consider the signal path DC errors as contributing to the uncertainty in the useable output range.
- The Limiter Offset Voltage only slightly degrades the limiter accuracy.

Figure 8 shows how the limiters affect distortion performance. Virtually no degradation in linearity is observed for output voltages swinging right up to the limiter voltages.

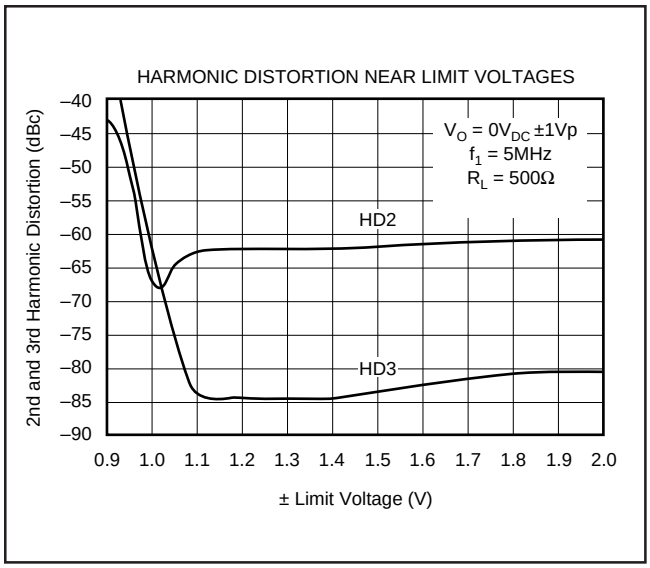


FIGURE 8. Linearity Guardband.

OFFSET VOLTAGE ADJUSTMENT

The circuit in Figure 9 allows offset adjustment without degrading offset drift with temperature. Use this circuit with caution since power supply noise can inadvertently couple into the op amp.

Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the resistance seen by both DC Input Bias Currents by using R_3. This minimizes the output offset voltage caused by the Input Bias Currents.

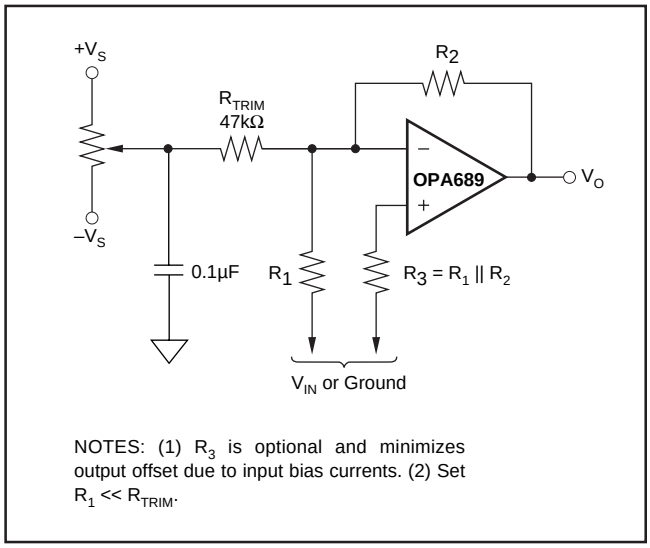


FIGURE 9. Offset Voltage Trim.

OUTPUT DRIVE

The OPA689 has been optimized to drive 500Ω loads, such as A/D converters. It still performs very well driving 100Ω loads. This makes the OPA689 an ideal choice for a wide range of high frequency applications.

Many high speed applications, such as driving A/D converters, require op amps with low output impedance. As shown in the *Output Impedance vs Frequency* performance curve, the OPA689 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain decreases with frequency.

THERMAL CONSIDERATIONS

The OPA689 will not require heat-sinking under most operating conditions. Maximum desired junction temperature will set a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and the additional power dissipated in the output stage (P_{DL}) while delivering load power. P_{DQ} is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signals and loads. For a grounded resistive load, and equal bipolar supplies, it is at a maximum when the output is at 1/2 either supply voltage. In this condition, $P_{DL} = V_S^2/(4R_L)$ where R_L includes the feedback network loading. Note that it is the power in the output stage, and not in the load, that determines internal power dissipation.

The operating junction temperature is: $T_J = T_A + P_D \theta_{JA}$, where T_A is the ambient temperature.

For example, the maximum T_J for a OPA689U with G = +6, $R_{FB} = 750\Omega$, $R_L = 100\Omega$, and $\pm V_S = \pm 5V$ at the maximum $T_A = +85°C$ is calculated this way:

$$P_{DQ} = (10V \cdot 20mA) = 200mW$$

$$P_{DL} = \frac{(5V)^2}{4 \cdot (100\Omega \,||\, 850\Omega)}$$

$$P_D = 200mW + 70mW = 270mW$$

$$T_J = 85°C + 270mW \cdot 125°C/W = 119°C$$

CAPACITIVE LOADS

Capacitive loads, such as flash A/D converters, will decrease the amplifier's phase margin, which may cause peaking or oscillations. Capacitive loads ≥ 1pF should be isolated by connecting a small resistor in series with the output as shown in Figure 10. Increasing the gain from +6 will improve the capacitive drive capabilities due to increased phase margin.

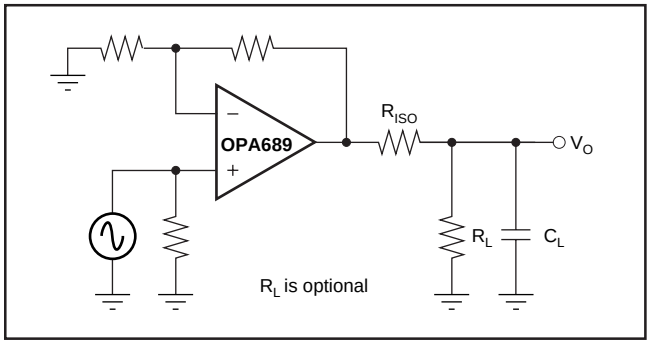


FIGURE 10. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable, or transmission line, is terminated in its characteristic impedance.

FREQUENCY RESPONSE COMPENSATION

The OPA689 is internally compensated to be stable at a gain of +4, and has a nominal phase margin of 60° at a gain of +6. Phase margin and peaking improve at higher gains. Recall that an inverting gain of –5 is equivalent to a gain of +6 for bandwidth purposes (i.e., noise gain = 6).

Standard external compensation techniques work with this device. For example, in the inverting configuration, the bandwidth may be limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at high frequencies, which limits the bandwidth.

To maintain a large bandwidth at high gains, cascade several op amps.

In applications where a large feedback resistor is required, such as photodiode transimpedance amplifier, the parasitic capacitance from the inverting input to ground causes peaking or oscillations. To compensate for this effect, connect a small capacitor in parallel with the feedback resistor. The bandwidth will be limited by the pole that the feedback resistor and this capacitor create. In other high gain applications, use a three resistor "Tee" network to reduce the RC time constants set by the parasitic capacitances. Be careful to not increase the noise generated by this feedback network too much.

PULSE SETTLING TIME

The OPA689 is capable of an extremely fast settling time in response to a pulse input. Frequency response flatness and phase linearity are needed to obtain the best settling times. For capacitive loads, such as an A/D converter, use the recommended R_S in the *R_S vs Capacitive Load* plot. Extremely fine scale settling (0.01%) requires close attention to ground return current in the supply decoupling capacitors.

The pulse settling characteristics when recovering from overdrive are very good.

DISTORTION

The OPA689's distortion performance is specified for a 500Ω load, such as an A/D converter. Driving loads with smaller resistance will increase the distortion as illustrated in Figure 11. Remember to include the feedback network in the load resistance calculations.

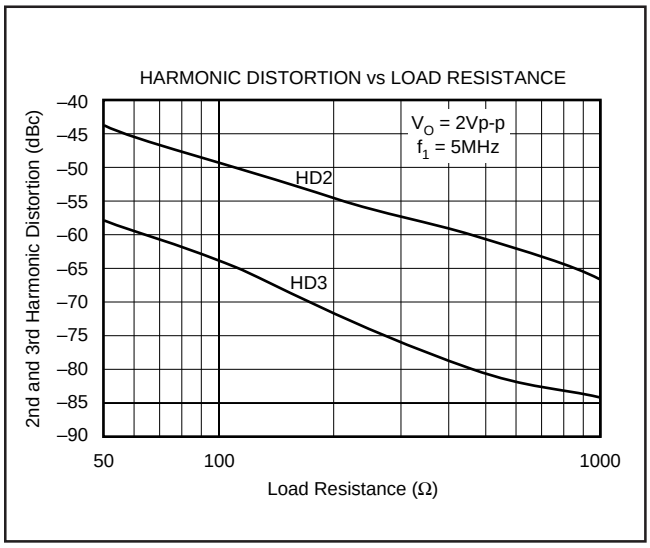


FIGURE 11. 5MHz Harmonic Distortion vs Load Resistance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA689P	LIFEBUY	PDIP	P	8	50	Pb-Free (RoHS)	Call TI	Level-NC-NC-NC
OPA689U	OBSOLETE	SOIC	D	8		None	Call TI	Call TI
OPA689U/2K5	OBSOLETE	SOIC	D	8		None	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265