

**PGA204  
PGA205**

## Programmable Gain INSTRUMENTATION AMPLIFIER

### FEATURES

- **DIGITALLY PROGRAMMABLE GAIN:**  
     PGA204:  $G=1, 10, 100, 1000V/V$   
     PGA205:  $G=1, 2, 4, 8V/V$
- **LOW OFFSET VOLTAGE:**  $50\mu V$  max
- **LOW OFFSET VOLTAGE DRIFT:**  $0.25\mu V/^\circ C$
- **LOW INPUT BIAS CURRENT:**  $2nA$  max
- **LOW QUIESCENT CURRENT:**  $5.2mA$  typ
- **NO LOGIC SUPPLY REQUIRED**
- **16-PIN PLASTIC DIP, SOL-16 PACKAGES**

### APPLICATIONS

- **DATA ACQUISITION SYSTEM**
- **GENERAL PURPOSE ANALOG BOARDS**
- **MEDICAL INSTRUMENTATION**

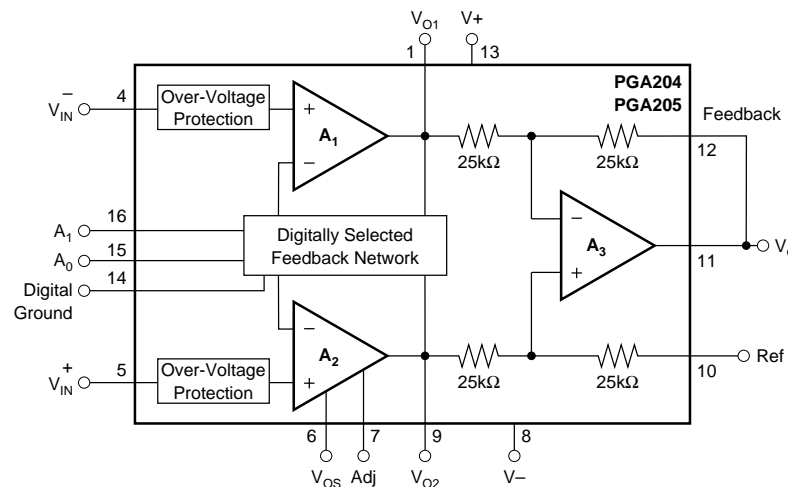
### DESCRIPTION

The PGA204 and PGA205 are low cost, general purpose programmable-gain instrumentation amplifiers offering excellent accuracy. Gains are digitally selected: PGA204—1, 10, 100, 1000, and PGA205—1, 2, 4, 8V/V. The precision and versatility, and low cost of the PGA204 and PGA205 make them ideal for a wide range of applications.

Gain is selected by two TTL or CMOS-compatible address lines,  $A_0$  and  $A_1$ . Internal input protection can withstand up to  $\pm 40V$  on the analog inputs without damage.

The PGA204 and PGA205 are laser trimmed for very low offset voltage ( $50\mu V$ ), drift ( $0.25\mu V/^\circ C$ ) and high common-mode rejection (115dB at  $G=1000$ ). They operate with power supplies as low as  $\pm 4.5V$ , allowing use in battery operated systems. Quiescent current is 5mA.

The PGA204 and PGA205 are available in 16-pin plastic DIP, and SOL-16 surface-mount packages, specified for the  $-40^\circ C$  to  $+85^\circ C$  temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706  
 Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132





## PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
PGA204AP	16-Pin Plastic DIP	180
PGA204BP	16-Pin Plastic DIP	180
PGA204AU	SOL-16 Surface Mount	211
PGA204BU	SOL-16 Surface Mount	211
PGA205AP	16-Pin Plastic DIP	180
PGA205BP	16-Pin Plastic DIP	180
PGA205AU	SOL-16 Surface Mount	211
PGA205BU	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

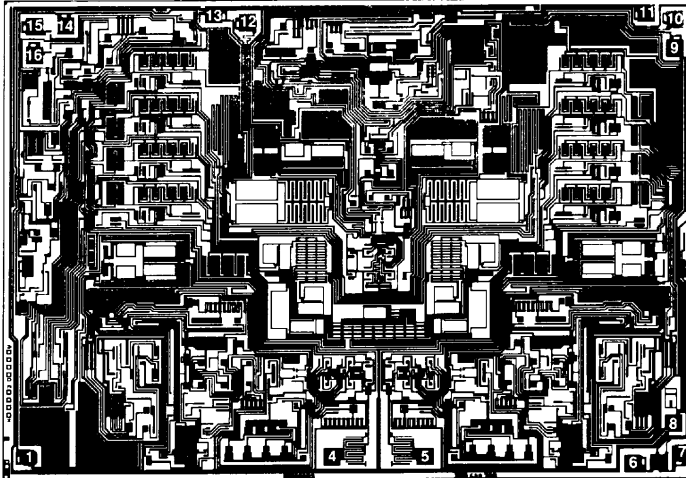
## ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....	±18V
Analog Input Voltage Range .....	±40V
Logic Input Voltage Range .....	±V <sub>S</sub>
Output Short-Circuit (to ground) .....	Continuous
Operating Temperature .....	-40°C to +125°C
Storage Temperature .....	-40°C to +125°C
Junction Temperature .....	+150°C
Lead Temperature (soldering -10s) .....	+300°C

## ORDERING INFORMATION

MODEL	GAINS	PACKAGE	TEMPERATURE RANGE
PGA204AP	1, 10, 100, 1000V/V	16-Pin Plastic DIP	-40 to +85°C
PGA204BP	1, 10, 100, 1000V/V	16-Pin Plastic DIP	-40 to +85°C
PGA204AU	1, 10, 100, 1000V/V	SOL-16 Surface-Mount	-40 to +85°C
PGA204BU	1, 10, 100, 1000V/V	SOL-16 Surface-Mount	-40 to +85°C
PGA205AP	1, 2, 4, 8V/V	16-Pin Plastic DIP	-40 to +85°C
PGA205BP	1, 2, 4, 8V/V	16-Pin Plastic DIP	-40 to +85°C
PGA205AU	1, 2, 4, 8V/V	SOL-16 Surface-Mount	-40 to +85°C
PGA205BU	1, 2, 4, 8V/V	SOL-16 Surface-Mount	-40 to +85°C

## DICE INFORMATION



PGA204/205 DIE TOPOGRAPHY

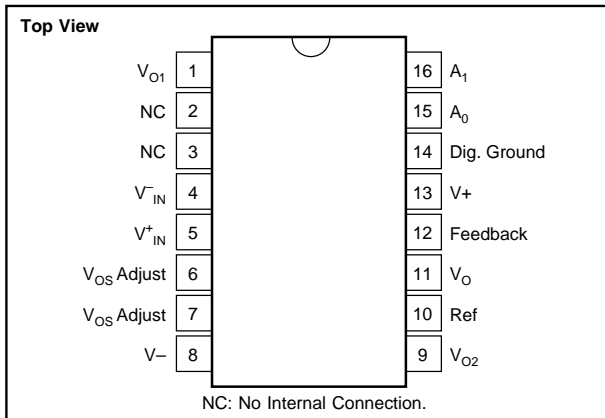
PAD	FUNCTION	PAD	FUNCTION
1	$V_{O1}$	9	$V_{O2}$
2	—	10	Ref
3	—	11	$V_O$
4	$V_{IN}^-$	12	Feedback
5	$V_{IN}^+$	13	$V_+$
6	$V_{OS}$ Adj	14	Dig. Ground
7	$V_{OS}$ Adj	15	$A_0$
8	$V_-$	16	$A_1$

Substrate Bias: Internally connected to  $V_-$  power supply.

## MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	186 x 130 ±5	4.72 x 3.30 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Gold

## PIN CONFIGURATION



## ELECTROSTATIC DISCHARGE SENSITIVITY

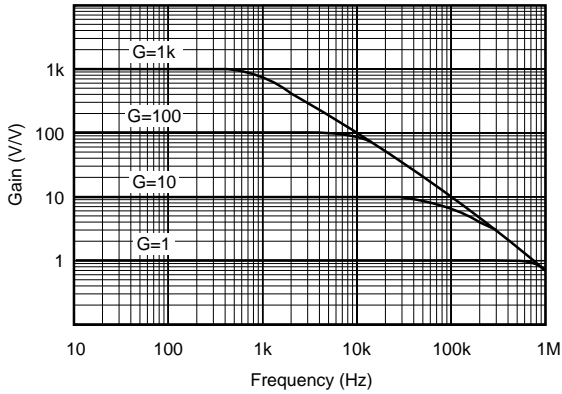
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

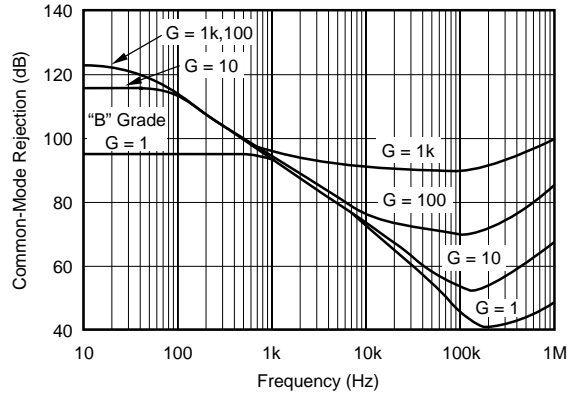
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.

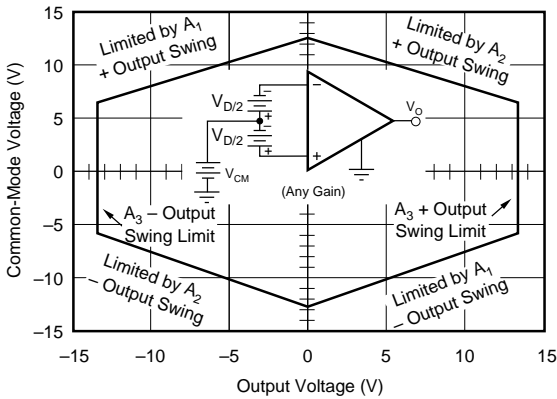
GAIN vs FREQUENCY



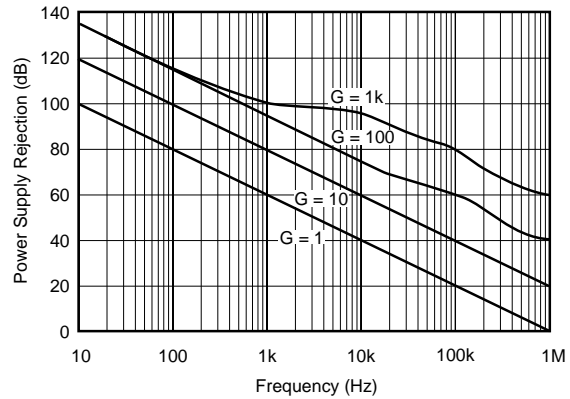
COMMON-MODE REJECTION vs FREQUENCY



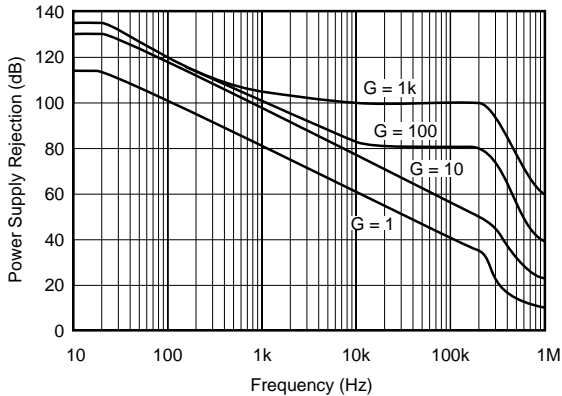
INPUT COMMON-MODE VOLTAGE RANGE vs OUTPUT VOLTAGE



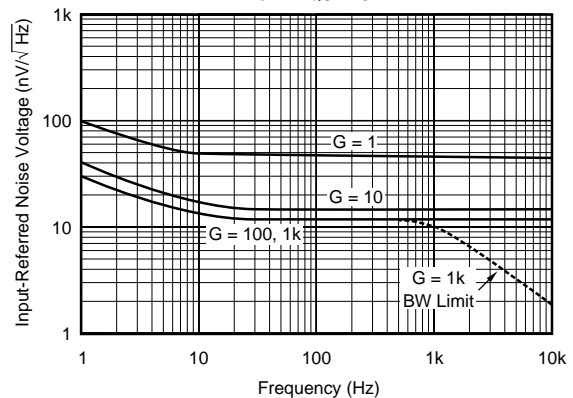
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY

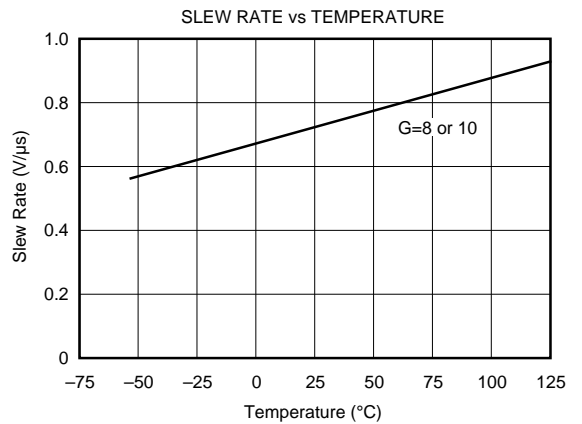
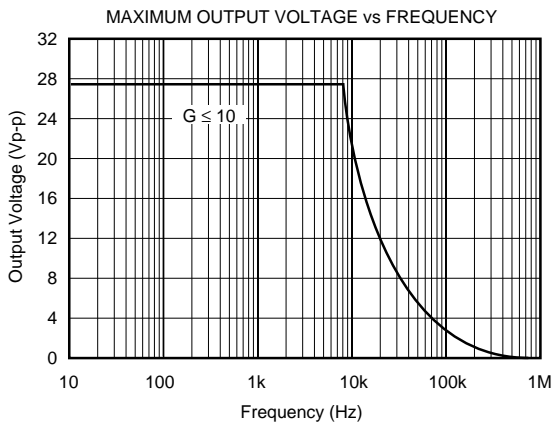
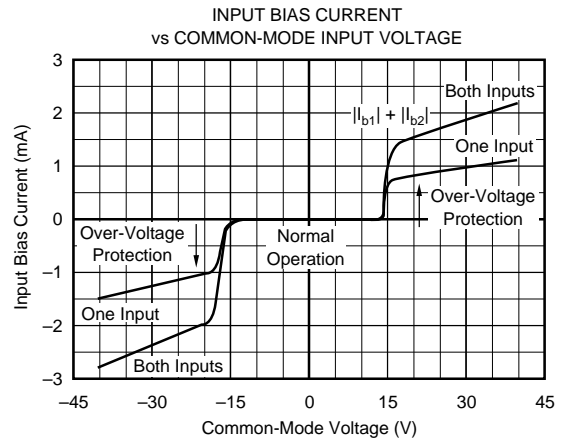
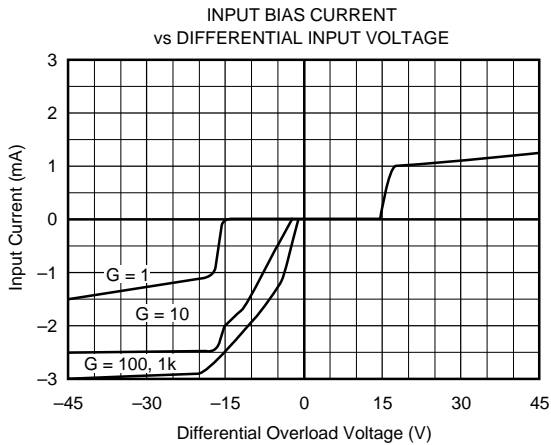
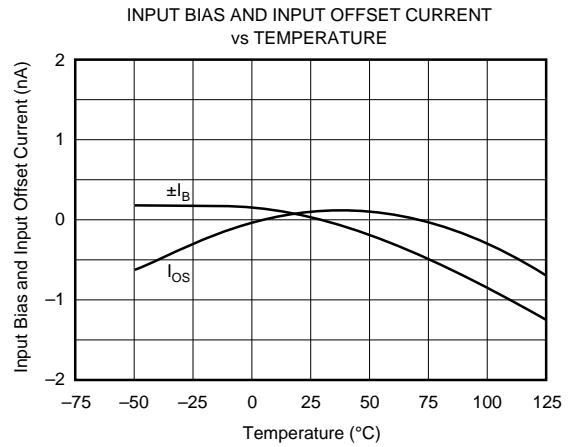
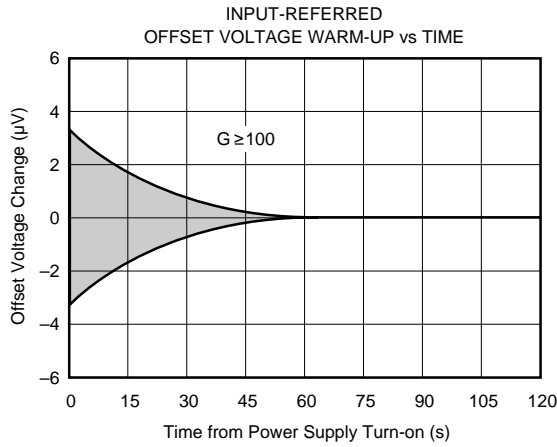


INPUT-REFERRED NOISE VOLTAGE vs FREQUENCY



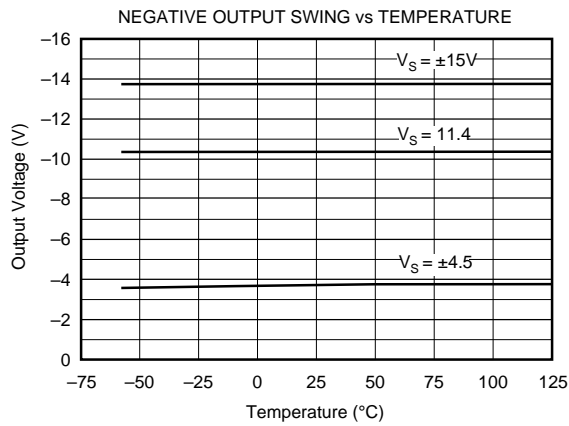
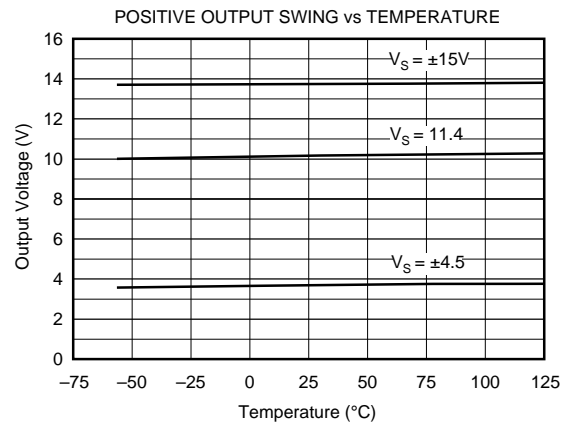
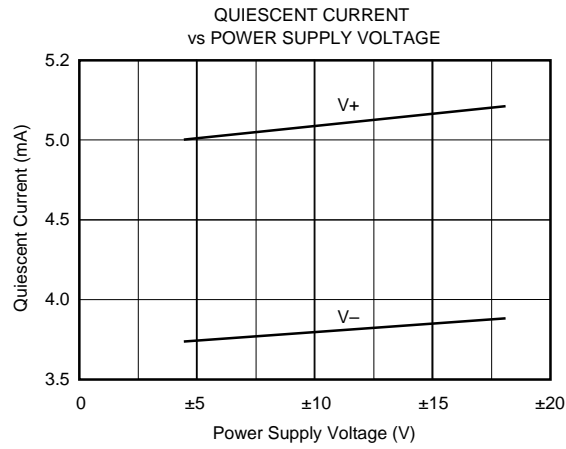
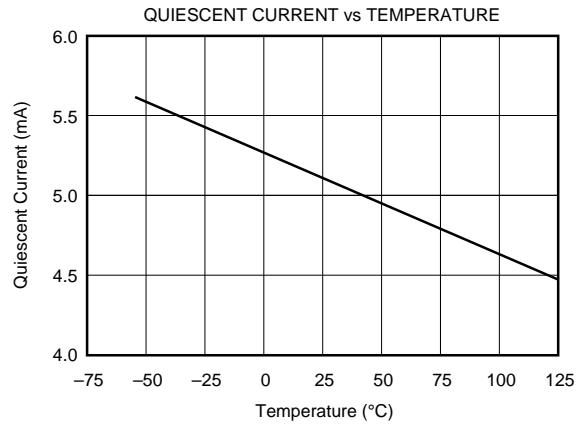
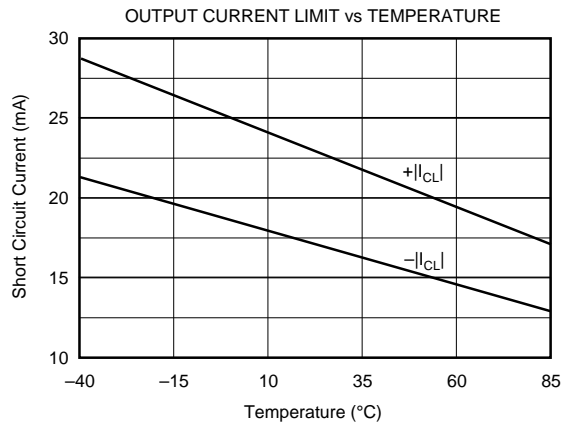
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (CONT)

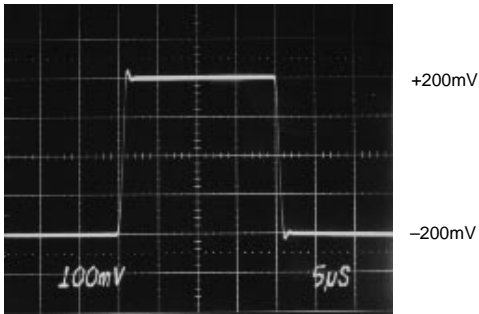
At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



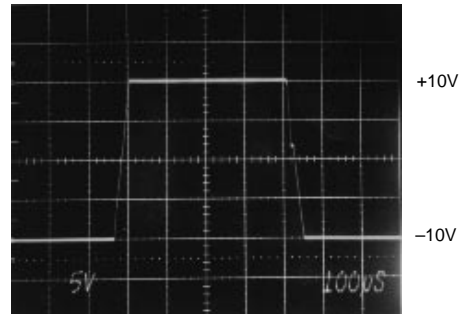
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.

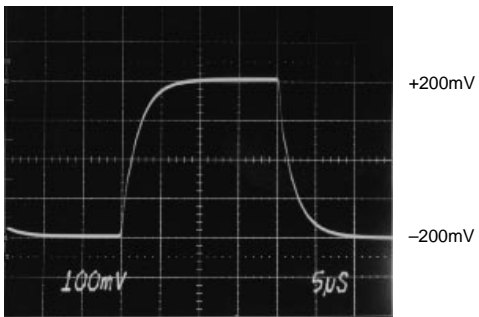
SMALL-SIGNAL RESPONSE,  $G = 1$



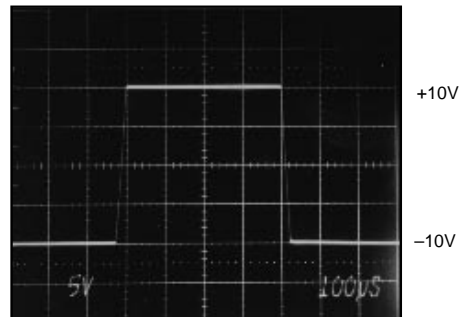
LARGE-SIGNAL RESPONSE,  $G = 1$



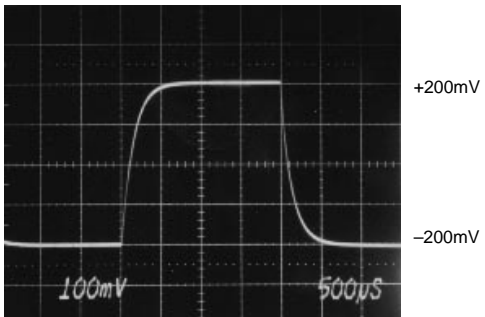
SMALL-SIGNAL RESPONSE,  $G = 10$



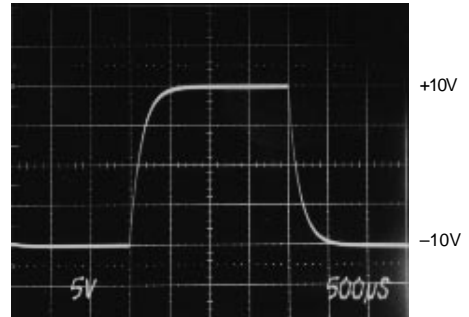
LARGE-SIGNAL RESPONSE,  $G = 10$



SMALL-SIGNAL RESPONSE,  $G = 1000$

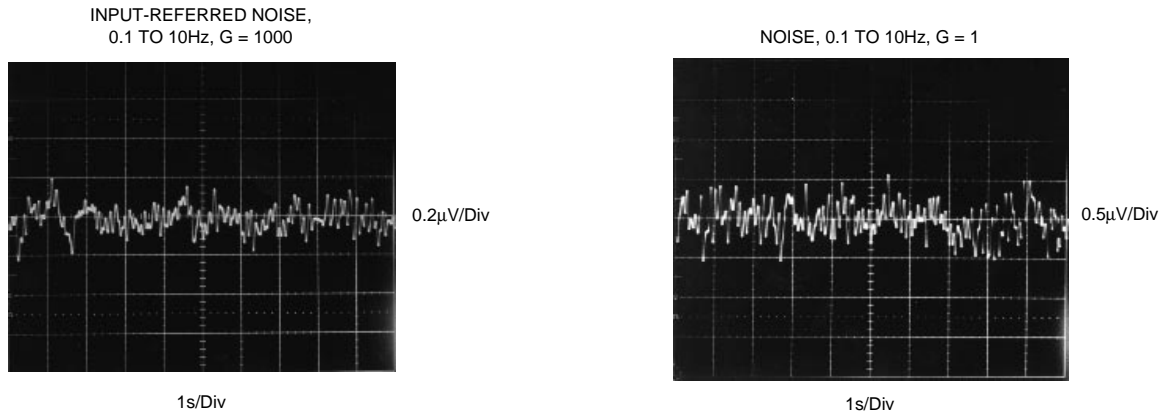


LARGE-SIGNAL RESPONSE,  $G = 1000$



# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



## APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the PGA204/205. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of  $5\Omega$  in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR ( $G=1$ ).

The PGA204/205 has an output feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. The output Feedback connection can

be used to sense the output voltage directly at the load for best accuracy.

### DIGITAL INPUTS

The digital inputs  $A_0$  and  $A_1$  select the gain according to the logic table in Figure 1. Logic "1" is defined as a voltage greater than 2V above digital ground potential (pin 14). Digital ground can be connected to any potential from the  $V^-$  power supply to 4V less than  $V^+$ . Digital ground is normally connected to ground. The digital inputs interface directly CMOS and TTL logic components.

Approximately  $1\mu\text{A}$  flows out of the digital input pins when a logic "0" is applied. Logic input current is nearly zero with a logic "1" input. A constant current of approximately

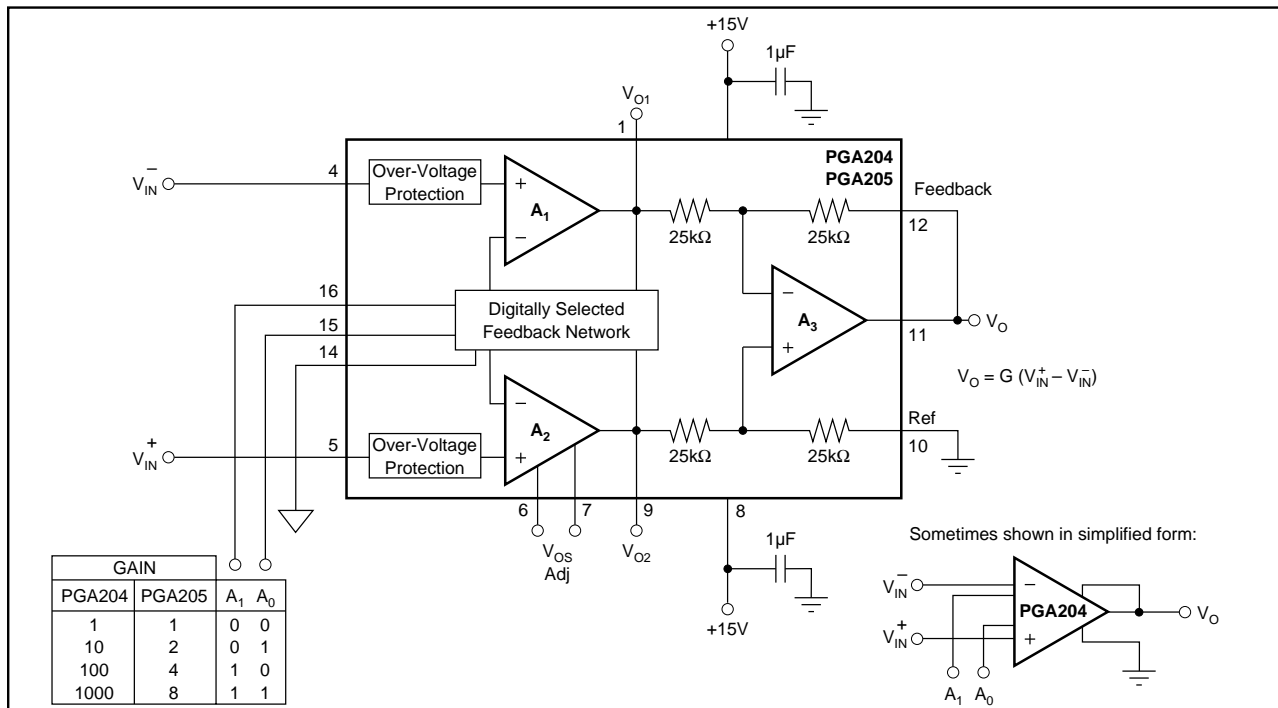


FIGURE 1. Basic Connections.

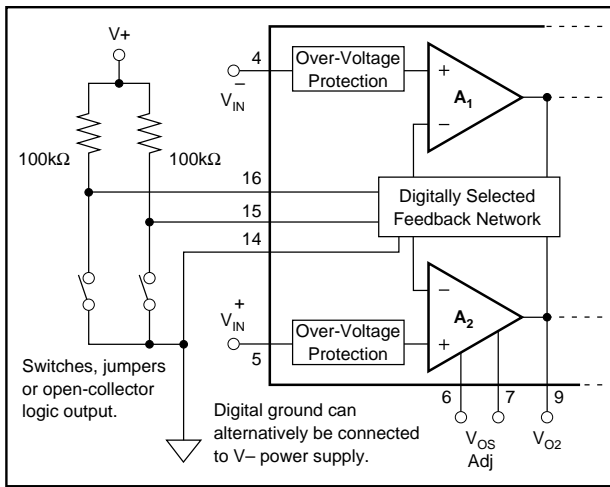


FIGURE 2. Switch or Jumper-Selected Digital Inputs.

1.3mA flows in the digital ground pin. It is good practice to return digital ground through a separate connection path so that analog ground is not affected by the digital ground current.

The digital inputs,  $A_0$  and  $A_1$ , are not latched; a change in logic inputs immediately selects a new gain. Switching time of the logic is approximately 1 $\mu$ s. The time to respond to gain change is effectively the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see settling time specifications).

Many applications use an external logic latch to access gain control data from a high speed data bus (see Figure 7). Using an external latch isolates the high speed digital bus from sensitive analog circuitry. Locate the latch circuitry as far as practical from analog circuitry.

Some applications select gain of the PGA204/205 with switches or jumpers. Figure 2 shows pull-up resistors connected to assure a noise-free logic “1” when the switch, jumper or open-collector logic is open or off. Fixed-gain applications can connect the logic inputs directly to  $V_+$  or  $V_-$  (or other valid logic level); no resistor is required.

## OFFSET VOLTAGE

Voltage offset of the PGA204/205 consists of two components—input stage offset and output stage offset. Both components are specified in the specification table in equation form:

$$V_{OS} = V_{OSI} + V_{OSO} / G \quad (1)$$

where:

$V_{OS}$  total is the combined offset, referred to the input.

$V_{OSI}$  is the offset voltage of the input stage,  $A_1$  and  $A_2$ .

$V_{OSO}$  is the offset voltage of the output difference amplifier,  $A_3$ .

$V_{OSI}$  and  $V_{OSO}$  do not change with gain. The composite offset voltage  $V_{OS}$  changes with gain because of the gain term in equation 1. Input stage offset dominates in high gain ( $G \geq 100$ ); both sources of offset may contribute at low gain ( $G = 1$  to 10).

## OFFSET TRIMMING

Both the input and output stages are laser trimmed for very low offset voltage and drift. Many applications require no external offset adjustment.

Figure 3 shows an optional input offset voltage trim circuit. This circuit should be used to adjust only the input stage offset voltage of the PGA204/205. Do this by programming

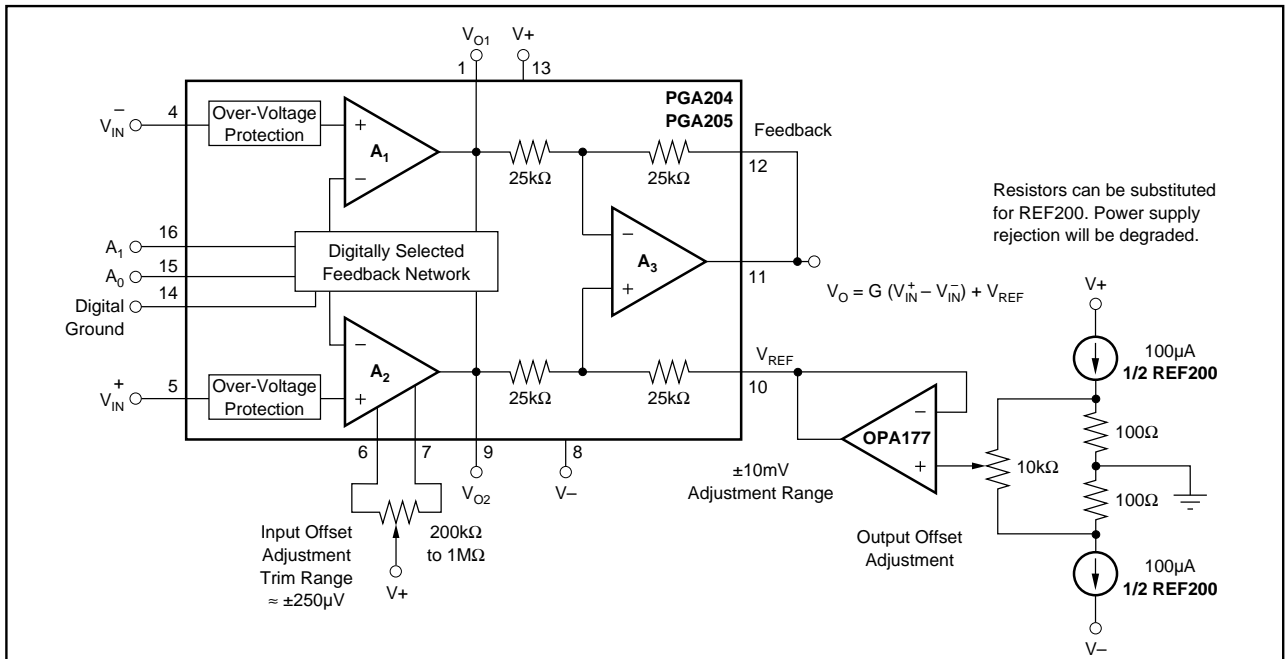


FIGURE 3. Optional Offset Voltage Trim Circuit.

it to its highest gain and trimming the output voltage to zero with the inputs grounded. Drift performance usually improves slightly when the input offset is nulled with this procedure.

Do not use the input offset adjustment to trim system offset or offset produced by a sensor. Nulling offset that is not produced by the input amplifiers will increase temperature drift by approximately  $3.3\mu\text{V}/^\circ\text{C}$  per 1mV of offset adjustment.

Many applications that need input stage offset adjustment do not need output stage offset adjustment. Figure 3 also shows a circuit for adjusting output offset voltage. First, adjust the input offset voltage as discussed above. Then program the device for  $G=1$  and adjust the output to zero. Because of the interaction of these two adjustments at  $G=8$ , the PGA205 may require iterative adjustment.

The output offset adjustment can be used to trim sensor or system offsets without affecting drift. The voltage applied to the Ref terminal is summed with the output signal. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering the trim voltage with an op amp as shown.

## NOISE PERFORMANCE

The PGA204/205 provides very low noise in most applications. Low frequency noise is approximately  $0.4\mu\text{Vp-p}$  measured from 0.1 to 10Hz. This is approximately one-tenth the noise of “low noise” chopper-stabilized amplifiers.

## INPUT BIAS CURRENT RETURN PATH

The input impedance of the PGA204/205 is extremely high—approximately  $10^{10}\Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than  $\pm 1\text{nA}$  (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the PGA204/205 is to operate properly. Figure 4 shows provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the PGA204/205 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 4). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due bias current and better common-mode rejection.

Many sources or sensors inherently provide a path for input bias current (e.g. the bridge sensor shown in Figure 4). These applications do not require additional resistor(s) for proper operation.

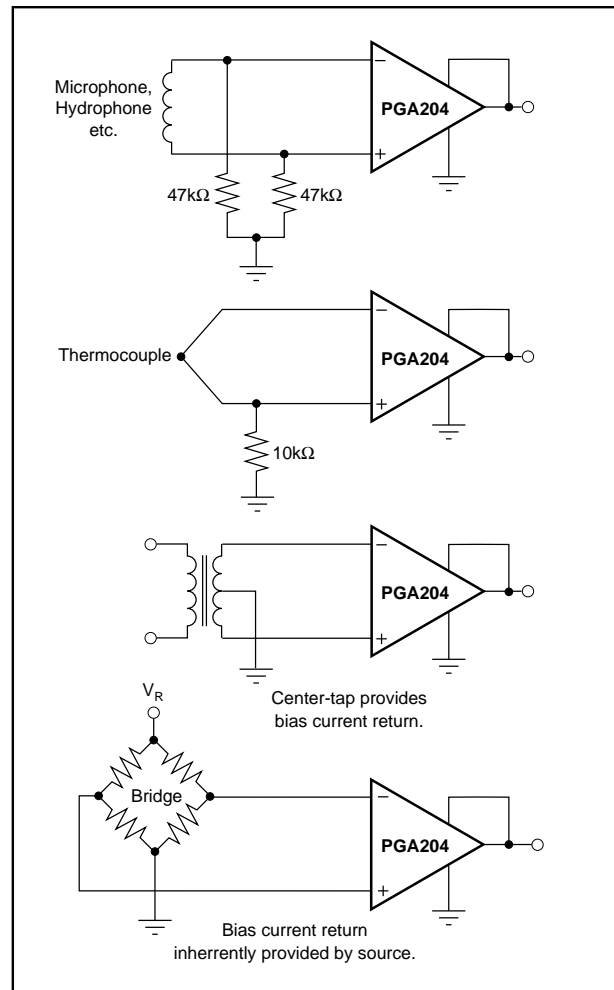


FIGURE 4. Providing an Input Common-Mode Current Path.

## INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the PGA204/205 is approximately  $\pm 12.7\text{V}$  (or 2.3V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers,  $A_1$  and  $A_2$ . The common-mode range is related to the output voltage of the complete amplifier—see performance curve “Input Common-Mode Range vs Output Voltage”.

A combination of common-mode and differential input voltage can cause the output of  $A_1$  or  $A_2$  to saturate. Figure 5 shows the output voltage swing of  $A_1$  and  $A_2$  expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier,  $A_3$ . For applications where input common-mode range must be maximized, limit the output voltage swing by selecting a lower gain of the PGA204/205 (see performance curve “Input Common-Mode Voltage Range vs Output Voltage”). If necessary, add gain after the PGA204/205 to increase the voltage swing.

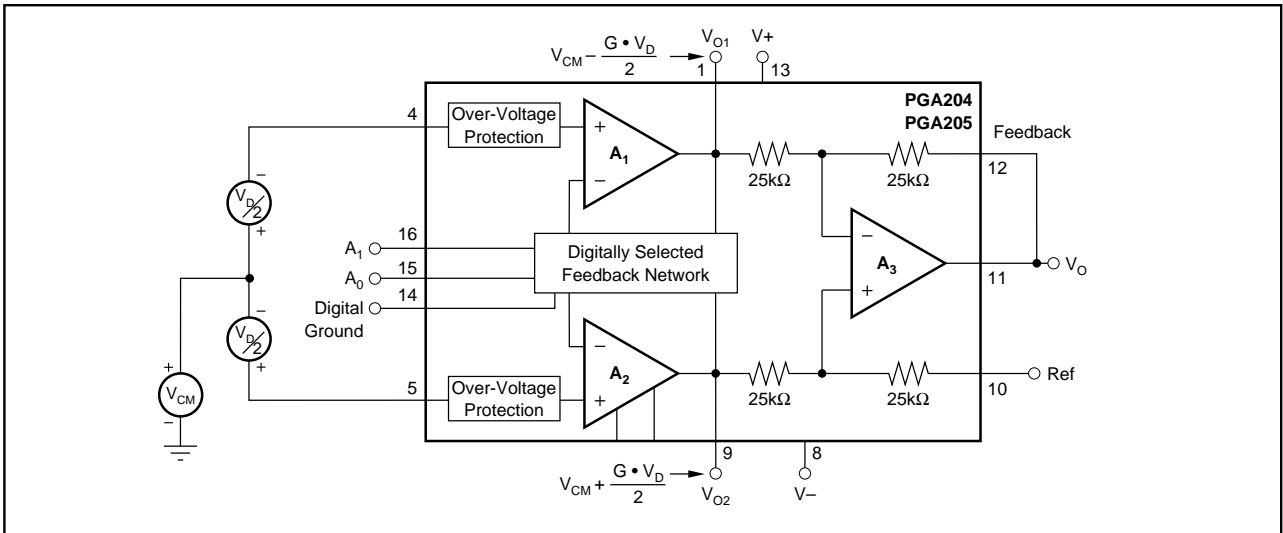


FIGURE 5. Voltage Swing of A<sub>1</sub> and A<sub>2</sub>.

Input-overload often produces an output voltage that appears normal. For example, consider an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the PGA204/205 will be near 0V even though both inputs are overloaded.

### INPUT PROTECTION

The inputs of the PGA204/205 are individually protected for voltages up to  $\pm 40V$ . For example, a condition of  $-40V$  on one input and  $+40V$  on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

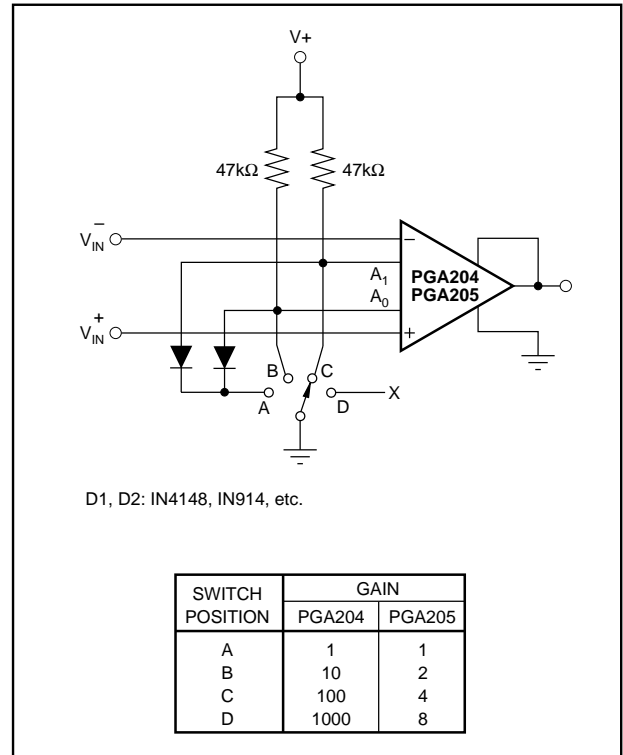


FIGURE 6. Switch-Selected PGIA.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

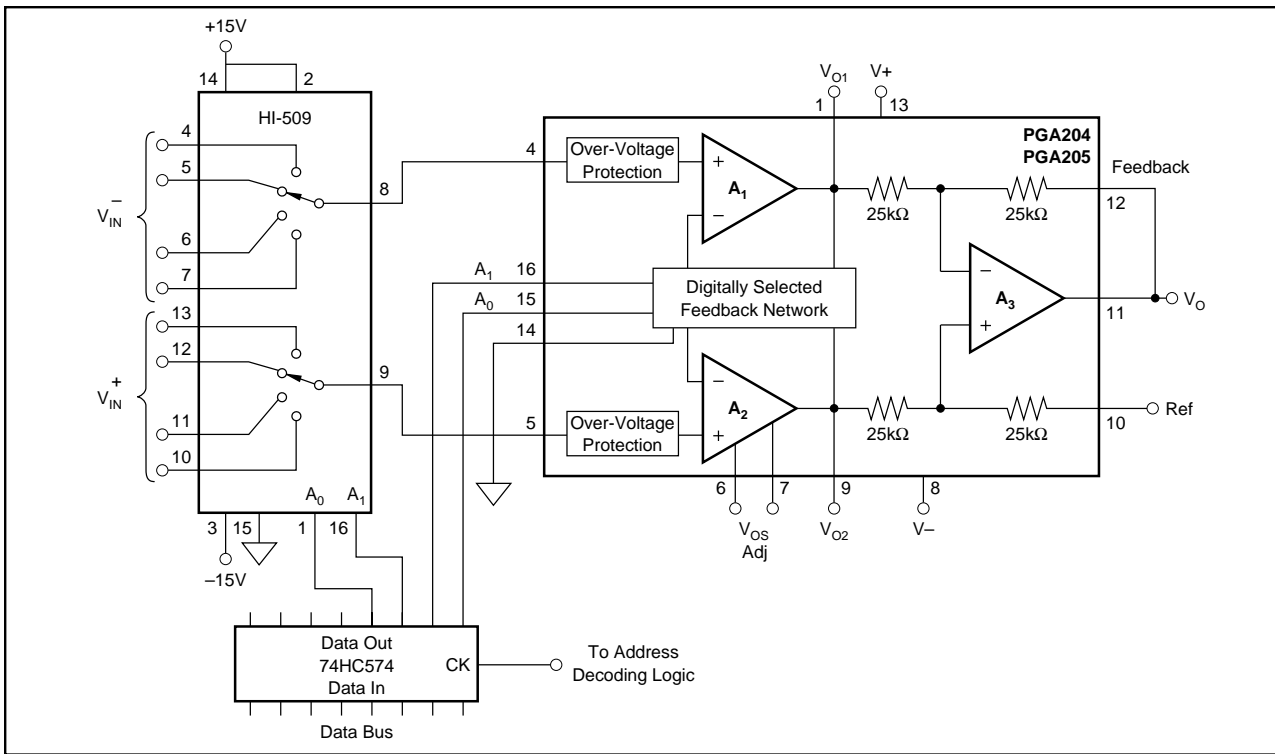


FIGURE 7. Multiplexed-Input Programmable Gain IA.

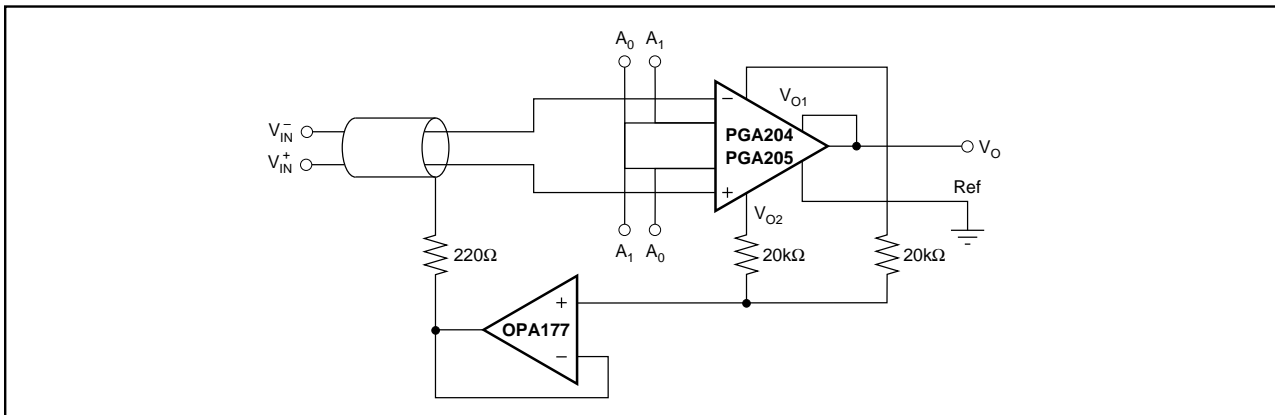


FIGURE 8. Shield Drive Circuit.

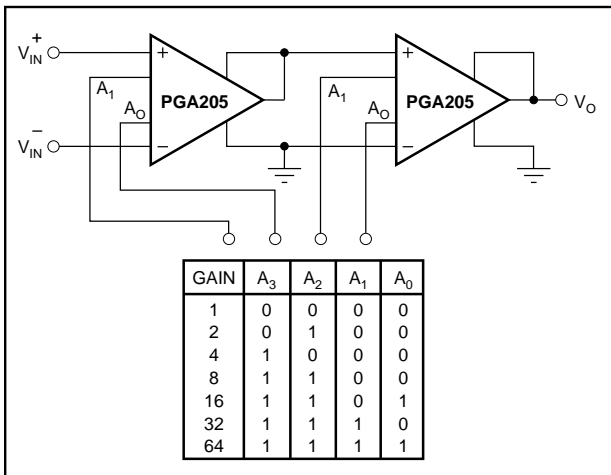


FIGURE 9. Binary Gain Steps, G=1 to G=64.

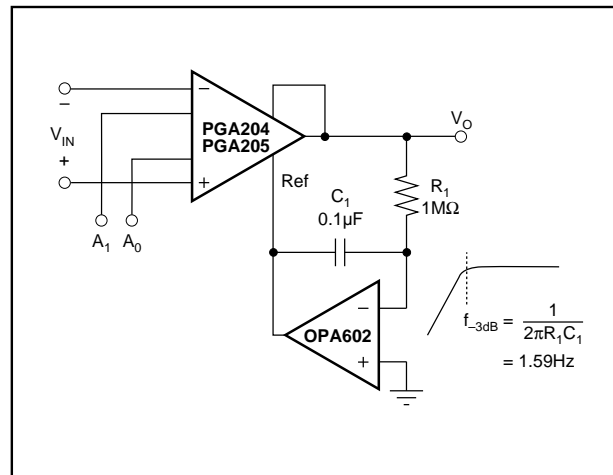


FIGURE 10. AC-Coupled PGIA.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
PGA204AP	ACTIVE	PDIP	N	16	25	None	Call TI	Level-NA-NA-NA
PGA204AU	ACTIVE	SOIC	DW	16	48	None	CU SNPB	Level-3-220C-168 HR
PGA204AU/1K	ACTIVE	SOIC	DW	16	1000	None	CU SNPB	Level-3-220C-168 HR
PGA204BP	ACTIVE	PDIP	N	16	25	None	Call TI	Level-NA-NA-NA
PGA204BU	ACTIVE	SOIC	DW	16	48	None	CU SNPB	Level-3-220C-168 HR
PGA204BU/1K	ACTIVE	SOIC	DW	16	1000	None	CU SNPB	Level-3-220C-168 HR
PGA205AP	ACTIVE	PDIP	N	16	25	None	Call TI	Level-NA-NA-NA
PGA205AU	ACTIVE	SOIC	DW	16	48	None	CU SNPB	Level-3-260C-168 HR
PGA205AU/1K	ACTIVE	SOIC	DW	16	1000	None	CU SNPB	Level-3-260C-168 HR
PGA205BP	ACTIVE	PDIP	N	16	25	None	Call TI	Level-NA-NA-NA
PGA205BU	ACTIVE	SOIC	DW	16	48	None	CU SNPB	Level-3-260C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265