

SN54164, SN54LS164, SN74164, SN74LS164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

MARCH 1974 — REVISED MARCH 1988

- Gated Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear

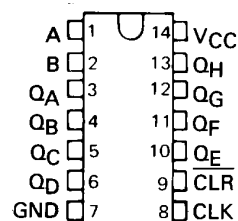
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'164	36 MHz	21 mW per bit
'LS164	36 MHz	10 mW per bit

description

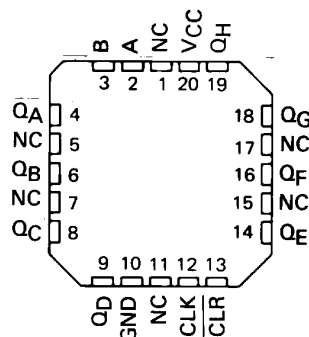
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup-time requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

The SN54164 and SN54LS164 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74164 and SN74LS164 are characterized for operation from 0°C to 70°C .

SN54164, SN54LS164 . . . J OR W PACKAGE
SN74164 . . . N PACKAGE
SN74LS164 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS164 . . . FK PACKAGE
(TOP VIEW)



NC — No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	QA	QB . . . QH	
L	X	X	X	L	L	L
H	L	X	X	QA0	QB0	QH0
H	↑	H	H	H	QAn	QGn
H	↑	L	X	L	QAn	QGn
H	↑	X	L	L	QAn	QGn

H = high level (steady state), L = low level (steady state)

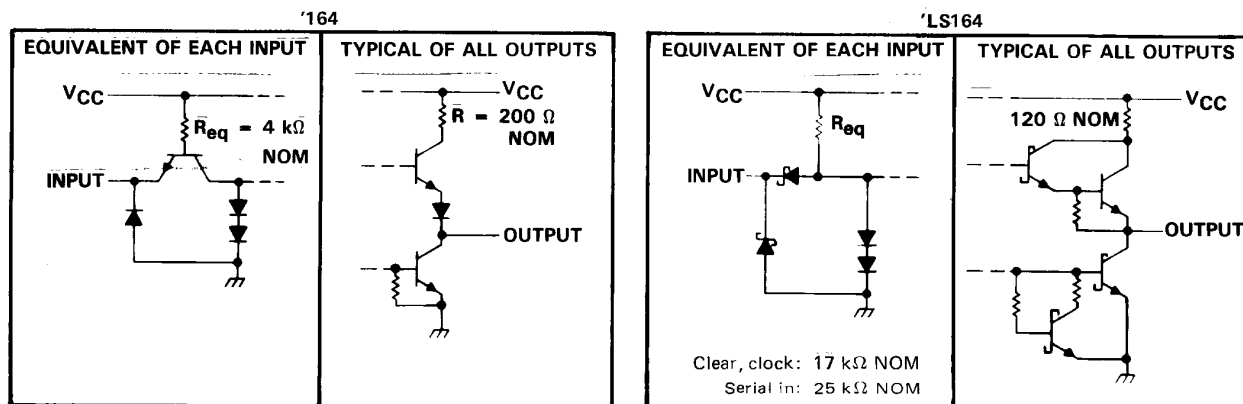
X = irrelevant (any input, including transitions)

↑ = transition from low to high level.

QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.

QAn, QGn = the level of QA or QG before the most-recent ↑ transition of the clock; indicates a one-bit shift.

schematics of inputs and outputs

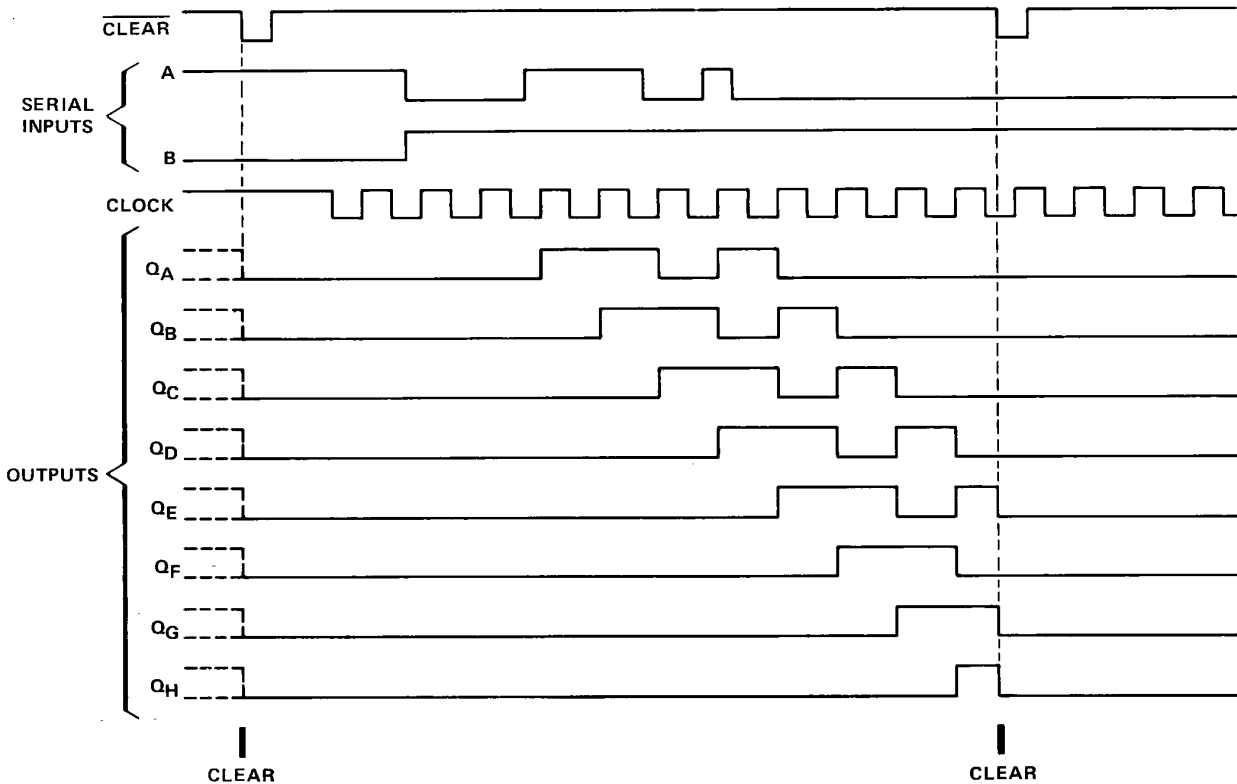


TEXAS
INSTRUMENTS

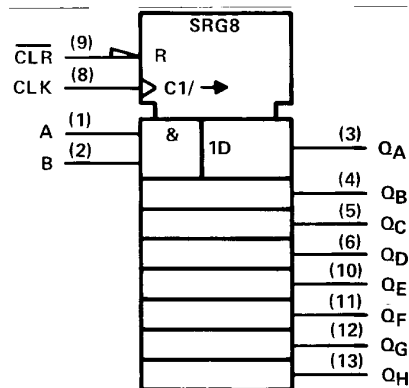
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SN54164, SN54LS164, SN74164, SN74LS164 **8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS**

typical clear, shift, and clear sequences



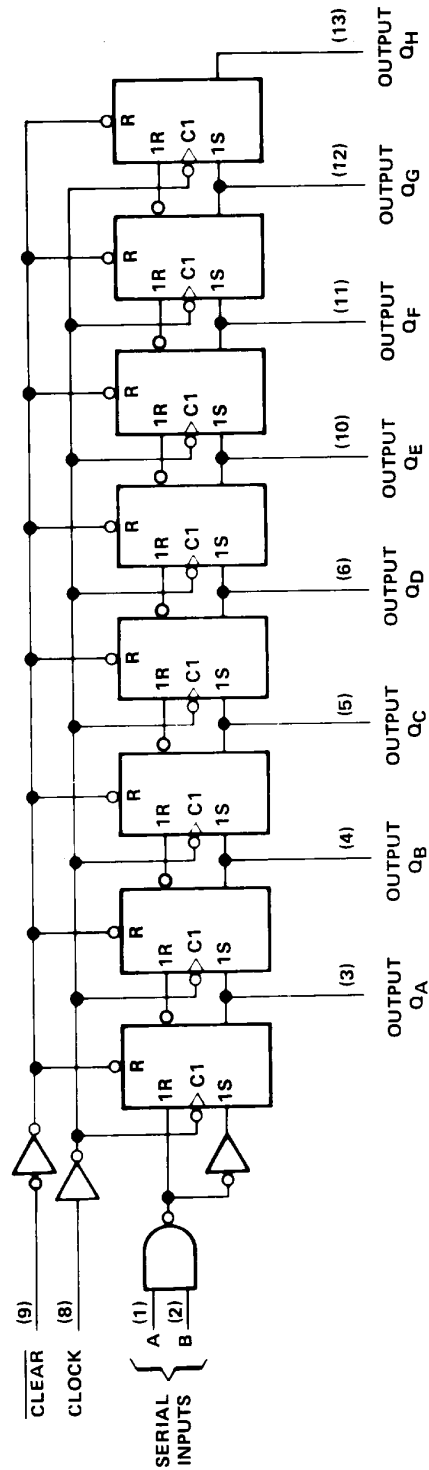
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

SN54164, SN54LS164, SN74164, SN74LS164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

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TTL Devices

SN54164, SN74164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54164	–55°C to 125°C
SN74164	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54164			SN74164			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–400			–400	μ A
Low-level output current, I_{OL}			8			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear input pulse, t_W	20			20			ns
Data setup time, t_{SU} (see Figure 1)	15			15			ns
Data setup time, t_{SU} (Clear Inactive) (see Figure 1)	20			20			ns
Data hold time, t_H (see Figure 1)	5			5			ns
Operating free-air temperature, T_A	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54164			SN74164			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			–1.5			–1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$	2.4	3.2		2.4	3.2		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 8 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V},$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–1.6			–1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	–10		–27.5	–9		–27.5	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, V_I(\text{clock}) = 0.4 \text{ V}$		30			30		mA
	See Note 2 $V_I(\text{clock}) = 2.4 \text{ V}$		37	54		37	54	

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than two outputs should be shorted at a time.

NOTE 2: I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}$	25	36		MHz
t_{PHL} Propagation delay time, high-to-low-level Q outputs from clear input	$C_L = 15 \text{ pF}$		24	36	ns
	$C_L = 50 \text{ pF}$		28	42	
t_{PLH} Propagation delay time, low-to-high-level Q outputs from clock input	$C_L = 15 \text{ pF}$	8	17	27	ns
	$C_L = 50 \text{ pF}$	10	20	30	
t_{PHL} Propagation delay time, high-to-low-level Q outputs from the clock input	$C_L = 15 \text{ pF}$	10	21	32	ns
	$C_L = 50 \text{ pF}$	10	25	37	

SN54LS164, SN74LS164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS164	–55°C to 125°C
SN74LS164	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS164			SN74LS164			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0		25	0		25	MHz
t_w	Width of clock or clear input pulse	20			20			ns
t_{su}	Data setup time (See Figure 1)	15			15			ns
t_{su}	Clear inactive setup time (See Figure 1)	20			20			ns
t_h	Data hold time (See Figure 1)	5			5			ns
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS164		SN74LS164		UNIT
			MIN	TYP‡	MAX	MIN	
V _{IK}	V _{CC} = MIN, I _I = –18 mA		–1.5		–1.5		V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = –0.4 mA		2.5	3.5	2.7	3.5	V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 4 mA	0.25	0.4	0.25	0.4	V
		I _{OL} = 8 mA			0.35	0.5	
I _I	V _{CC} = MAX, V _I = 7 V		0.1		0.1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V		20		20		μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V		–0.4		–0.4		mA
I _{OS}	V _{CC} = MAX		–20	–100	–20	–100	mA
I _{CC}	V _{CC} = MAX, See Note 3		16	27	16	27	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3: I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied to clear.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		25	36		MHz
t_{PHL} Propagation delay time, high-to-low-level Q outputs from clear input	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF},$		24	36	ns
t_{PLH} Propagation delay time, low-to-high-level Q outputs from clock input	See Figure 1		17	27	ns
t_{PHL} Propagation delay time, high-to-low-level Q outputs from clock input			21	32	ns

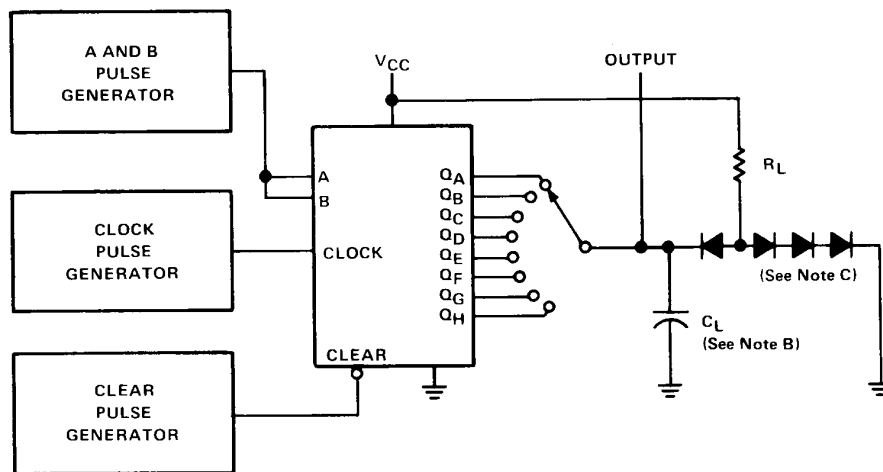
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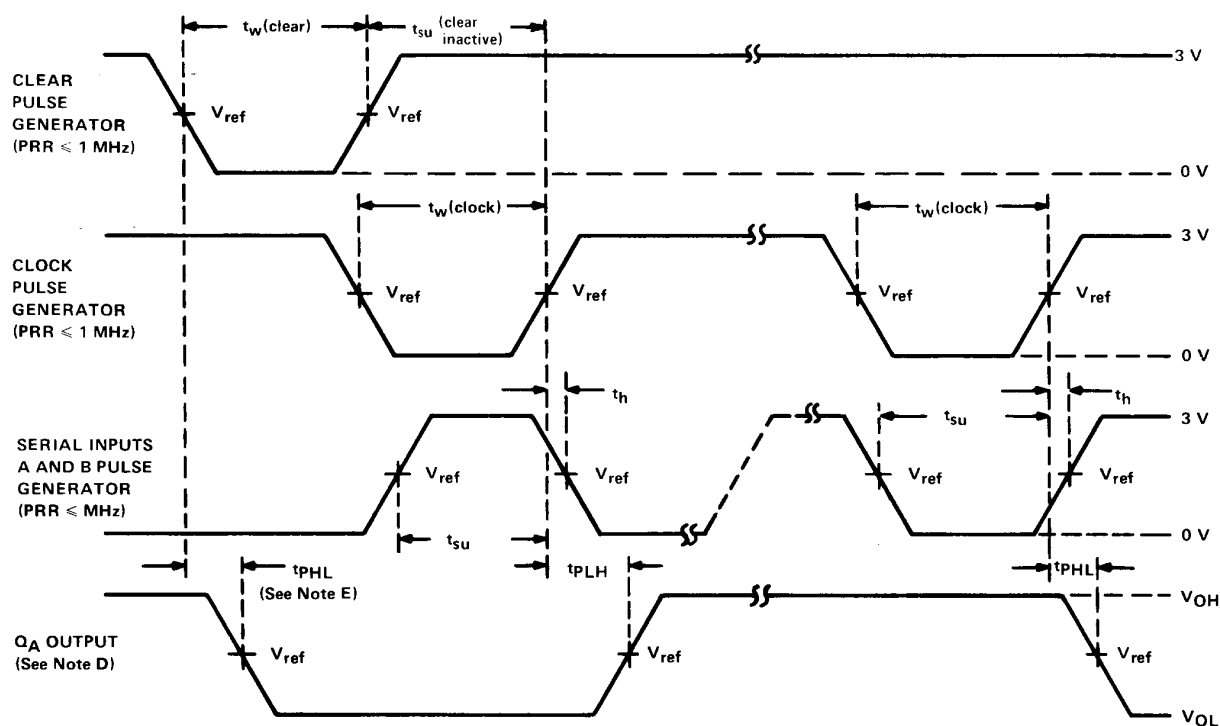
SN54164, SN54LS164, SN74164, SN74LS164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generators have the following characteristics: duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$; for '164, $t_r \leq 10$ ns, $t_f \leq 10$ ns; and for 'LS164, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
- E. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
- F. For '164, $V_{ref} = 1.5$ V; for 'LS164, $V_{ref} = 1.3$ V.

FIGURE 1—SWITCHING TIMES

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