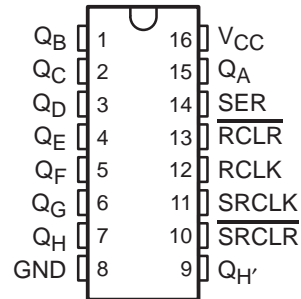


# SN54AHC594, SN74AHC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

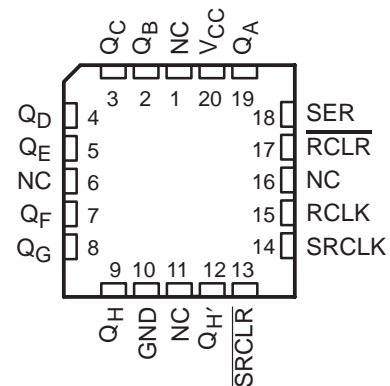
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- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Operating Range 2-V to 5.5-V  $V_{CC}$**
- **8-Bit Serial-In, Parallel-Out Shift Registers With Storage**
- **Independent Direct Overriding Clears on Shift and Storage Registers**
- **Independent Clocks for Shift and Storage Registers**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

SN54AHC594 . . . J OR W PACKAGE  
SN74AHC594 . . . D, DB, N, OR PW PACKAGE  
(TOP VIEW)



SN54AHC594 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

The 'AHC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear ( $\overline{SRCLR}$ ,  $\overline{RCLR}$ ) inputs are provided on the shift and storage registers. A serial ( $Q_{H^r}$ ) output is provided for cascading purposes.

The shift register (SRCLK) and storage register (RCLK) clocks are positive-edge triggered. If the clocks are tied together, the shift register always is one clock pulse ahead of the storage register.

The SN54AHC594 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AHC594 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .



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 **TEXAS  
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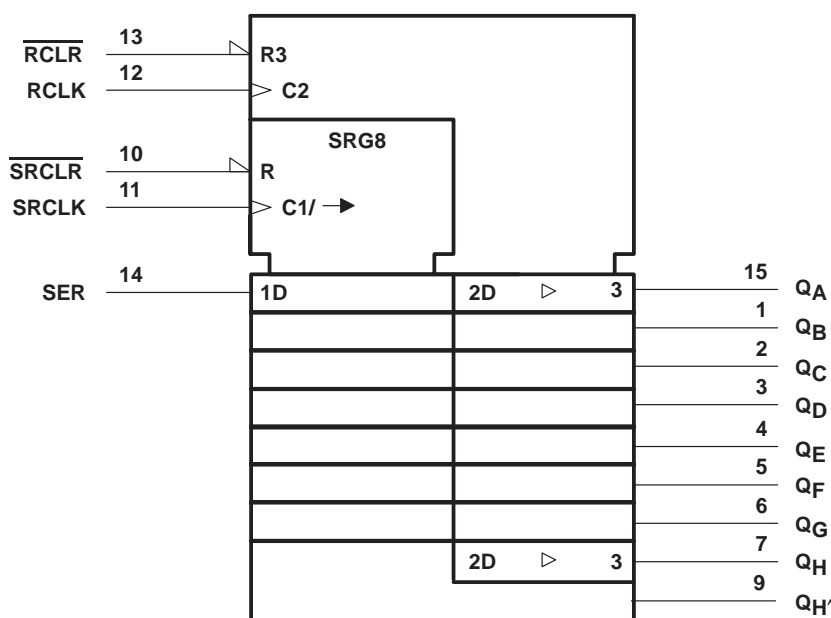
# SN54AHC594, SN74AHC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	RCLR	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

## logic symbol†

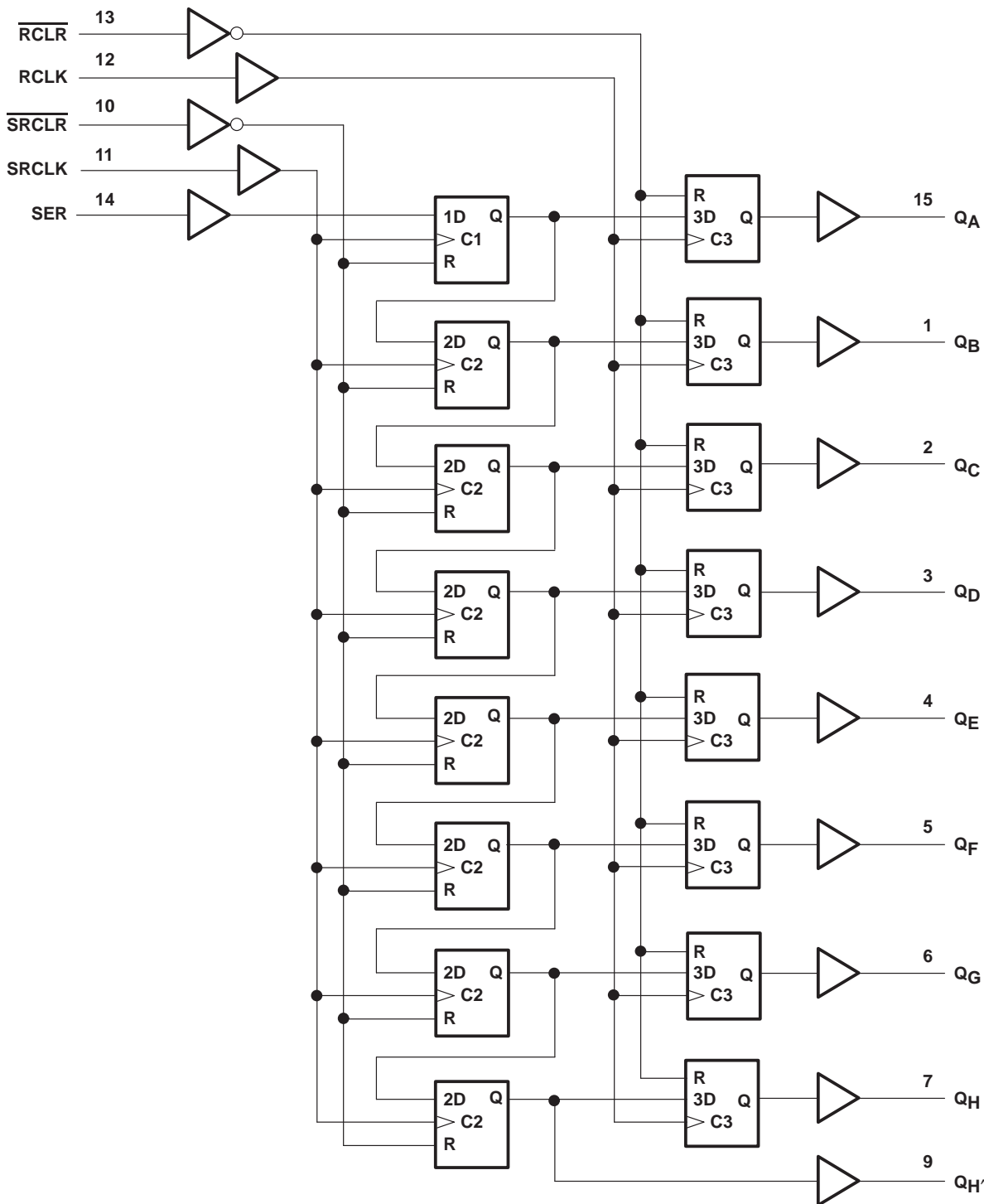


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, N, PW, and W packages.

# SN54AHC594, SN74AHC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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## logic diagram (positive logic)

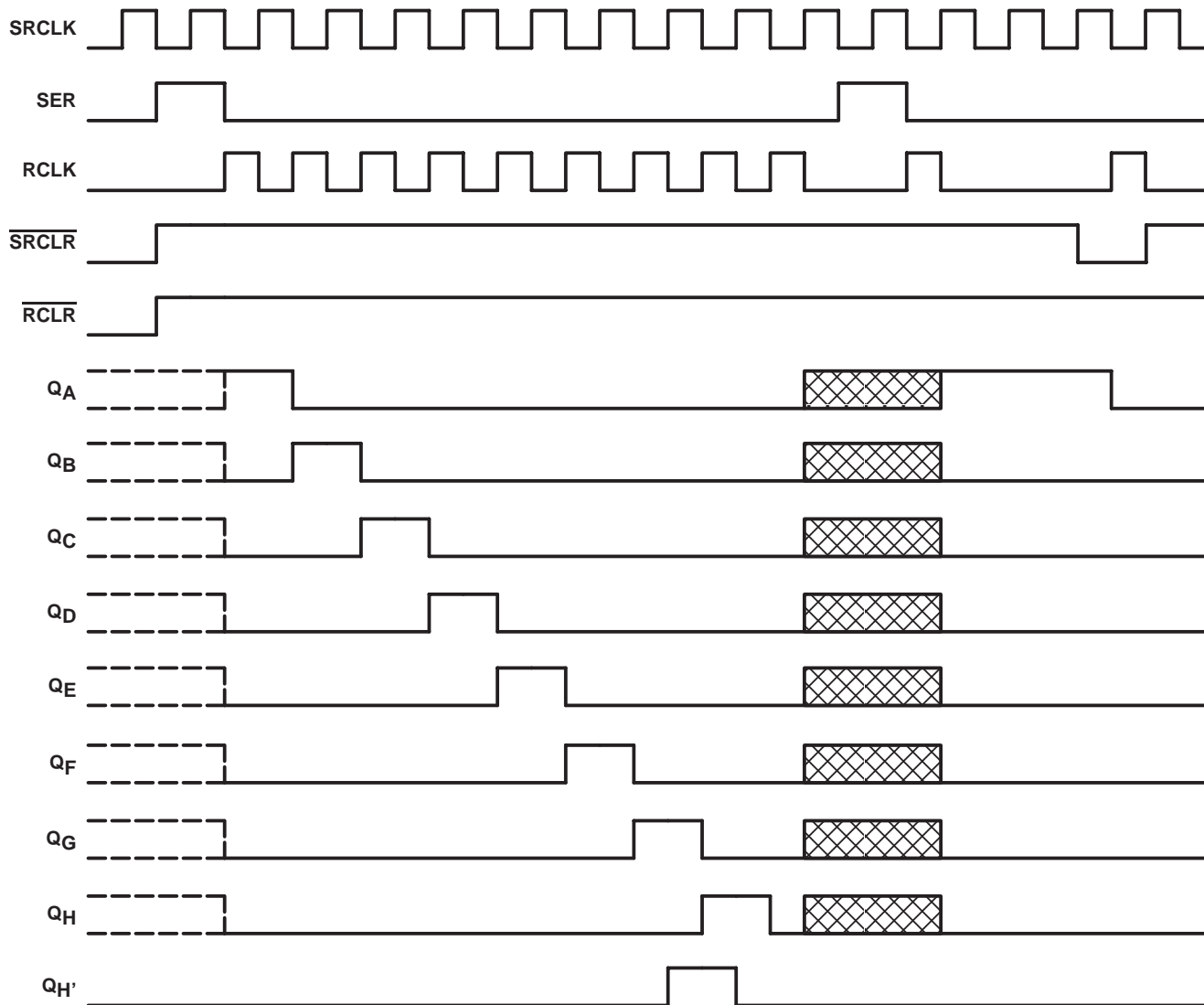


Pin numbers shown are for the D, DB, J, N, PW, and W packages.

# SN54AHC594, SN74AHC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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## timing diagram



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	73°C/W
DB package	82°C/W
N package	67°C/W
PW package	108°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

**recommended operating conditions (see Note 3)**

		SN54AHC594		SN74AHC594		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2	5.5	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	1.5		V
		$V_{CC} = 3$ V	2.1	2.1		
		$V_{CC} = 5.5$ V	3.85	3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	0.5		V
		$V_{CC} = 3$ V	0.9	0.9		
		$V_{CC} = 5.5$ V	1.65	1.65		
$V_I$	Input voltage	0	5.5	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	–50	–50		µA
		$V_{CC} = 3.3$ V ± 0.3 V	–4	–4		mA
		$V_{CC} = 5$ V ± 0.5 V	–8	–8		
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	50		µA
		$V_{CC} = 3.3$ V ± 0.3 V	4	4		mA
		$V_{CC} = 5$ V ± 0.5 V	8	8		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V	100	100		ns/V
		$V_{CC} = 5$ V ± 0.5 V	20	20		
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54AHC594, SN74AHC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC594		SN74AHC594		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		2.48		
	Q <sub>H</sub> , I <sub>OH</sub> = -4 mA	4.5 V	3.94			3.8		3.8		
Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OH</sub> = -8 mA		4.5 V	3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1		0.1	0.1	V	
		3 V			0.1		0.1	0.1		
		4.5 V			0.1		0.1	0.1		
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.5	0.44		
	Q <sub>H</sub> , I <sub>OL</sub> = 4 mA	4.5 V			0.36		0.5	0.44		
Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OL</sub> = 8 mA		4.5 V			0.36		0.5	0.44		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			± 0.1		± 1*	± 1	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	40	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			2		10	10	pF	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T <sub>A</sub> = 25°C		SN54AHC594		SN74AHC594		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	RCLK or SRCLK high or low	5.5		5.5		5.5		ns
		RCLR or SRCLR low	5		5		5		
t <sub>su</sub>	Setup time	SER before SRCLK↑	3.5		3.5		3.5		ns
		SRCLK↑ before RCLK↑†	8		8.5		8.5		
		SRCLR low before RCLK↑	8		9		9		
		SRCLR high (inactive) before SRCLK↑	4.2		4.8		4.8		
		RCLR high (inactive) before RCLK↑	4.6		5.3		5.3		
t <sub>h</sub>	Hold time	SER after SRCLK↑	1.5		1.5		1.5		ns

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

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# SN54AHC594, SN74AHC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54AHC594		SN74AHC594		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	RCLK or SRCLK high or low	5		5		5		ns
		$\overline{\text{RCLR}}$ or $\overline{\text{SRCLR}}$ low	5.2		5.2		5.2		
$t_{su}$	Setup time	SER before SRCLK $\uparrow$	3		3		3		ns
		SRCLK $\uparrow$ before RCLK $\uparrow$ $\dagger$	5		5		5		
		$\overline{\text{SRCLR}}$ low before RCLK $\uparrow$	5		5		5		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK $\uparrow$	2.9		3.3		3.3		
		RCLR high (inactive) before RCLK $\uparrow$	3.2		3.7		3.7		
$t_h$	Hold time	SER after SRCLK $\uparrow$	2		2		2		ns

$\dagger$  This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC594		SN74AHC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			$C_L = 15\text{ pF}$	80*	120*		70*		70		MHz
			$C_L = 50\text{ pF}$	55	105		50		50		
$t_{PLH}$	RCLK	$Q_A-Q_H$	$C_L = 15\text{ pF}$	4.6*	8*		1*	8.5*	1	8.5	ns
$t_{PHL}$				4.9*	8.2*		1*	8.8*	1	8.8	
$t_{PLH}$	SRCLK	$Q_H'$	$C_L = 15\text{ pF}$	5.4*	9.1*		1*	9.7*	1	9.7	ns
$t_{PHL}$				5.5*	9.2*		1*	9.9*	1	9.9	
$t_{PHL}$	$\overline{\text{RCLR}}$	$Q_A-Q_H$	$C_L = 15\text{ pF}$	6*	9.8*		1*	10.6*	1	10.6	ns
$t_{PHL}$	$\overline{\text{SRCLR}}$	$Q_H'$	$C_L = 15\text{ pF}$	5.6*	9.2*		1*	10*	1	10	ns
$t_{PLH}$	RCLK	$Q_A-Q_H$	$C_L = 50\text{ pF}$	6.9	10.5		1	11.1	1	11.1	ns
$t_{PHL}$				8.1	11.9		1	13.1	1	13.1	
$t_{PLH}$	SRCLK	$Q_H'$	$C_L = 50\text{ pF}$	7.7	11.7		1	12.4	1	12.4	ns
$t_{PHL}$				8.4	12.5		1	13.9	1	13.9	
$t_{PHL}$	$\overline{\text{RCLR}}$	$Q_A-Q_H$	$C_L = 50\text{ pF}$	9.1	13.1		1	14.4	1	14.4	ns
$t_{PHL}$	$\overline{\text{SRCLR}}$	$Q_H'$	$C_L = 50\text{ pF}$	8.5	12.4		1	14	1	14	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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# SN54AHC594, SN74AHC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC594		SN74AHC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			$C_L = 15\text{ pF}$	135*	170*		115*		115		MHz
			$C_L = 50\text{ pF}$	120	140		95		95		
$t_{PLH}$	RCLK	$Q_A-Q_H$	$C_L = 15\text{ pF}$		3.3*	6.2*	1*	6.5*	1	6.5	ns
$t_{PHL}$					3.7*	6.5*	1*	6.9*	1	6.9	
$t_{PLH}$	SRCLK	$Q_H$	$C_L = 15\text{ pF}$		3.7*	6.8*	1*	7.2*	1	7.2	ns
$t_{PHL}$					4.1*	7.2*	1*	7.6*	1	7.6	
$t_{PHL}$	$\overline{\text{RCLR}}$	$Q_A-Q_H$	$C_L = 15\text{ pF}$		4.5*	7.6*	1*	8.2*	1	8.2	ns
$t_{PHL}$	$\overline{\text{SRCLR}}$	$Q_H$	$C_L = 15\text{ pF}$		4.1*	7.1*	1*	7.6*	1	7.6	ns
$t_{PLH}$	RCLK	$Q_A-Q_H$	$C_L = 50\text{ pF}$		4.9	7.8	1	8.3	1	8.3	ns
$t_{PHL}$					5.8	8.9	1	9.7	1	9.7	
$t_{PLH}$	SRCLK	$Q_H$	$C_L = 50\text{ pF}$		5.5	8.6	1	9.1	1	9.1	ns
$t_{PHL}$					6	9.2	1	10.1	1	10.1	
$t_{PHL}$	$\overline{\text{RCLR}}$	$Q_A-Q_H$	$C_L = 50\text{ pF}$		6.6	10	1	10.7	1	10.7	ns
$t_{PHL}$	$\overline{\text{SRCLR}}$	$Q_H$	$C_L = 50\text{ pF}$		6	9.2	1	10.1	1	10.1	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER	SN74AHC594			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		1		V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		-0.6		V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		3.8		V
$V_{IH(D)}$ High-level dynamic input voltage		3.5		V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

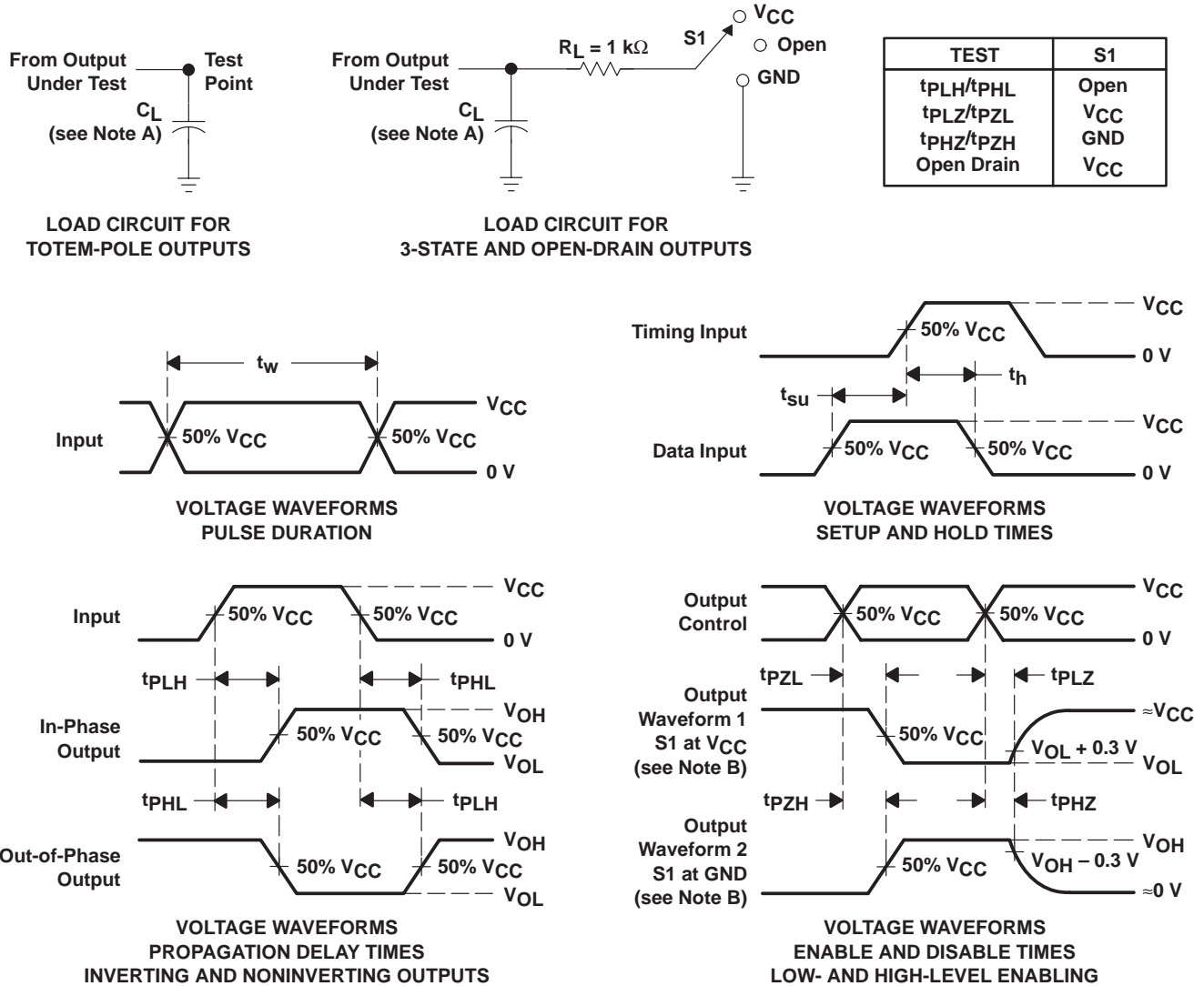
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	112	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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