

The SN5405 is obsolete and no longer is supplied.

# SN54LS05, SN54S05 SN7405, SN74LS05, SN74S05 HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

SDLS030A – DECEMBER 1983 – REVISED NOVEMBER 2003

- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

- Dependable Texas Instrument Quality and Reliability

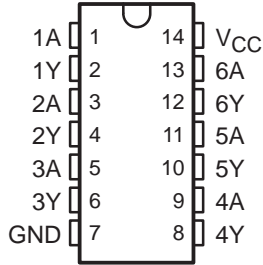
SN5405, SN54LS05, SN54S05 . . . J PACKAGE

SN7405 . . . N PACKAGE

SN74LS05 . . . D, DB, N, OR NS PACKAGE

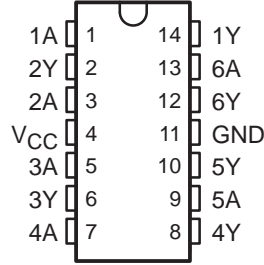
SN74S05 . . . D, N, OR NS PACKAGE

(TOP VIEW)



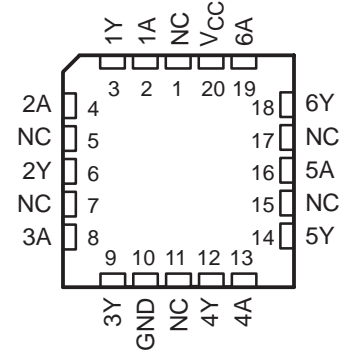
SN54LS05, SN54S05 . . . W PACKAGE

(TOP VIEW)



SN54LS05, SN54S05 . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection

## description/ordering information

These devices contain six independent inverters. To perform correctly, the open-collector outputs require pullup resistors. These devices may be connected to other open-collector outputs to implement active-low wired-OR or active-high wire-AND functions. Open-collector devices often are used to generate high  $V_{OH}$  levels.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	PDIP – N	Tube	SN7405N	SN7405N	
			SN74LS05N	SN74LS05N	
			SN74S05N	SN74S05N	
	SOIC – D	Tube	SN74LS05D	LS05	
			Tape and reel		SN74LS05DR
			Tube	SN74S05D	S05
				Tape and reel	
SOP – NS	Tape and reel	SN74LS05NSR	74LS05		
		SN74S05NSR	74S05		
–55°C to 125°C	CDIP – J	Tube	SNJ54LS05J	SNJ54LS05J	
			SNJ54S05J	SNJ54S05J	
	CDIP – W	Tube	SNJ54LS05W	SNJ54LS05W	
			SNJ54S05W	SNJ54S05W	
	LCCC – FK	Tube	SNJ54LS05FK	SNJ54LS05FK	
SNJ54S05FK			SNJ54S05FK		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54LS05, SN54S05**  
**SN7405, SN74LS05, SN74S05**  
**HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS**

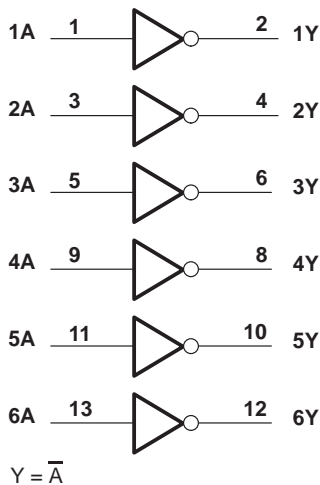
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FUNCTION TABLE  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, and NS packages.



**SN54LS05, SN54S05  
SN7405, SN74LS05, SN74S05  
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS**

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**recommended operating conditions**

	SN5405			SN7405			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.8			0.8	V
V <sub>OH</sub> High-level output voltage			5.5			5.5	V
I <sub>OL</sub> Low-level output current			16			16	mA
T <sub>A</sub> Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN5405			SN7405			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5			-1.5	V
I <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>OH</sub> = 5.5 V V <sub>IL</sub> = 0.8 V V <sub>IL</sub> = 0.7 V						0.25	mA
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA		0.2	0.4		0.2	0.4	V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V			40			40	µA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-1.6			-1.6	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V		6	12		6	12	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V		18	33		18	33	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A	Y	R <sub>L</sub> = 4 kΩ	C <sub>L</sub> = 15 pF		40	55	ns
t <sub>PHL</sub>			R <sub>L</sub> = 400 Ω			8	15	



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**SN54LS05, SN54S05**  
**SN7405, SN74LS05, SN74S05**  
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**recommended operating conditions**

		SN54LS05			SN74LS05			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage				0.7			V
V <sub>OH</sub>	High-level output voltage				5.5			V
I <sub>OL</sub>	Low-level output current				4			mA
T <sub>A</sub>	Operating free-air temperature	-55			125			°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN54LS05			SN74LS05			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA				-1.5			V	
I <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>OH</sub> = 5.5 V				0.1			mA	
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V				0.25	0.4	0.25	0.4	V
								0.35	
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V				0.1			mA	
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V				20			μA	
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V				-0.4			mA	
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V				1.2	2.4	1.2	2.4	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V				3.6	6.6	3.6	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A	Y	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF			17	32
t <sub>PHL</sub>						15	28



**SN54LS05, SN54S05  
SN7405, SN74LS05, SN74S05  
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The SN5405 is obsolete  
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**recommended operating conditions**

	SN54S05			SN74S05			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.8			0.8	V
V <sub>OH</sub> High-level output voltage			5.5			5.5	V
I <sub>OL</sub> Low-level output current			20			20	mA
T <sub>A</sub> Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†		SN54S05			SN74S05			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA			-1.2			-1.2	V
I <sub>OH</sub>	V <sub>CC</sub> = MIN,	V <sub>OH</sub> = 5.5 V					0.25		mA
		V <sub>IL</sub> = 0.8 V							
		V <sub>IL</sub> = 0.7 V			0.25				
V <sub>OL</sub>	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 20 mA			0.5			0.5	V
I <sub>I</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V			50			50	µA
I <sub>IL</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.5 V			-2			-2	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0 V		9	19.8		9	19.8	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 4.5 V		30	54		30	54	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

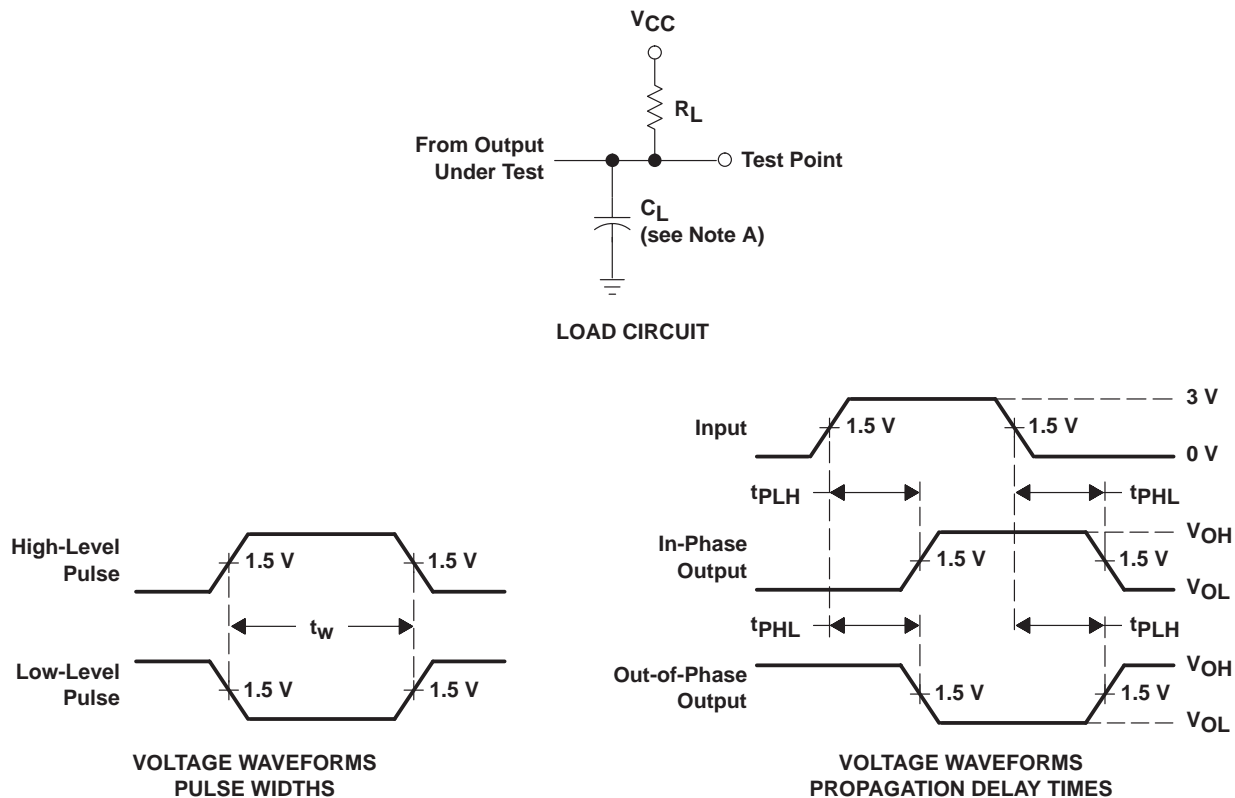
‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A	Y	R <sub>L</sub> = 280 Ω	C <sub>L</sub> = 15 pF	2	5	7.5	ns
t <sub>PHL</sub>					2	4.5	7	
t <sub>PLH</sub>				C <sub>L</sub> = 50 pF	7.5	ns		
t <sub>PHL</sub>					7			



**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54/74 AND 54S/74S DEVICES**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , and:  
 For Series 54/74,  $t_r \leq 7 \text{ ns}$ ,  $t_f \leq 7 \text{ ns}$ .  
 For Series 54S/74S,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

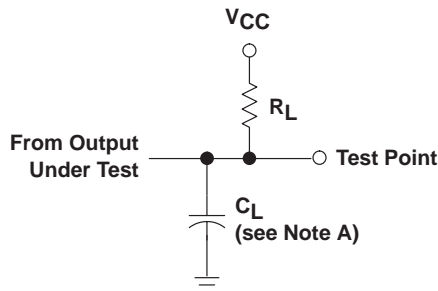
**Figure 1. Load Circuit and Voltage Waveforms**

**SN54LS05, SN54S05  
SN7405, SN74LS05, SN74S05  
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS**

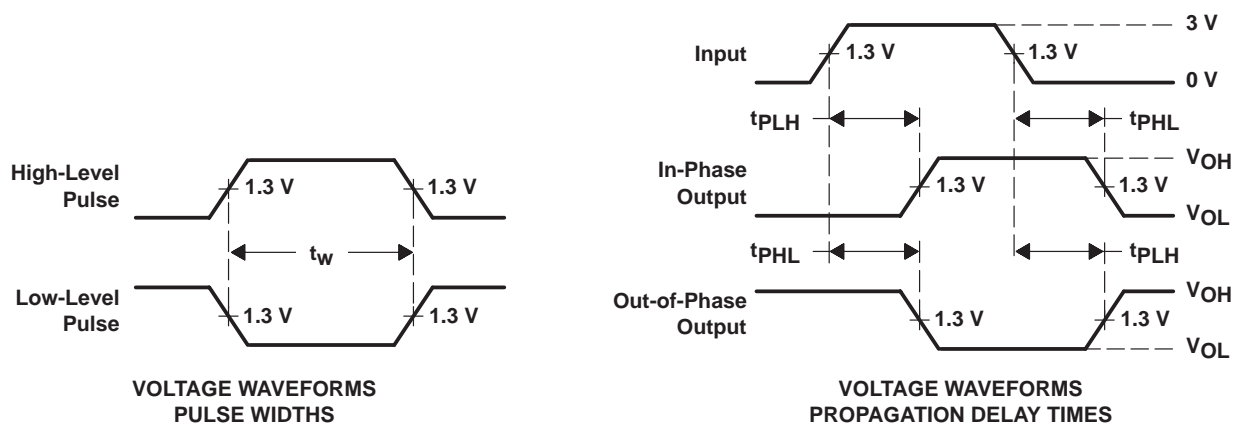
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**PARAMETER MEASUREMENT INFORMATION  
SERIES 54LS/74LS DEVICES**



**LOAD CIRCUIT**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 1.5 \text{ ns}$ ,  $t_f \leq 2.6 \text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
JM38510/07003BDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
JM38510/07004BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN54LS05J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN54S05J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN7405D	OBSOLETE	SOIC	D	14		None	Call TI	Call TI
SN7405DR	OBSOLETE	SOIC	D	14		None	Call TI	Call TI
SN7405N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN7405N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74LS05D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS05DBLE	OBSOLETE	SSOP	DB	14		None	Call TI	Call TI
SN74LS05DBR	ACTIVE	SSOP	DB	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS05DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS05N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS05N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74LS05NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74S05D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74S05DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74S05N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S05N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74S05NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ54LS05FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54LS05J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ54LS05W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SNJ54S05FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54S05J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ54S05W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

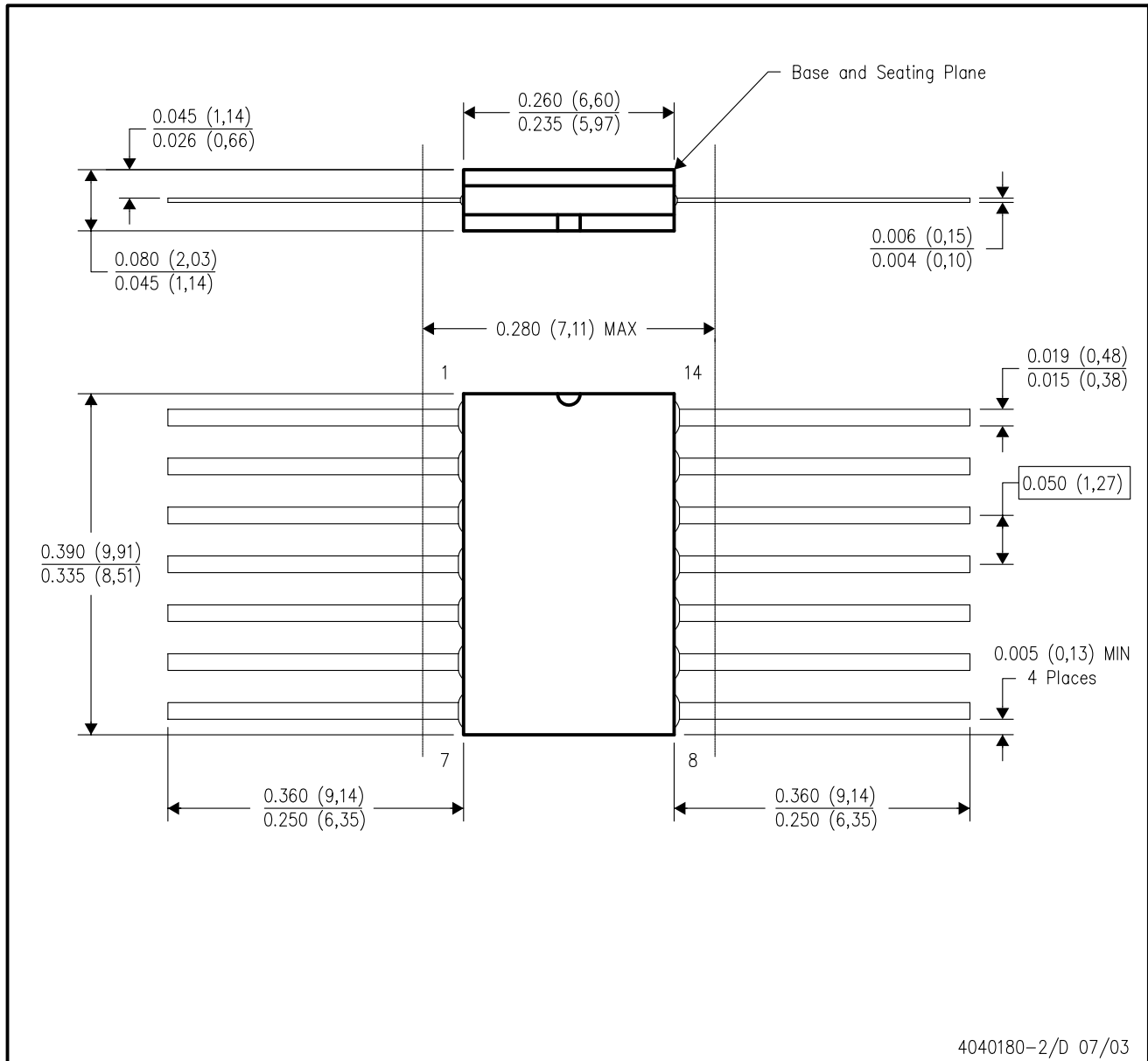


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

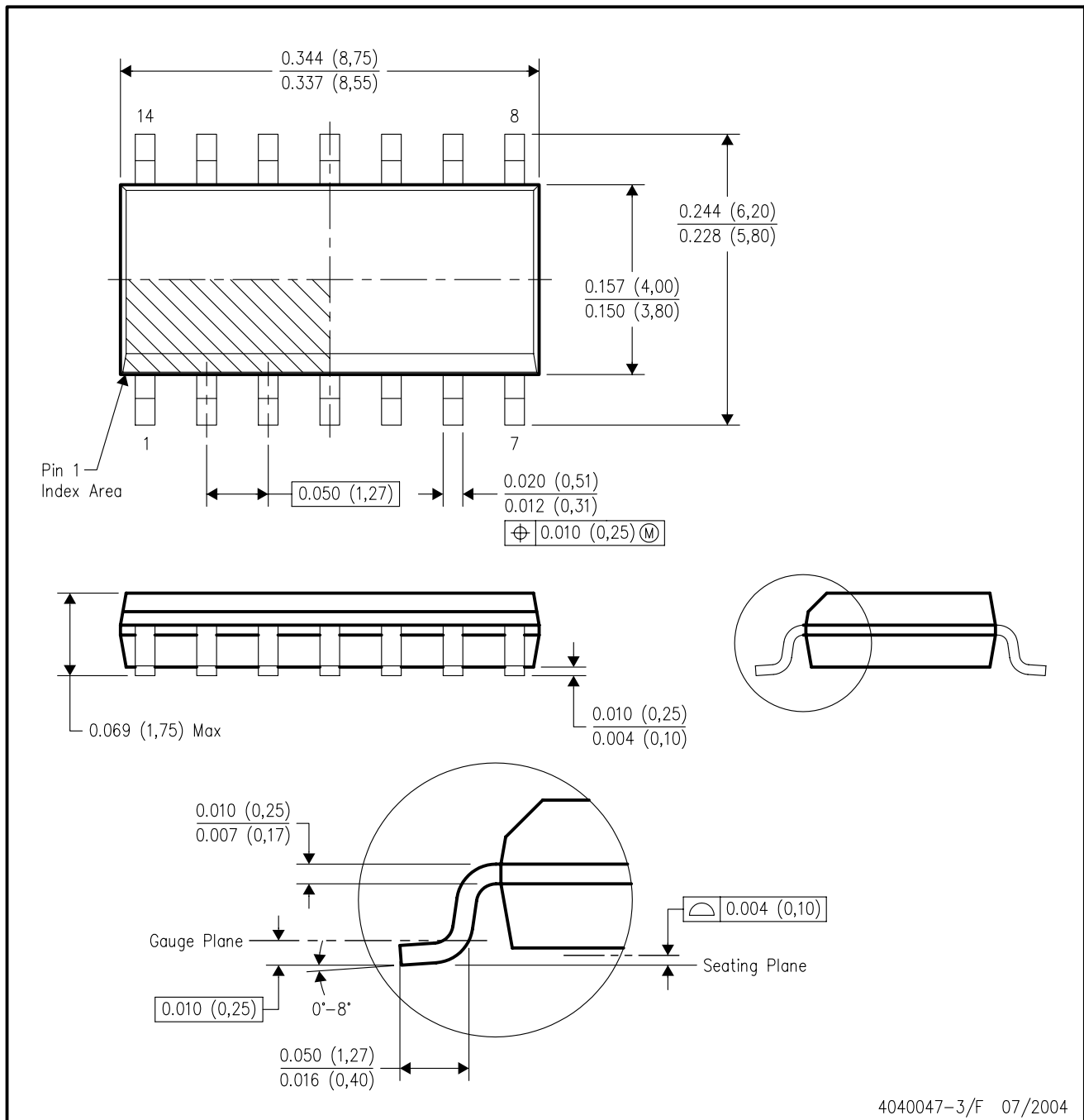


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

4040065 /E 12/01

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