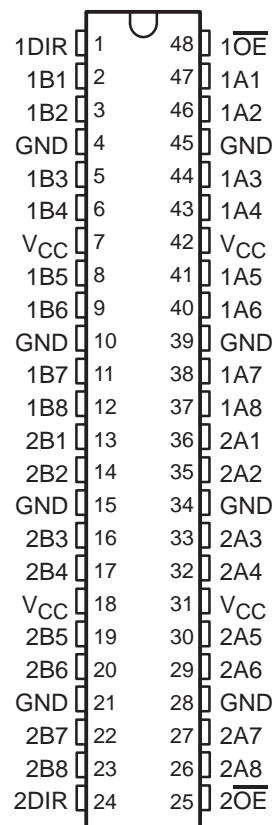


SN54LVTH162245, SN74LVTH162245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS260L – JUNE 1993 – REVISED MARCH 2000

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**
- **A-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II (SN74LVTH162245A Only)**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101) (SN74LVTH162245A Only)
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54LVTH162245 . . . WD PACKAGE
SN74LVTH162245A . . . DGG OR DL PACKAGE
(TOP VIEW)



NOTE: For tape and reel order entry:
The DGGR package is abbreviated to GR.

description

The SN54LVTH162245 and SN74LVTH162245A devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000 Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH162245, SN74LVTH162245A

3.3-V ABT 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS260L – JUNE 1993 – REVISED MARCH 2000

description (continued)

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH162245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH162245A is characterized for operation from -40°C to 85°C .

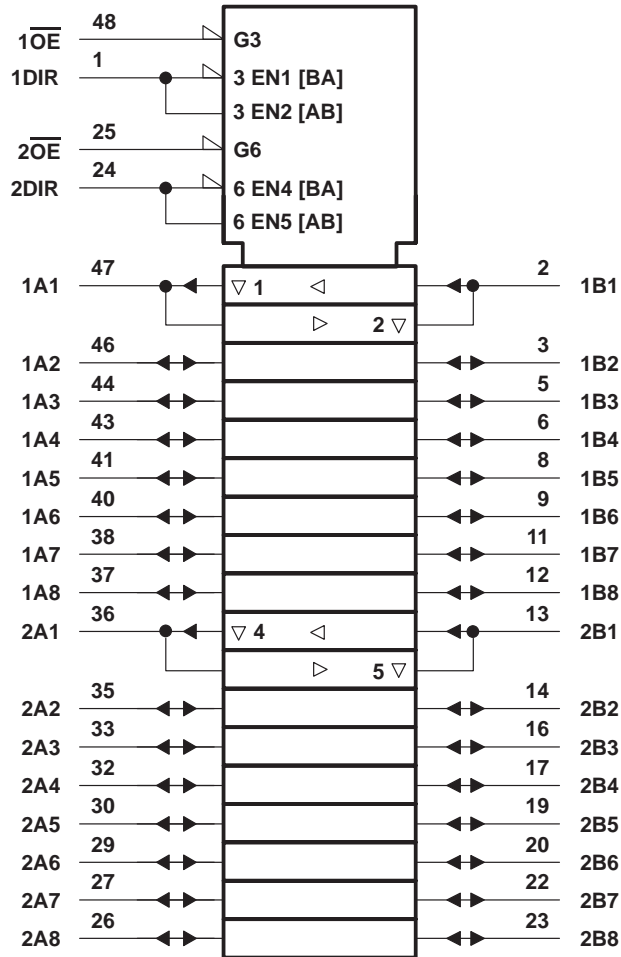
FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

SN54LVTH162245, SN74LVTH162245A
 3.3-V ABT 16-BIT BUS TRANSCEIVERS
 WITH 3-STATE OUTPUTS

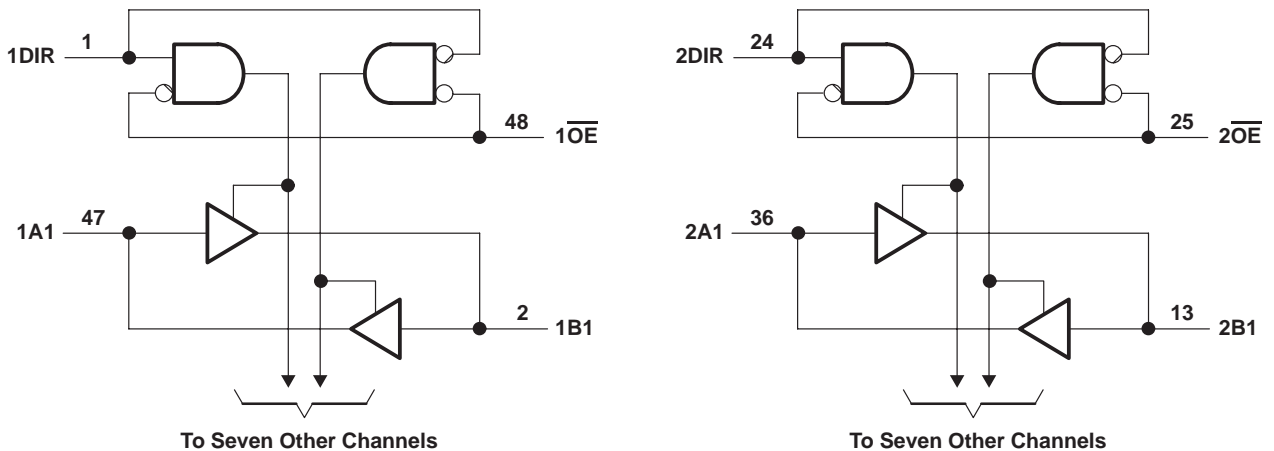
SCBS260L – JUNE 1993 – REVISED MARCH 2000

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH162245, SN74LVTH162245A

3.3-V ABT 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS260L – JUNE 1993 – REVISED MARCH 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH162245 (B port)	96 mA
SN74LVTH162245A (B port)	128 mA
A port	30 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH162245 (B port)	48 mA
SN74LVTH162245A (B port)	64 mA
A port	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	70°C/W
DL package	63°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH162245		SN74LVTH162245A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current	A port	-12		-12	mA
		B port	-24		-32	
I_{OL}	Low-level output current	A port	12		12	mA
		B port	48		64	
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μ s/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVTH162245, SN74LVTH162245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS260L – JUNE 1993 – REVISED MARCH 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH162245			SN74LVTH162245A			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}		V _{CC} = 2.7 V, I _I = -18 mA		-1.2			-1.2			V	
V _{OH}	A port	V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA		V _{CC} -0.2			V _{CC} -0.2			V	
		V _{CC} = 3 V, I _{OH} = -12 mA		2			2				
	B port	V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA		V _{CC} -0.2			V _{CC} -0.2				
		V _{CC} = 2.7 V, I _{OH} = -8 mA		2.4			2.4				
		V _{CC} = 3 V, I _{OH} = -24 mA		2							
		V _{CC} = 3 V, I _{OH} = -32 mA					2				
V _{OL}	A port	V _{CC} = 2.7 V to 3.6 V, I _{OL} = 100 μA		0.2			0.2			V	
		V _{CC} = 3 V, I _{OL} = 12 mA		0.8			0.8				
	B port	V _{CC} = 2.7 V, I _{OL} = 100 μA		0.2			0.2				
		V _{CC} = 2.7 V, I _{OL} = 24 mA		0.5			0.5				
		V _{CC} = 3 V, I _{OL} = 16 mA		0.4			0.4				
		V _{CC} = 3 V, I _{OL} = 32 mA		0.5			0.5				
		V _{CC} = 3 V, I _{OL} = 48 mA		0.55							
		V _{CC} = 3 V, I _{OL} = 64 mA					0.55				
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1			±1			μA	
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10			10				
	A or B ports‡	V _{CC} = 3.6 V, V _I = 5.5 V		20			20				
		V _{CC} = 3.6 V, V _I = V _{CC}		5			5				
		V _{CC} = 3.6 V, V _I = 0		-10			-10				
I _{off}	V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100			μA		
I _I (hold)	A or B ports	V _{CC} = 3 V, V _I = 0.8 V		75			75			μA	
		V _{CC} = 3 V, V _I = 2 V		-75			-75				
		V _{CC} = 3.6 V§, V _I = 0 to 3.6 V					±500				
I _{OZPU}	V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care		±100*			±100			μA		
I _{OZPD}	V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care		±100*			±100			μA		
I _{CC}	V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.19			0.19			mA
			Outputs low		5			5			
			Outputs disabled		0.19			0.19			
ΔI _{CC} ¶	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		0.3			0.2			mA		
C _i	V _I = 3 V or 0		4			4			pF		
C _{io}	V _O = 3 V or 0		10			10			pF		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ Unused pins at V_{CC} or GND.

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54LVTH162245, SN74LVTH162245A
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS260L – JUNE 1993 – REVISED MARCH 2000

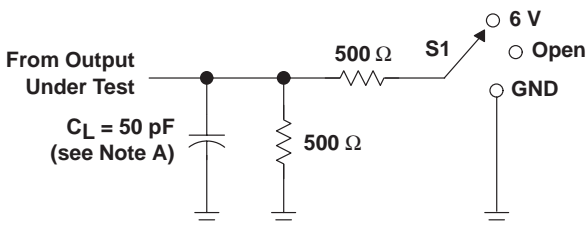
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162245				SN74LVTH162245A				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t_{PLH}	A	B	1	3.5	4		1	2.3	3.3	3.7		ns
t_{PHL}			1	3.5	3.9		1	2.2	3.3	3.5		
t_{PLH}	B	A	1	4.3	5.3		1	2.8	4	4.6		ns
t_{PHL}			1	4.2	4.5		1	2.5	3.4	3.6		
t_{PZH}	\overline{OE}	B	1	4.8	5.9		1	2.8	4.6	5.4		ns
t_{PZL}			1	4.8	5.5		1	3	4.6	5.2		
t_{PZH}	\overline{OE}	A	1	5.5	7.2		1	3.3	5.3	6.3		ns
t_{PZL}			1	5.4	6.4		1	3.3	5.1	5.8		
t_{PHZ}	\overline{OE}	B	1.5	5.5	5.8		1.5	3.8	5.2	5.5		ns
t_{PLZ}			1.5	5.5	5.8		1.5	3.5	5.1	5.4		
t_{PHZ}	\overline{OE}	A	1.5	5.8	6.5		1.5	4	5.6	5.9		ns
t_{PLZ}			1.2	6.3	6.3		1.5	3.8	5.5	5.5		
$t_{sk(o)}$								0.5			ns	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

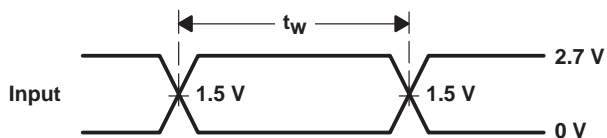


PARAMETER MEASUREMENT INFORMATION

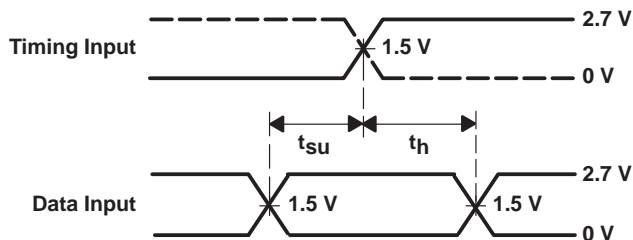


LOAD CIRCUIT

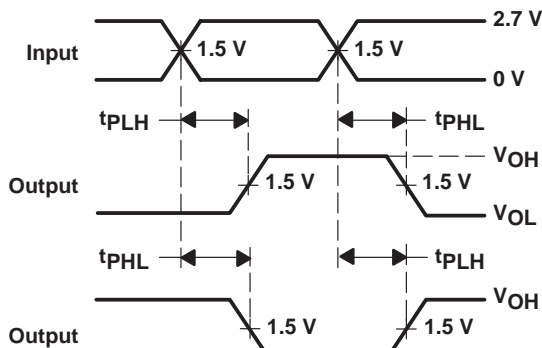
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



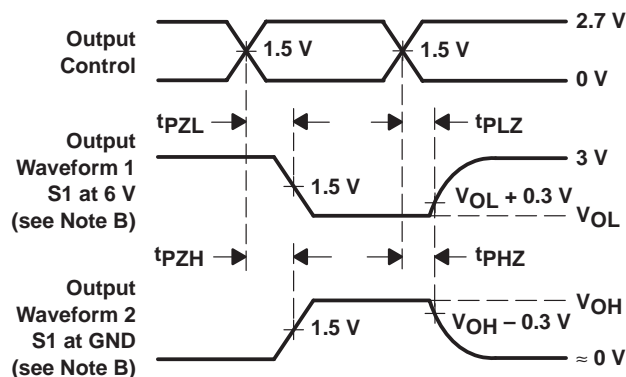
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.