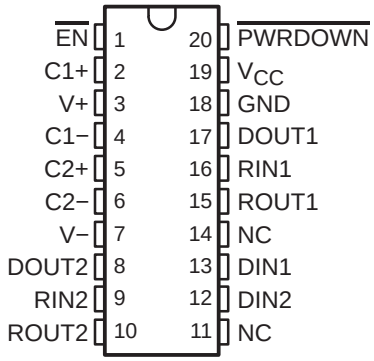
- **Operates With 3-V to 5.5-V $V_{CC}$ Supply**
- **Operates Up To 1 Mbit/s**
- **Low Standby Current . . . 1 μA Typ**
- **External Capacitors . . . 4 × 0.1 μF**
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)**
- **Applications**
  - **Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment**

**DB, DW, OR PW PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## description/ordering information

The SN65C3222 and SN75C3222 consist of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The devices provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/μs to 150 V/μs.

The SN65C3222 and SN75C3222 can be placed in the power-down mode by setting $\overline{\text{PWRDOWN}}$ low, which draws only 1 μA from the power supply. When the devices are powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled, V+ is lowered to $V_{CC}$, and V− is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting $\overline{\text{EN}}$ high.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −0°C to 70°C | SOIC (DW) | Tube of 25 | SN75C3222DW | 75C3222 |
| | | Reel of 2000 | SN75C3222DWR | |
| | SSOP (DB) | Reel of 2000 | SN75C3222DBR | CA3222 |
| | TSSOP (PW) | Tube of 70 | SN75C3222PW | CA3222 |
| | | Reel of 2000 | SN75C3222PWR | |
| −40°C to 85°C | SOIC (DW) | Tube of 25 | SN65C3222DW | 65C3222 |
| | | Reel of 2000 | SN65C3222DWR | |
| | SSOP (DB) | Reel of 2000 | SN65C3222DBR | CB3222 |
| | TSSOP (PW) | Tube of 70 | SN65C3222PW | CB3222 |
| | | Reel of 2000 | SN65C3222PWR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## Function Tables

**EACH DRIVER**

| INPUTS | | OUTPUT |
|---|---|---|
| DIN | $\overline{\text{PWRDOWN}}$ | DOUT |
| X | L | Z |
| L | H | H |
| H | H | L |

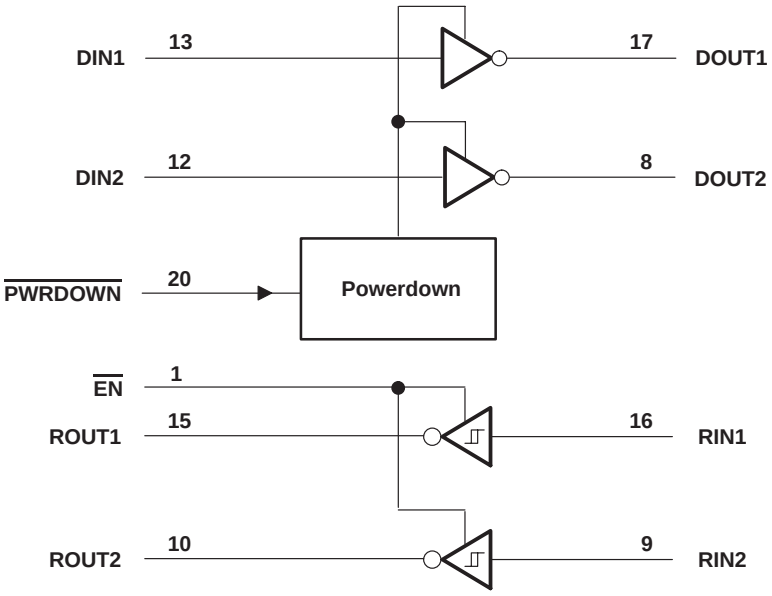
H = high level, L = low level, X = irrelevant,
Z = high impedance

**EACH RECEIVER**

| INPUTS | | OUTPUT |
|---|---|---|
| RIN | $\overline{\text{EN}}$ | ROUT |
| L | L | H |
| H | L | L |
| X | H | Z |
| Open | L | H |

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), Open = input
disconnected or connected driver off

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . −0.3 V to 6 V
Positive output supply voltage range, V+ (see Note 1) . . . . . −0.3 V to 7 V
Negative output supply voltage range, V− (see Note 1) . . . . . 0.3 V to −7 V
Supply voltage difference, V+ − V− (see Note 1) . . . . . 13 V
Input voltage range, $V_I$: Drivers, $\overline{EN}$, $\overline{PWRDOWN}$ . . . . . −0.3 V to 6 V
Receivers . . . . . −25 V to 25 V
Output voltage range, $V_O$: Drivers . . . . . −13.2 V to 13.2 V
Receivers . . . . . −0.3 V to $V_{CC}$ + 0.3 V
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
PW package . . . . . 83°C/W
Operating virtual junction temperature, $T_J$ . . . . . 150°C
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.
2. Maximum power dissipation is a function of $T_J(max)$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 4 and Figure 5)

| | | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Supply voltage | $V_{CC}$ = 3.3 V | | 3 | 3.3 | 3.6 | V |
| | | $V_{CC}$ = 5 V | | 4.5 | 5 | 5.5 | |
| $V_{IH}$ | Driver and control high-level input voltage | DIN, $\overline{EN}$, $\overline{PWRDOWN}$ | $V_{CC}$ = 3.3 V | 2 | | | V |
| | | | $V_{CC}$ = 5 V | 2.4 | | | |
| $V_{IL}$ | Driver and control low-level input voltage | DIN, $\overline{EN}$, $\overline{PWRDOWN}$ | | | | 0.8 | V |
| $V_I$ | Driver and control input voltage | DIN, $\overline{EN}$, $\overline{PWRDOWN}$ | | 0 | | 5.5 | V |
| $V_I$ | Receiver input voltage | | | −25 | | 25 | V |
| $T_A$ | Operating free-air temperature | SN65C3222 | | −40 | | 85 | °C |
| | | SN75C3222 | | 0 | | 70 | |

NOTE 4: Test conditions are C1−C4 = 0.1 µF at $V_{CC}$ = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2−C4 = 0.33 µF at $V_{CC}$ = 5 V ± 0.5 V.

### electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

| PARAMETER | | TEST CONDITIONS | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_I$ | Input leakage current ($\overline{EN}$, $\overline{PWRDOWN}$) | | | ±0.01 | ±1 | µA |
| $I_{CC}$ | Supply current | No load, $\overline{PWRDOWN}$ at $V_{CC}$ | | 0.3 | 1 | mA |
| | Supply current (powered off) | No load, $\overline{PWRDOWN}$ at GND | | 1 | 10 | µA |

‡ All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.
NOTE 4: Test conditions are C1−C4 = 0.1 µF at $V_{CC}$ = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2−C4 = 0.33 µF at $V_{CC}$ = 5 V ± 0.5 V.

## DRIVER SECTION

### electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | DOUT at $R_L$ = 3 kΩ to GND, DIN = GND | | 5 | 5.4 | | V |
| $V_{OL}$ | Low-level output voltage | DOUT at $R_L$ = 3 kΩ to GND, DIN = $V_{CC}$ | | −5 | −5.4 | | V |
| $I_{IH}$ | High-level input current | $V_I = V_{CC}$ | | | ±0.01 | ±1 | µA |
| $I_{IL}$ | Low-level input current | $V_I$ at GND | | | ±0.01 | ±1 | µA |
| $I_{OS}$ | Short-circuit output current‡ | $V_{CC}$ = 3.6 V, | $V_O$ = 0 V | | ±35 | ±60 | mA |
| | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 V | | ±35 | ±90 | |
| $r_o$ | Output resistance | $V_{CC}$, V+, and V− = 0 V, | $V_O$ = ±2 V | 300 | 10M | | Ω |
| $I_{off}$ | Output leakage current | $\overline{PWRDOWN}$ = GND | $V_O$ = ±12 V, $V_{CC}$ = 3 V to 3.6 V | | | ±25 | µA |
| | | | $V_O$ = ±10 V, $V_{CC}$ = 4.5 V to 5.5 V | | | ±25 | |

† All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.
‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.
NOTE 4: Test conditions are C1−C4 = 0.1 µF at $V_{CC}$ = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2−C4 = 0.33 µF at $V_{CC}$ = 5 V ± 0.5 V.

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Maximum data rate (see Figure 1) | | $R_L$ = 3 kΩ, One DOUT switching | $C_L$ = 1000 pF | 250 | | | kbit/s |
| | | | $C_L$ = 250 pF, $V_{CC}$ = 3 V to 4.5 V | 1000 | | | |
| | | | $C_L$ = 1000 pF, $V_{CC}$ = 4.5 V to 5.5 V | 1000 | | | |
| $t_{sk(p)}$ | Pulse skew§ | $C_L$ = 150 pF to 2500 pF | $R_L$ = 3 kΩ to 7 kΩ, See Figure 2 | | 300 | | ns |
| SR(tr) | Slew rate, transition region (see Figure 1) | $R_L$ = 3 kΩ to 7 kΩ, $V_{CC}$ = 3.3 V | $C_L$ = 150 pF to 1000 pF | 18 | | 150 | V/µs |

† All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.
§ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
NOTE 4: Test conditions are C1−C4 = 0.1 µF at $V_{CC}$ = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2−C4 = 0.33 µF at $V_{CC}$ = 5 V ± 0.5 V.

## RECEIVER SECTION

### electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = −1 mA | $V_{CC}$ − 0.6 V | $V_{CC}$ − 0.1 V | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| $V_{IT+}$ | Positive-going input threshold voltage | $V_{CC}$ = 3.3 V | | 1.5 | 2.4 | V |
| | | $V_{CC}$ = 5 V | | 1.8 | 2.4 | |
| $V_{IT-}$ | Negative-going input threshold voltage | $V_{CC}$ = 3.3 V | 0.6 | 1.2 | | V |
| | | $V_{CC}$ = 5 V | 0.8 | 1.5 | | |
| $V_{hys}$ | Input hysteresis ($V_{IT+}$ − $V_{IT-}$) | | | 0.3 | | V |
| $I_{off}$ | Output leakage current | $\overline{EN}$ = $V_{CC}$ | | ±0.05 | ±10 | µA |
| $r_i$ | Input resistance | $V_I$ = ±3 V to ±25 V | 3 | 5 | 7 | kΩ |

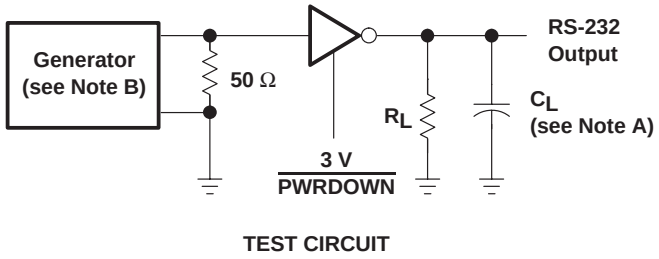
† All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.
NOTE 4: Test conditions are C1−C4 = 0.1 µF at $V_{CC}$ = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2−C4 = 0.33 µF at $V_{CC}$ = 5 V ± 0.5 V.

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

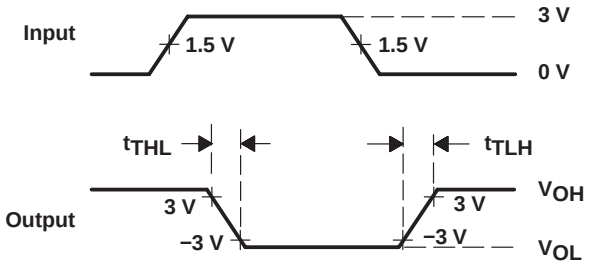
| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $C_L$ = 150 pF, See Figure 3 | | 300 | | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | $C_L$= 150 pF, See Figure 3 | | 300 | | ns |
| $t_{en}$ | Output enable time | $C_L$= 150 pF, $R_L$ = 3 kΩ, See Figure 4 | | 200 | | ns |
| $t_{dis}$ | Output disable time | $C_L$= 150 pF, $R_L$ = 3 kΩ, See Figure 4 | | 200 | | ns |
| $t_{sk(p)}$ | Pulse skew‡ | See Figure 3 | | 300 | | ns |

† All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.
‡ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
NOTE 4: Test conditions are C1−C4 = 0.1 µF at $V_{CC}$ = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2−C4 = 0.33 µF at $V_{CC}$ = 5 V ± 0.5 V.

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT

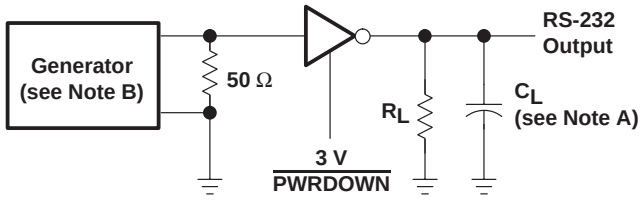



VOLTAGE WAVEFORMS

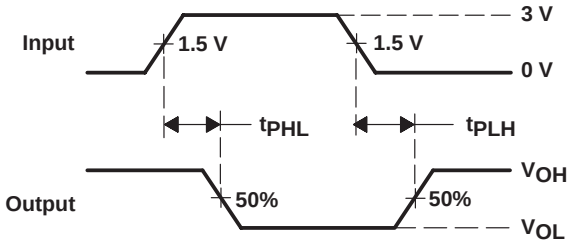
$$SR(tr) = \frac{6\ V}{t_{THL} \text{ or } t_{TLH}}$$

NOTES: A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

**Figure 1. Driver Slew Rate**



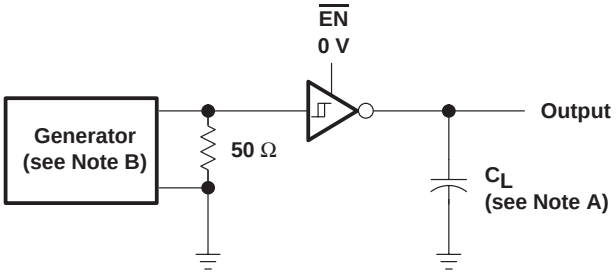

TEST CIRCUIT



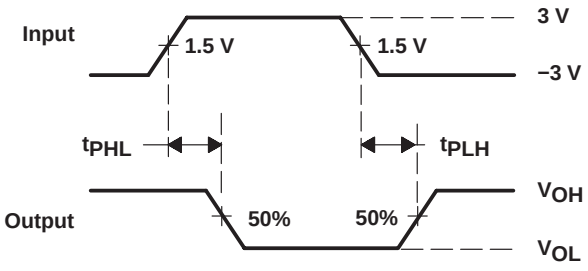

VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

**Figure 2. Driver Pulse Skew**




TEST CIRCUIT

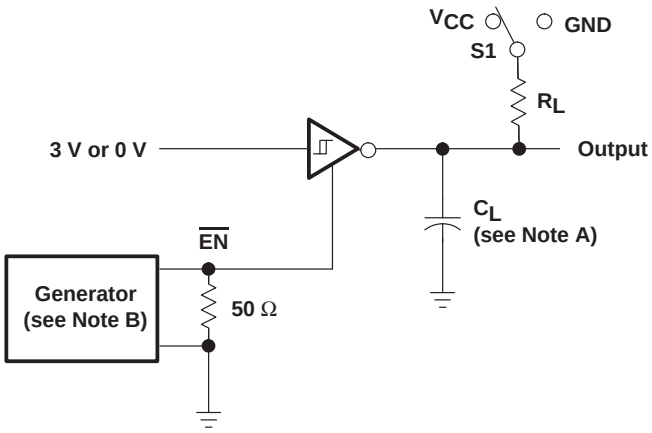



VOLTAGE WAVEFORMS

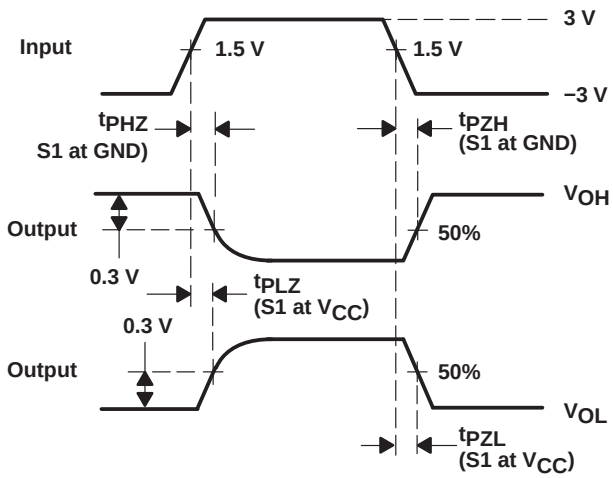
NOTES: A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

**Figure 3. Receiver Propagation-Delay Times**

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT

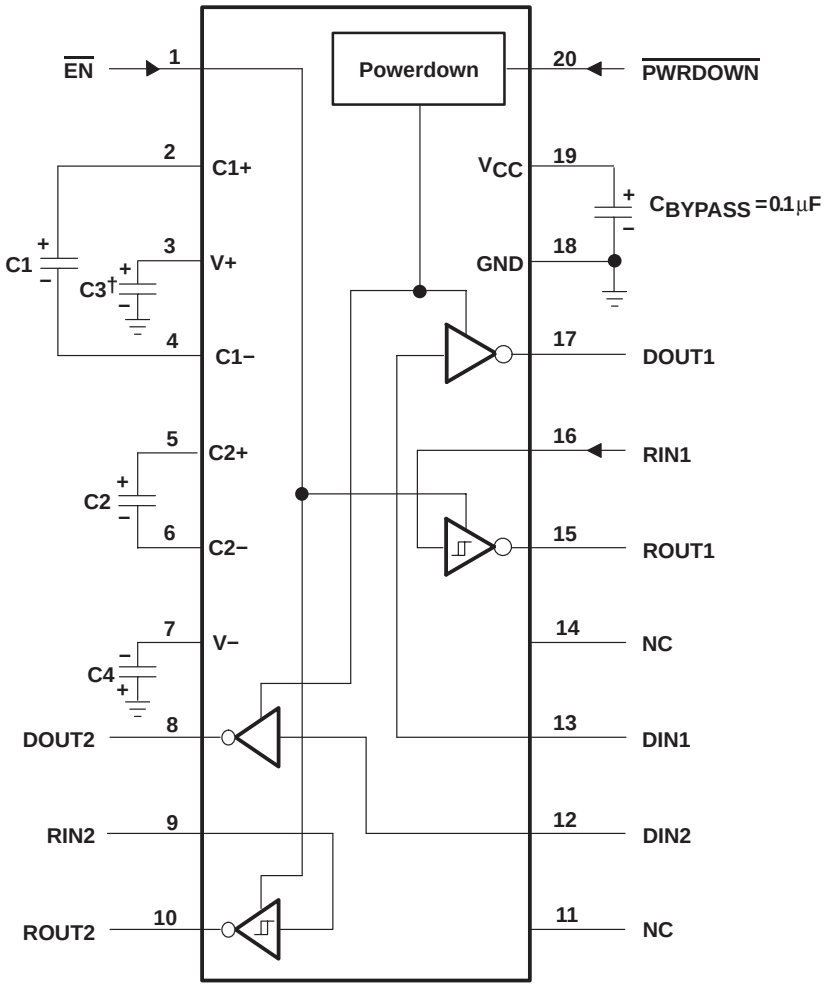



VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

**Figure 4. Receiver Enable and Disable Times**

## APPLICATION INFORMATION




† C3 can be connected to $V_{CC}$ or GND.

NOTES: A. Resistor values shown are nominal.
B. NC − No internal connection

**$V_{CC}$ vs CAPACITOR VALUES**

| $V_{CC}$ | C1 | C2, C3, and C4 |
|---|---|---|
| 3.3 V ± 0.3 V | 0.1 μF | 0.1 μF |
| 5 V ± 0.5 V | 0.047 μF | 0.33 μF |
| 3 V to 5.5 V | 0.1 μF | 0.47 μF |

**Figure 5. Typical Operating Circuit and Capacitor Values**

## PACKAGING INFORMATION

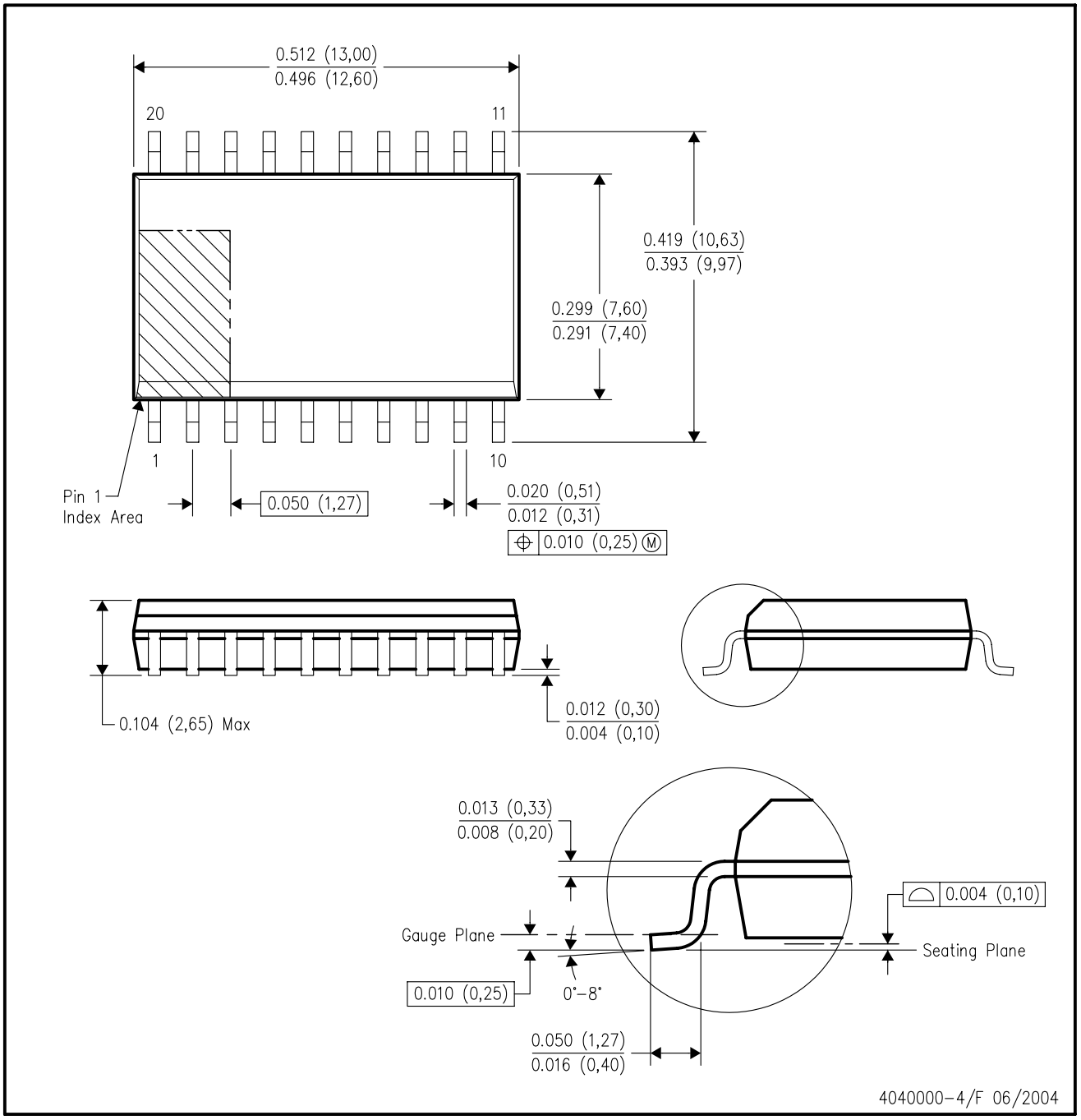
| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| SN65C3222DB | PREVIEW | SSOP | DB | 20 | 70 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN65C3222DBR | ACTIVE | SSOP | DB | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN65C3222DW | ACTIVE | SOIC | DW | 20 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN65C3222DWR | ACTIVE | SOIC | DW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN65C3222PW | ACTIVE | TSSOP | PW | 20 | 70 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN65C3222PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN75C3222DB | PREVIEW | SSOP | DB | 20 | 70 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN75C3222DBR | ACTIVE | SSOP | DB | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN75C3222DW | ACTIVE | SOIC | DW | 20 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN75C3222DWR | ACTIVE | SOIC | DW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN75C3222PW | ACTIVE | TSSOP | PW | 20 | 70 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN75C3222PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**None:** Not yet available Lead (Pb-Free).
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

## DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE

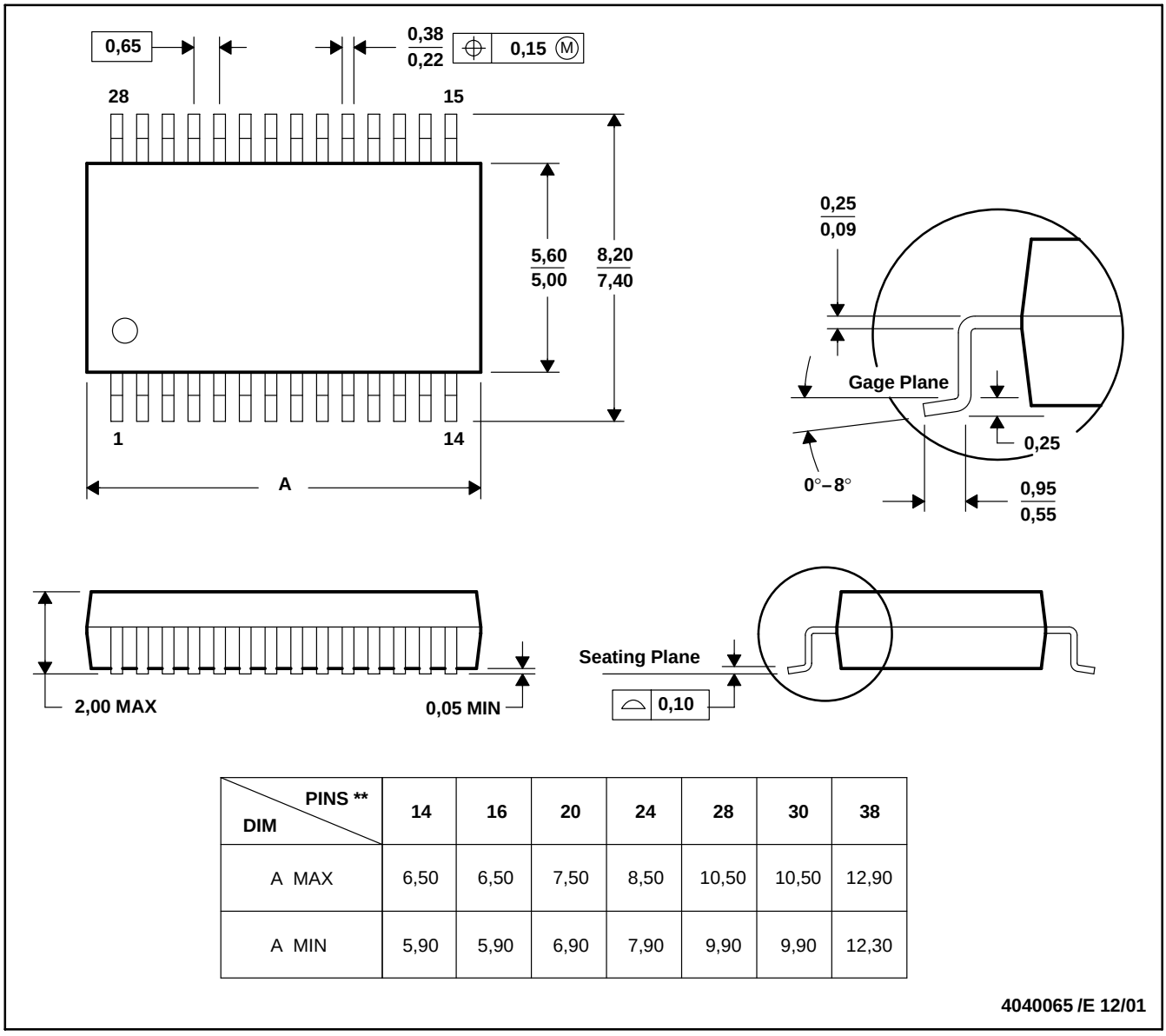



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**



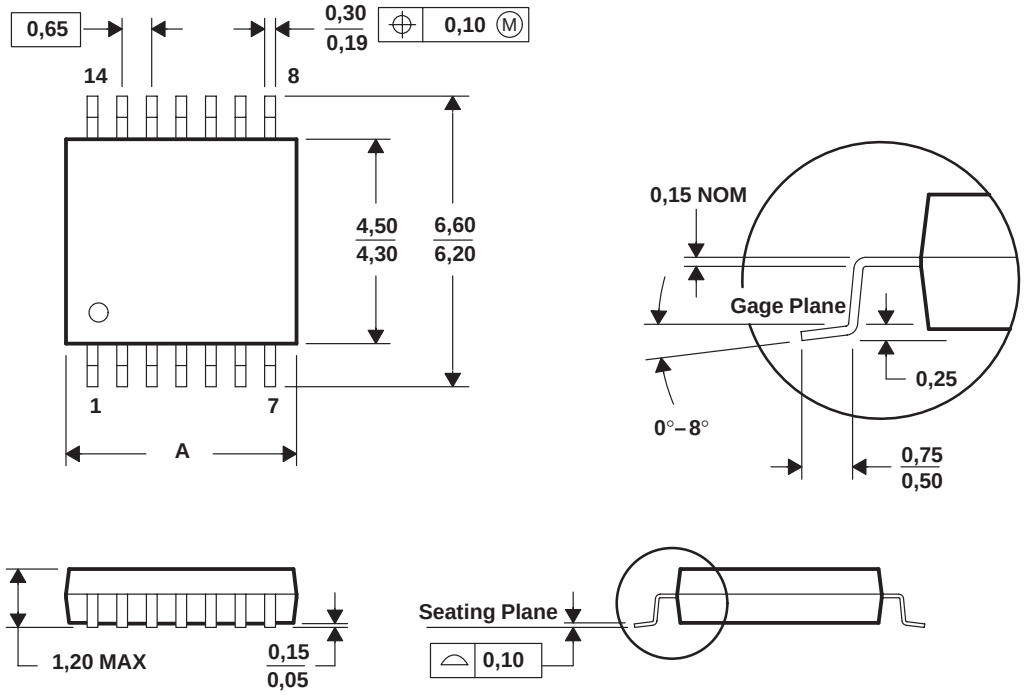

| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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