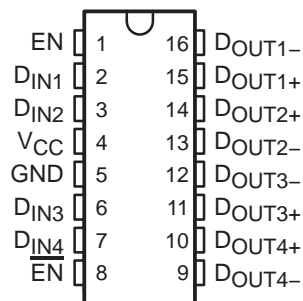


SN65LVDS047 LVDS QUAD DIFFERENTIAL LINE DRIVER

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- >400 Mbps (200 MHz) Signaling Rates
- Flow-Through Pinout Simplifies PCB Layout
- 300 ps Maximum Differential Skew
- Propagation Delay Times 1.8 ns (Typical)
- 3.3 V Power Supply Design
- ± 350 mV Differential Signaling
- High Impedance on LVDS Outputs on Power Down
- Conforms to TIA/EIA-644 LVDS Standard
- Industrial Operating Temperature Range (-40°C to 85°C)
- Available in SOIC and TSSOP Packages

D OR PW PACKAGE
(Marked as LVDS047)
(TOP VIEW)



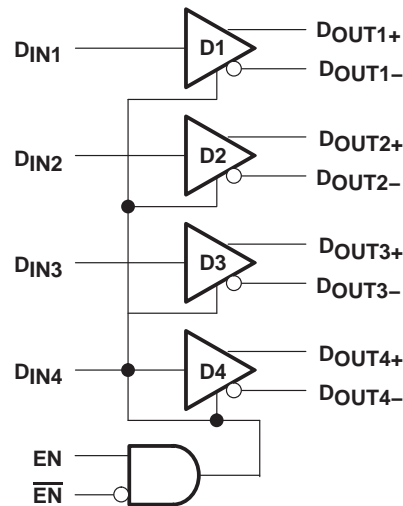
description

The SN65LVDS047 is a quad differential line driver that implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100- Ω load when enabled.

The intended application of this device and signaling technique is for point-to-point and multi-drop baseband data transmission over controlled impedance media of approximately 100 Ω . The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.

The SN65LVDS047 is characterized for operation from -40°C to 85°C .

functional block diagram



TRUTH TABLE

INPUT D _{IN}	ENABLES		OUTPUTS	
	EN	$\overline{\text{EN}}$	D _{OUT+}	D _{OUT-}
L	H	L or OPEN	L	H
H			H	L
X	All other conditions		Z	Z

H = high level, L = low level, X = irrelevant, Z = high impedance (off)



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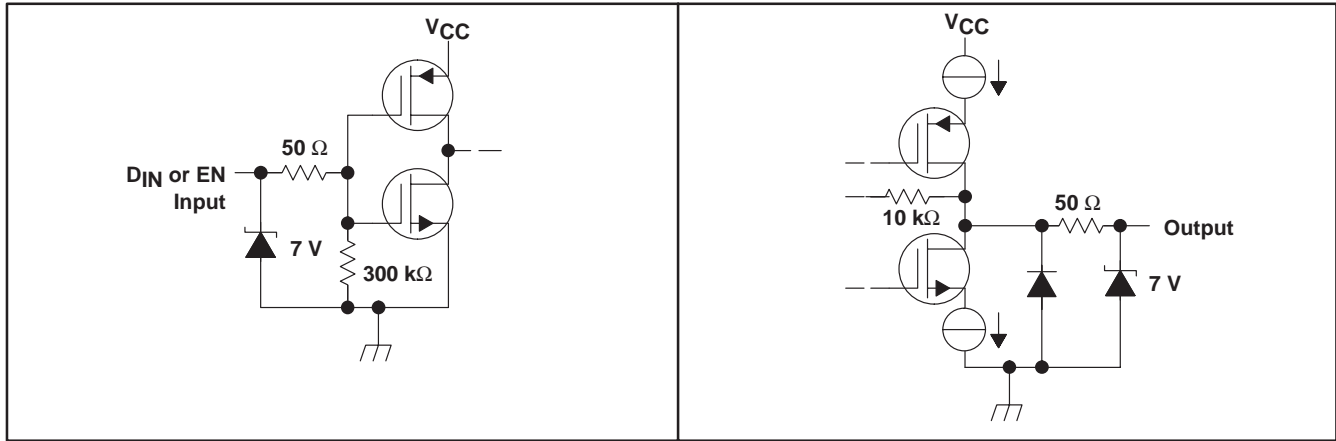
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equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (see Note 1) (unless otherwise noted)†

Supply voltage (V_{CC})	-0.3 V to 4 V
Input voltage range, $V_I(D_{IN})$	-0.3 V to ($V_{CC} + 0.3$ V)
Enable input voltage (EN, \overline{EN})	-0.3 V to ($V_{CC} + 0.3$ V)
Output voltage, $V_O(D_{OUT+}, D_{OUT-})$	-0.5 V to ($V_{CC} + 0.5$ V)
Bus-pin (D_{OUT+}, D_{OUT-}) electrostatic discharge, (see Note 2)	>10 kV
Short circuit duration (D_{OUT+}, D_{OUT-})	Continuous
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
PW	774 mW	6.2 mW/°C	402 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Operating free-air temperature, T_A	-40	25	85	°C

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electrical characteristics over recommended operating free-air temperature range (see Notes 3, 4) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OD}	Differential output voltage	$R_L = 100 \Omega$ (see Figure 1)	250	310	450	mV
$\Delta V_{OD} $	Change in magnitude of V_{OD} for complementary output states			1	35	mV
$V_{OC(SS)}$	Steady-state, common-mode output voltage		1.125	1.17	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			1	25	mV
V_{OH}	Output high voltage			1.33	1.6	V
V_{OL}	Output low voltage		0.90	1.02		V
V_{IH}	Input high voltage			2	V_{CC}	V
V_{IL}	Input low voltage		GND	0.8	V	
I_{IH}	Input high current	$V_{IN} = V_{CC}$ or 2.5 V	-10	3	10	μ A
I_{IL}	Input low current	$V_{IN} = GND$ or 0.4 V	-10	1	10	μ A
V_{IK}	Input clamp voltage	$I_{CL} = -18$ mA	-1.5	-0.8		V
I_{OS}	Output short circuit current (see Note 5)	Enabled, $D_{IN} = V_{CC}$, $D_{OUT+} = 0$ V or $D_{IN} = GND$, $D_{OUT-} = 0$ V		-3.1	-9	mA
I_{OSD}	Differential output short circuit current (see Note 5)	Enabled, $V_{OD} = 0$ V			-9	mA
I_{OFF}	Power-off leakage	$V_O = 0$ V or 3.6 V, $V_{CC} = 0$ V or Open	-1		1	μ A
I_{OZ}	Output 3-state current	$EN = 0.8$ V and $\overline{EN} = 2$ V, $V_O = 0$ V or V_{CC}	-1		1	μ A
I_{CC}	No load supply current, drivers enabled	$D_{IN} = V_{CC}$ or GND		7		mA
I_{CCL}	Loaded supply current, drivers enabled	$R_L = 100 \Omega$ all channels, $D_{IN} = V_{CC}$ or GND (all inputs)		20	26	mA
$I_{CC(Z)}$	No load supply current, drivers disabled	$D_{IN} = V_{CC}$ or GND, $EN = GND$, $\overline{EN} = V_{CC}$		0.5	1.3	mA

† All typical values are given for: $V_{CC} = 3.3$ V, $T_A = 25^\circ$ C.

- NOTES:
3. Current into device pin is defined as positive. Current out of the device is defined as negative. All voltages are referenced to ground, unless otherwise specified.
 4. The SN65LVDS047 is a current mode device and only functions within data sheet specifications when a resistive load is applied to the driver outputs, 90 Ω to 110 Ω typical range.
 5. Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

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switching characteristics over recommended operating conditions (see Notes 6, 7, and 12) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{PHL}	Differential propagation delay, high-to-low	R _L = 100 Ω, C _L = 15 pF (see Figures 2 and 3)	1.4	1.8	2.8	ns
t _{PLH}	Differential propagation delay, low-to-high		1.4	1.8	2.8	ns
t _{SK(p)}	Differential pulse skew (t _{PHLD} – t _{PLHD}) (see Note 8)			50	300	ps
t _{SK(o)}	Channel-to-channel skew (see Note 9)			40	300	ps
t _{SK(pp)}	Differential part-to-part skew (see Note 10)				1	ns
t _{SK(lim)}	Differential part-to-part skew (see Note 11)				1.2	ns
t _r	Rise time			0.5	1.5	ns
t _f	Fall time		0.5	1.5	ns	
t _{PHZ}	Disable time high to Z	R _L = 100 Ω, C _L = 15 pF (see Figures 4 and 5)		5.5	8	ns
t _{PLZ}	Disable time low to Z			5.5	8	ns
t _{PZH}	Enable time Z to high			8.5	12	ns
t _{PZL}	Enable time Z to low			8.5	12	ns
f _(MAX)	Maximum operating frequency (see Note 13)			250		MHz

† All typical values are given for: V_{CC} = 3.3 V, T_A = 25°C.

NOTES: 6. Generator waveform for all tests unless otherwise: f = 1 MHz, Z₀ = 50 Ω, t_r < 1 ns, and t_f < 1 ns.

7. C_L includes probe and jig capacitance.

8. t_{SK(p)}|t_{PHL}–t_{PLH}| is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

9. t_{SK(o)} is the differential channel-to-channel skew of any event on the same device.

10. t_{SK(pp)} is the differential part-to-part skew, and is defined as the difference between the minimum and the maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

11. t_{SK(lim)} part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SK(lim)} is defined as |Min – Max| differential propagation delay.

12. All input voltages are for one channel unless otherwise specified. Other inputs are set to GND.

13. f_(MAX) generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle = 45% to 55, V_{OD} > 250 mV, all channels switching

PARAMETER MEASUREMENT INFORMATION

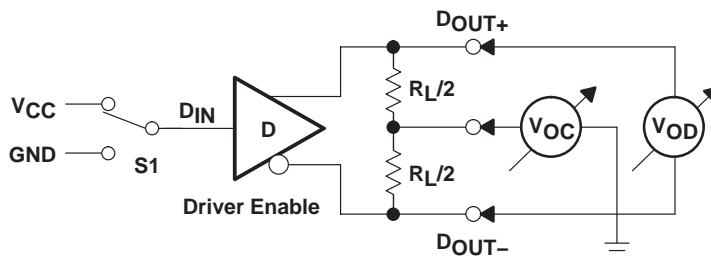


Figure 1. Driver V_{OD} and V_{OC} Test Circuit

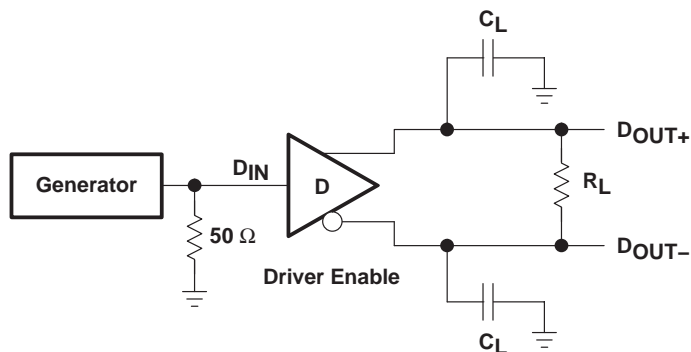


Figure 2. Driver Propagation Delay and Transition Time Test Circuit

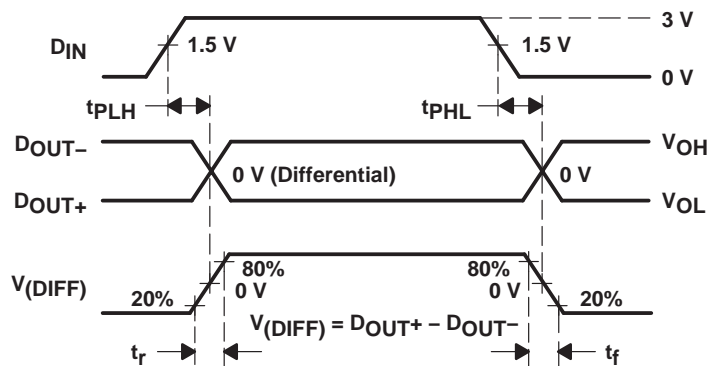


Figure 3. Driver Propagation Delay and Transition Time Waveforms

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PARAMETER MEASUREMENT INFORMATION

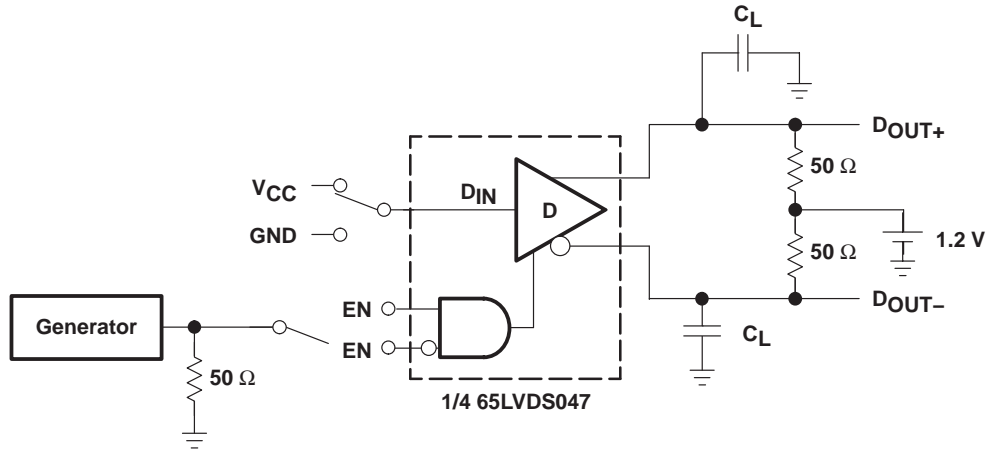


Figure 4. Driver 3-State Delay Test Circuit

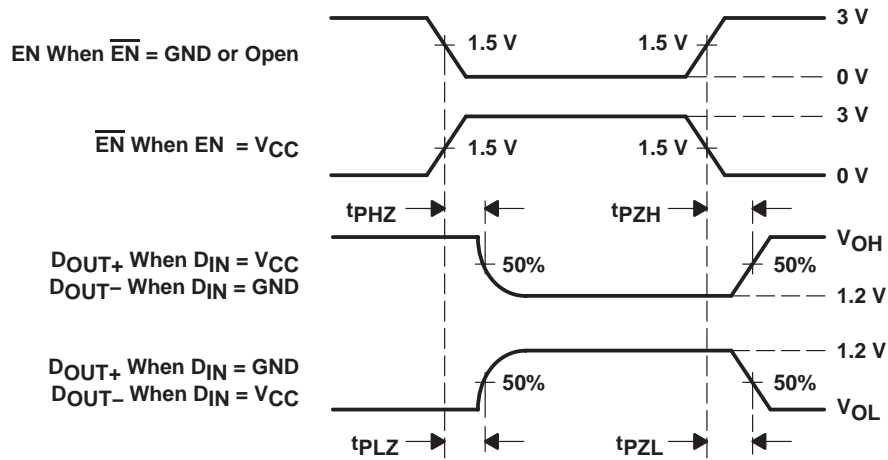


Figure 5. Driver 3-State Delay Waveform

TYPICAL CHARACTERISTICS

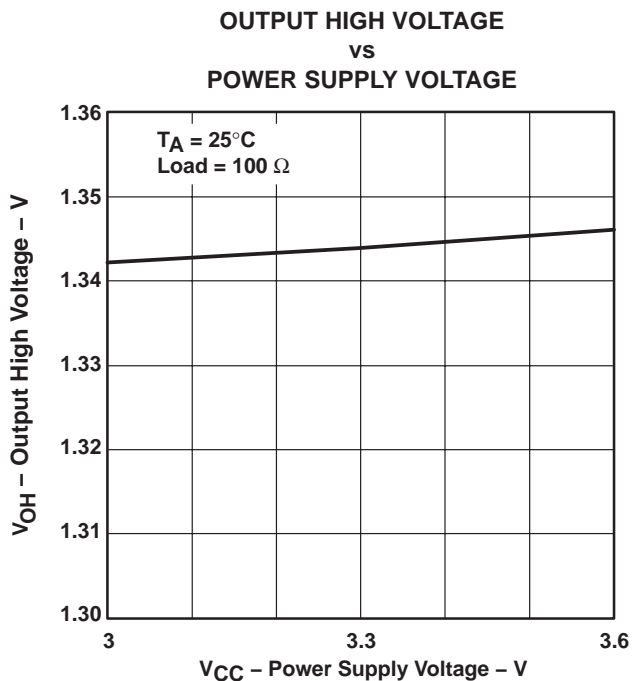


Figure 6

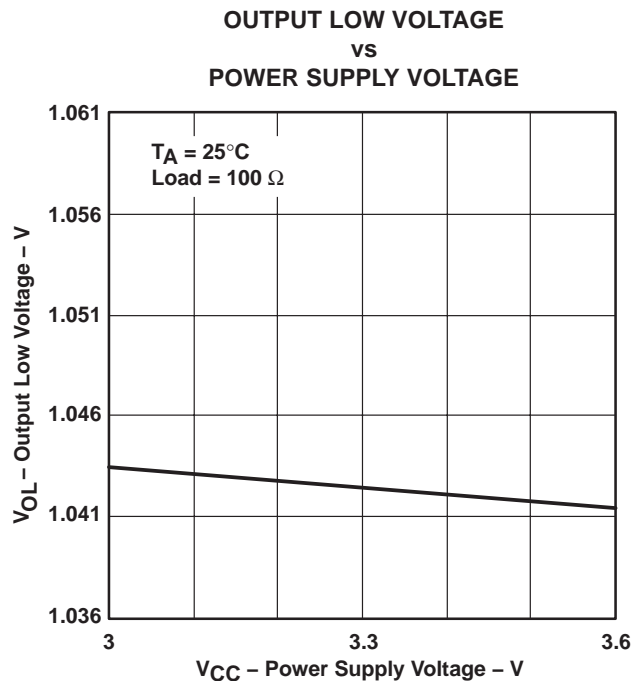


Figure 7

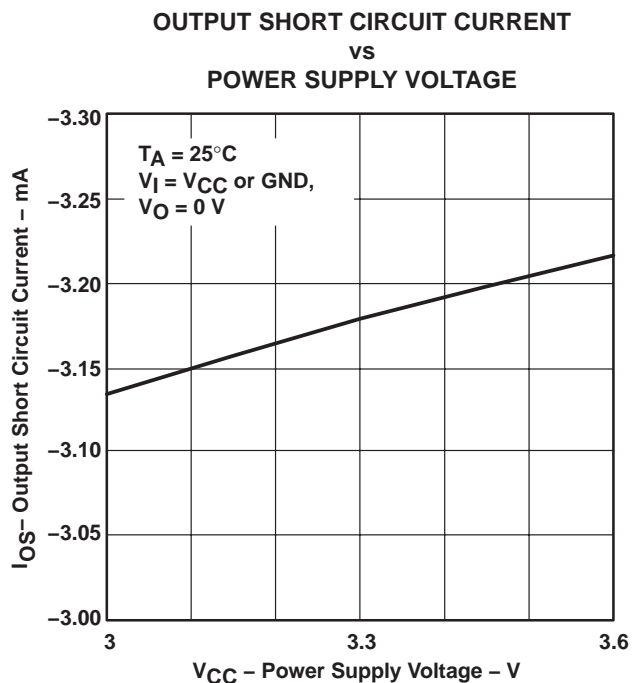


Figure 8

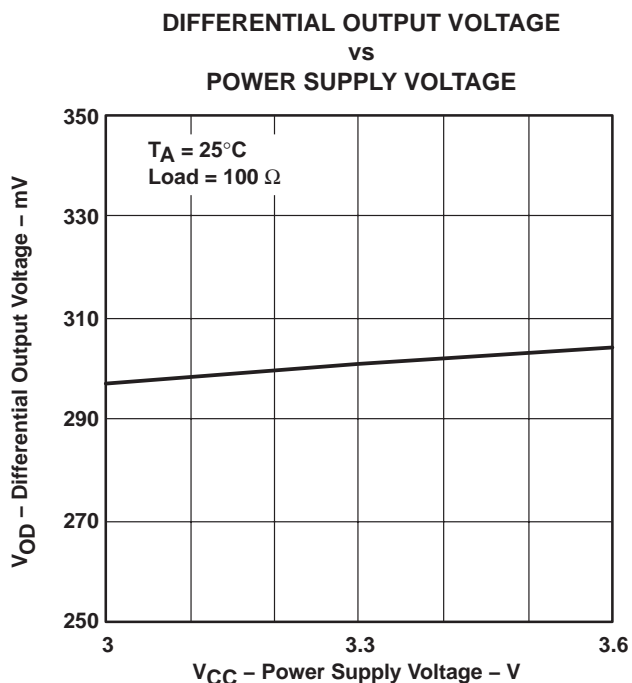


Figure 9

SN65LVDS047

LVDS QUAD DIFFERENTIAL LINE DRIVER

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TYPICAL CHARACTERISTICS

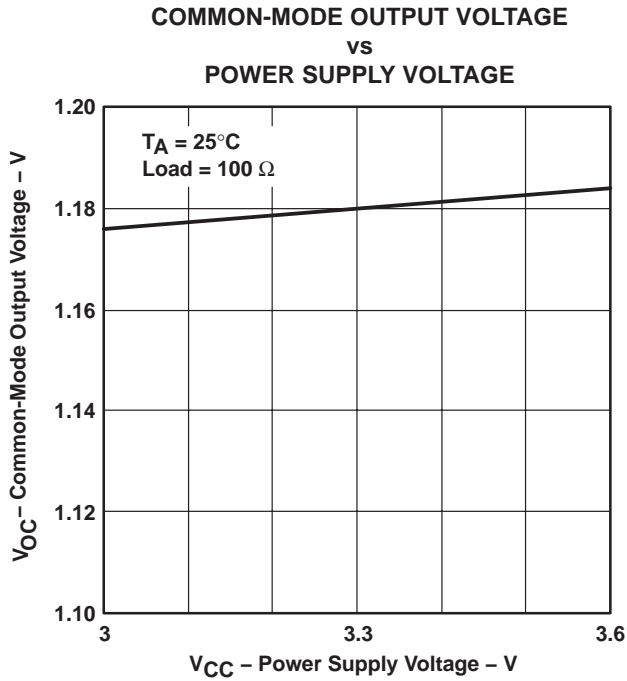


Figure 10

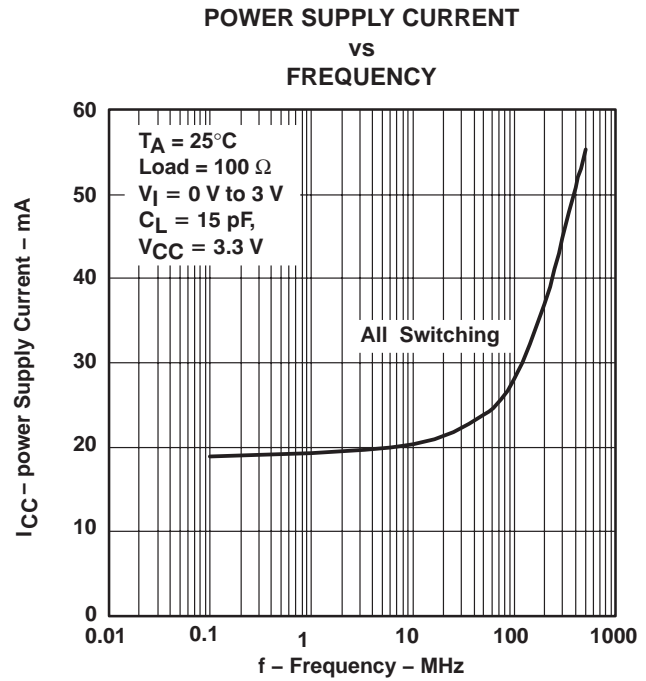


Figure 11

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65LVDS047D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS047DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS047PW	ACTIVE	TSSOP	PW	16	90	None	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS047PWR	ACTIVE	TSSOP	PW	16	2000	None	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS047PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AC.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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