

SN65LVDS179-Q1, SN65LVDS180-Q1, SN65LVDS050-Q1, SN65LVDS051-Q1 HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

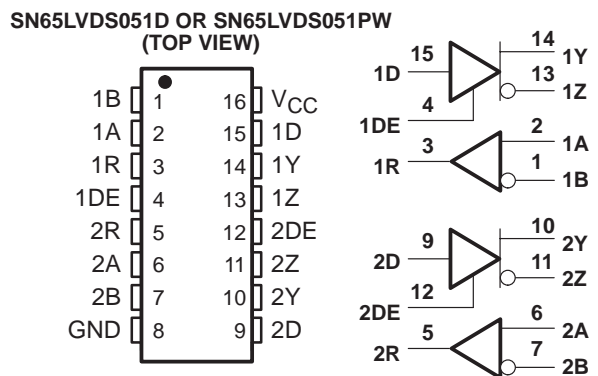
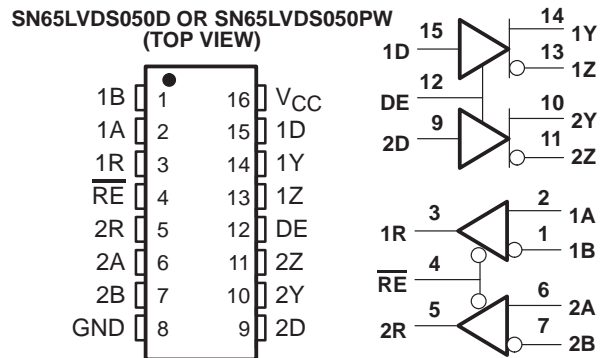
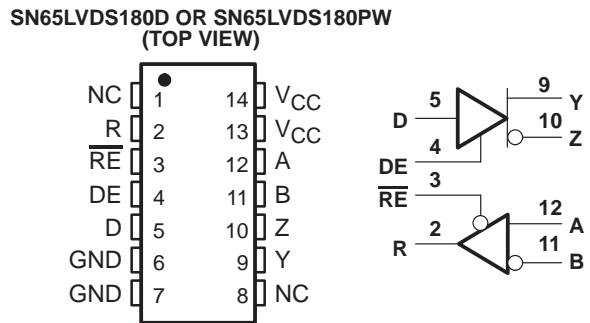
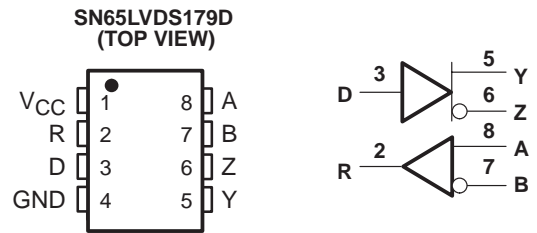
SGLS204 – SEPTEMBER 2003

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995 Standard
- Signaling Rates up to 400 Mbps
- Bus-Terminal ESD Exceeds 12 kV
- Operates From a Single 3.3-V Supply
- Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV and a 100-Ω Load
- Propagation Delay Times
 - Driver: 1.7 ns Typ
 - Receiver: 3.7 ns Typ
- Power Dissipation at 200 MHz
 - Driver: 25 mW Typical
 - Receiver: 60 mW Typical
- LVTTTL Input Levels Are 5-V Tolerant
- Receiver Maintains High Input Impedance With $V_{CC} < 1.5$ V
- Receiver Has Open-Circuit Fail Safe

† Contact factory for details. Q100 qualification data available on request.

description/ordering information

The SN65LVDS179, SN65LVDS180, SN65LVDS050, and SN65LVDS051 are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps. The TIA/EIA-644 standard compliant electrical interface provides a minimum differential output voltage magnitude of 247 mV into a 100-Ω load and receipt of 50-mV signals with up to 1 V of ground potential difference between a transmitter and receiver.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated

SN65LVDS179-Q1, SN65LVDS180-Q1, SN65LVDS050-Q1, SN65LVDS051-Q1 HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

SGLS204 – SEPTEMBER 2003

description/ordering information (continued)

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100-Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics).

The devices offer various driver, receiver, and enabling combinations in industry standard footprints. Since these devices are intended for use in simplex or distributed simplex bus structures, the driver enable function does not put the differential outputs into a high-impedance state but rather disconnects the input and reduces the quiescent power used by the device. (For these functions with a high-impedance driver output, see the SN65LVDM series of devices.) All devices are characterized for operation from -40°C to 85°C.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC (D)	Tape and Reel	SN65LVDS179DRQ1‡	VDS179Q
	TSSOP (PW)	Tape and Reel	SN65LVDS179PWRQ1‡	VDS179Q
-40°C to 85°C	SOIC (D)	Tape and Reel	SN65LVDS180DRQ1	VDS180Q
	TSSOP (PW)	Tape and Reel	SN65LVDS180PWRQ1	VDS180Q
-40°C to 85°C	SOIC (D)	Tape and Reel	SN65LVDS050DRQ1‡	VDS050Q
	TSSOP (PW)	Tape and Reel	SN65LVDS050PWRQ1‡	VDS050Q
-40°C to 85°C	SOIC (D)	Tape and Reel	SN65LVDS051DRQ1	VDS051Q
	TSSOP (PW)	Tape and Reel	SN65LVDS051PWRQ1	VDS051Q

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ Product Preview



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN65LVDS179-Q1, SN65LVDS180-Q1, SN65LVDS050-Q1, SN65LVDS051-Q1 HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

SGLS204 – SEPTEMBER 2003

Function Tables

SN65LVDS179 RECEIVER

INPUTS	OUTPUT
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 50 \text{ mV}$	H
$-50 \text{ mV} < V_{ID} < 50 \text{ mV}$?
$V_{ID} \leq -50 \text{ mV}$	L
Open	H

H = high level, L = low level, ? = indeterminate

SN65LVDS179 DRIVER

INPUT	OUTPUTS	
D	Y	Z
L	L	H
H	H	L
Open	L	H

H = high level, L = low level

SN65LVDS180, SN65LVDS050, and SN65LVDS051 RECEIVER

INPUTS		OUTPUT	
$V_{ID} = V_A - V_B$	RE	R	
$V_{ID} \geq 50 \text{ mV}$	L	H	
$-50 \text{ mV} < V_{ID} < 50 \text{ mV}$	L	?	
$V_{ID} \leq -50 \text{ mV}$	L	L	
Open	L	H	
X	H	Z	

H = high level, L = low level, Z = high impedance,
X = don't care

SN65LVDS180, SN65LVDS050, and SN65LVDS051 DRIVER

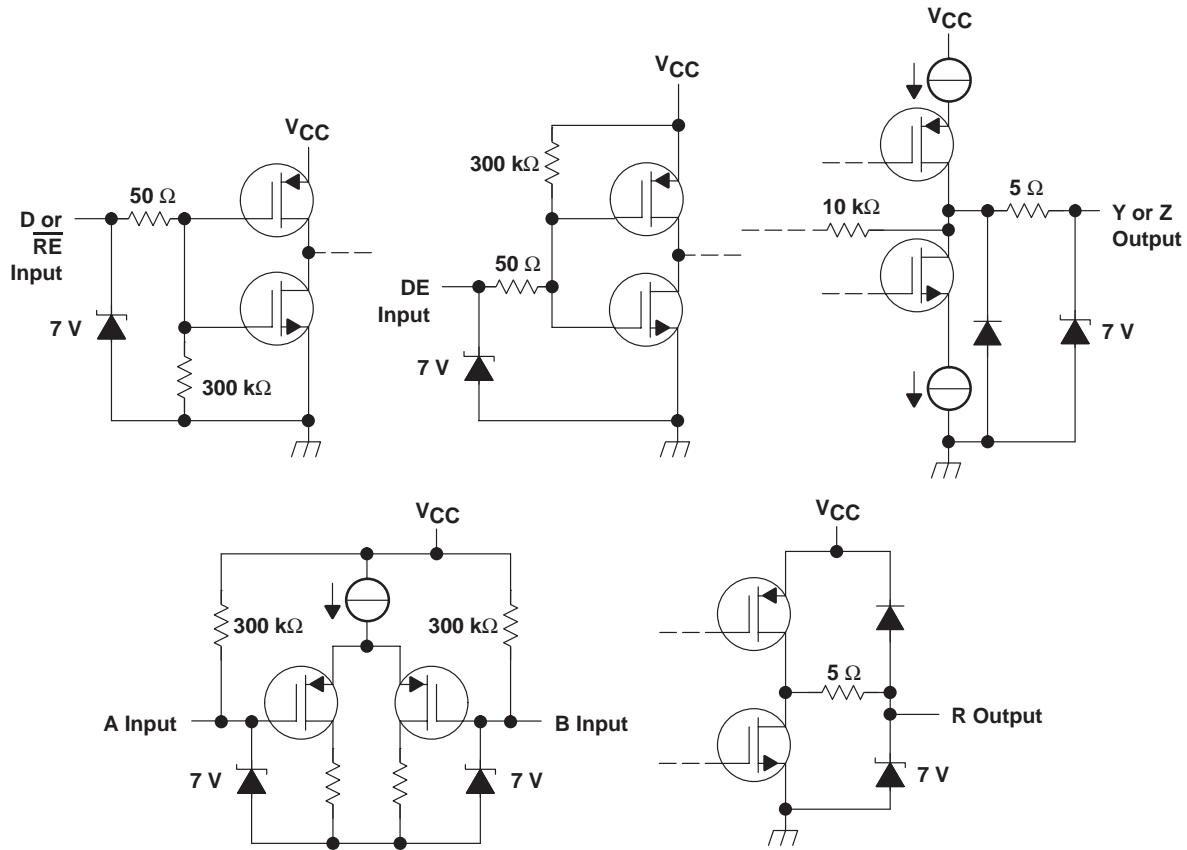
INPUTS		OUTPUTS	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	OFF	OFF

H = high level, L = low level, OFF = No Output,
X = don't care

SN65LVDS179-Q1, SN65LVDS180-Q1, SN65LVDS050-Q1, SN65LVDS051-Q1 HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

SGLS204 – SEPTEMBER 2003

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	-0.5 V to 4 V
Voltage range: D, R, DE, \overline{RE}	-0.5 V to 6 V
Y, Z, A, and B	-0.5 V to 4 V
Electrostatic discharge: Y, Z, A, B, and GND (see Note 2)	Class 3, A:12 kV, B:600 V
All	Class 3, A:7 kV, B:500 V
Continuous power dissipation	See Dissipation Rating Table
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	250°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltages are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

SN65LVDS179-Q1, SN65LVDS180-Q1, SN65LVDS050-Q1, SN65LVDS051-Q1 HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

SGLS204 – SEPTEMBER 2003

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ †	$T_A = 85^\circ\text{C}$ POWER RATING
PW(14)	736 mW	5.9 mW/°C	383 mW
PW(16)	839 mW	6.7 mW/°C	437 mW
D(8)	635 mW	5.1 mW/°C	330 mW/°C
D(14)	987 mW	7.9 mW/°C	513 mW/°C
D(16)	1110 mW	8.9 mW/°C	577 mW/°C

† This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Magnitude of differential input voltage, $ V_{ID} $	0.1		0.6	V
Magnitude of differential output voltage with disabled driver, $ V_{OD(dis)} $			520	mV
Driver output voltage, V_{OY} or V_{OZ}	0		2.4	V
Common-mode input voltage, V_{IC} (see Figure 5)	$\frac{ V_{ID} }{2}$		$2.4 - \frac{ V_{ID} }{2}$	V
			$V_{CC} - 0.8$	
Operating free-air temperature, T_A	-40		85	°C

device electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
I_{CC}	Supply current	SN65LVDS179	No receiver load, driver $R_L = 100 \Omega$		9	12	mA
		SN65LVDS180	Driver and receiver enabled, no receiver load, driver $R_L = 100 \Omega$		9	12	
			Driver enabled, receiver disabled, $R_L = 100 \Omega$		5	7	
			Driver disabled, receiver enabled, no load		1.5	2	
			Disabled		0.5	1	
		SN65LVDS050	Drivers and receivers enabled, no receiver loads, driver $R_L = 100 \Omega$		12	20	mA
			Drivers enabled, receivers disabled, $R_L = 100 \Omega$		10	16	
			Drivers disabled, receivers enabled, no loads		3	6	
		SN65LVDS051	Disabled		0.5	1	mA
			Drivers enabled, no receiver loads, driver $R_L = 100 \Omega$		12	20	
				Drivers disabled, no loads	3	6	

† All typical values are at 25°C and with a 3.3-V supply.



SN65LVDS179-Q1, SN65LVDS180-Q1, SN65LVDS050-Q1, SN65LVDS051-Q1 HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

SGLS204 – SEPTEMBER 2003

driver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OD} $	Differential output voltage magnitude	$R_L = 100 \Omega$, See Figures 1 and 2	247	340	454	mV
$\Delta V_{OD} $	Change in differential output voltage magnitude between logic states		-50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
I_{IH}	High-level input current	DE	$V_{IH} = 5 V$	-0.5	-20	μA
		D		2	20	
I_{IL}	Low-level input current	DE	$V_{IL} = 0.8 V$	-0.5	-10	μA
		D		2	10	
I_{OS}	Short-circuit output current	V_{OY} or $V_{OZ} = 0 V$		3	10	mA
		$V_{OD} = 0 V$		3	10	
$I_{O(OFF)}$	Off-state output current	DE = 0 V, $V_{OY} = V_{OZ} = 0 V$	-1		1	μA
		DE = V_{CC} , $V_{OY} = V_{OZ} = 0 V$, $V_{CC} < 1.5 V$				
C_{IN}	Input capacitance			3		pF

receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 5 and Table 1			50	mV
V_{IT-}	Negative-going differential input voltage threshold		-50			
V_{OH}	High-level output voltage	$I_{OH} = -8 mA$	2.4			V
		$I_{OH} = -4 mA$	2.8			
V_{OL}	Low-level output voltage	$I_{OL} = 8 mA$			0.4	V
I_I	Input current (A or B inputs)	$V_I = 0$	-2	-11	-20	μA
		$V_I = 2.4 V$	-1.2	-3		
$I_{I(OFF)}$	Power-off input current (A or B inputs)	$V_{CC} = 0$			± 20	μA
I_{IH}	High-level input current (enables)	$V_{IH} = 5 V$			± 10	μA
I_{IL}	Low-level input current (enables)	$V_{IL} = 0.8 V$			± 10	μA
I_{OZ}	High-impedance output current	$V_O = 0$ or $5 V$			± 10	μA
C_I	Input capacitance			5		pF

† All typical values are at 25°C and with a 3.3-V supply.



SN65LVDS179-Q1, SN65LVDS180-Q1, SN65LVDS050-Q1, SN65LVDS051-Q1 HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

SGLS204 – SEPTEMBER 2003

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	R _L = 100 Ω, C _L = 10 pF, See Figure 2		1.7	2.7	ns
t _{PHL}	Propagation delay time, high-to-low-level output			1.7	2.7	ns
t _r	Differential output signal rise time			0.8	1	ns
t _f	Differential output signal fall time			0.8	1	ns
t _{sk(p)}	Pulse skew (t _{pHL} - t _{pLH})‡				300	ps
t _{sk(o)}	Channel-to-channel output skew§				150	ps
t _{en}	Enable time	See Figure 4		4.3	10	ns
t _{dis}	Disable time			3.1	10	ns

† All typical values are at 25°C and with a 3.3-V.

‡ t_{sk(p)} is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

§ t_{sk(o)} is the magnitude of the time difference between the outputs of a single device with all of their inputs connected together.

¶ t_{sk(pp)} is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	C _L = 10 pF, See Figure 6		3.7	4.5	ns
t _{PHL}	Propagation delay time, high-to-low-level output			3.7	4.5	ns
t _{sk(p)}	Pulse skew (t _{pHL} - t _{pLH})‡				0.3	ns
t _r	Output signal rise time			0.7	1.5	ns
t _f	Output signal fall time			0.9	1.5	ns
t _{PZH}	Propagation delay time, high-level-to-high-impedance output	See Figure 7		2.5		ns
t _{PZL}	Propagation delay time, low-level-to-low-impedance output			2.5		ns
t _{PHZ}	Propagation delay time, high-impedance-to-high-level output				7	ns
t _{PLZ}	Propagation delay time, low-impedance-to-high-level output				4	ns

† All typical values are at 25°C and with a 3.3-V.

‡ t_{sk(p)} is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

§ t_{sk(o)} is the magnitude of the time difference between the outputs of a single device with all of their inputs connected together.

¶ t_{sk(pp)} is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

SN65LVDS179-Q1, SN65LVDS180-Q1, SN65LVDS050-Q1, SN65LVDS051-Q1 HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

SGLS204 – SEPTEMBER 2003

PARAMETER MEASUREMENT INFORMATION

driver

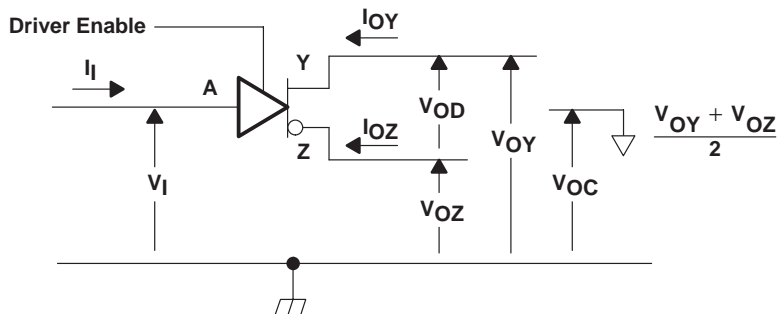
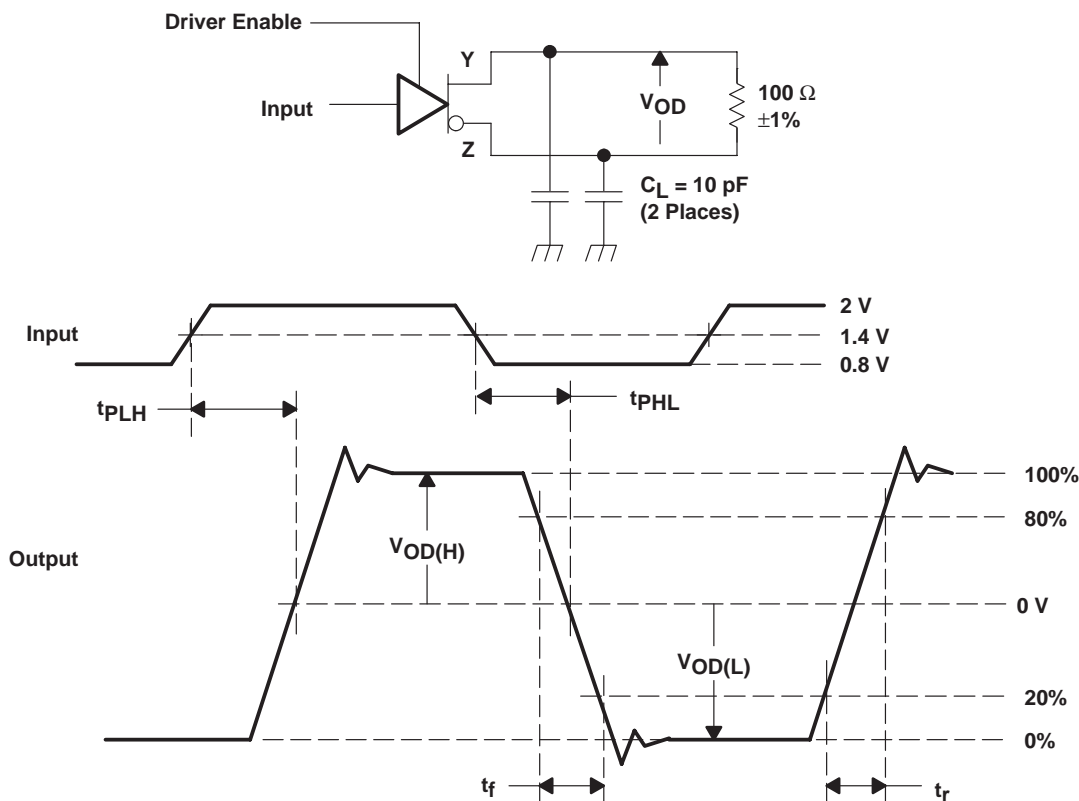


Figure 1. Driver Voltage and Current Definitions

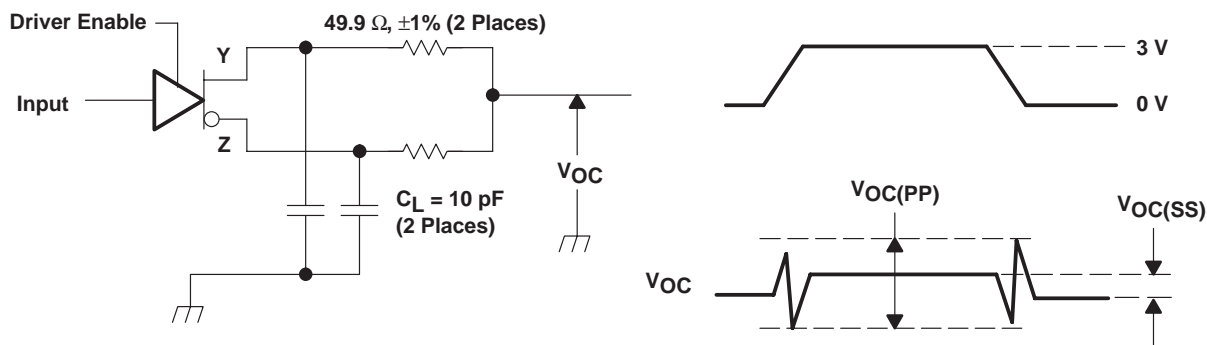


NOTE A: All input pulses are supplied by a generator having the following characteristics: t_f or $t_r \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

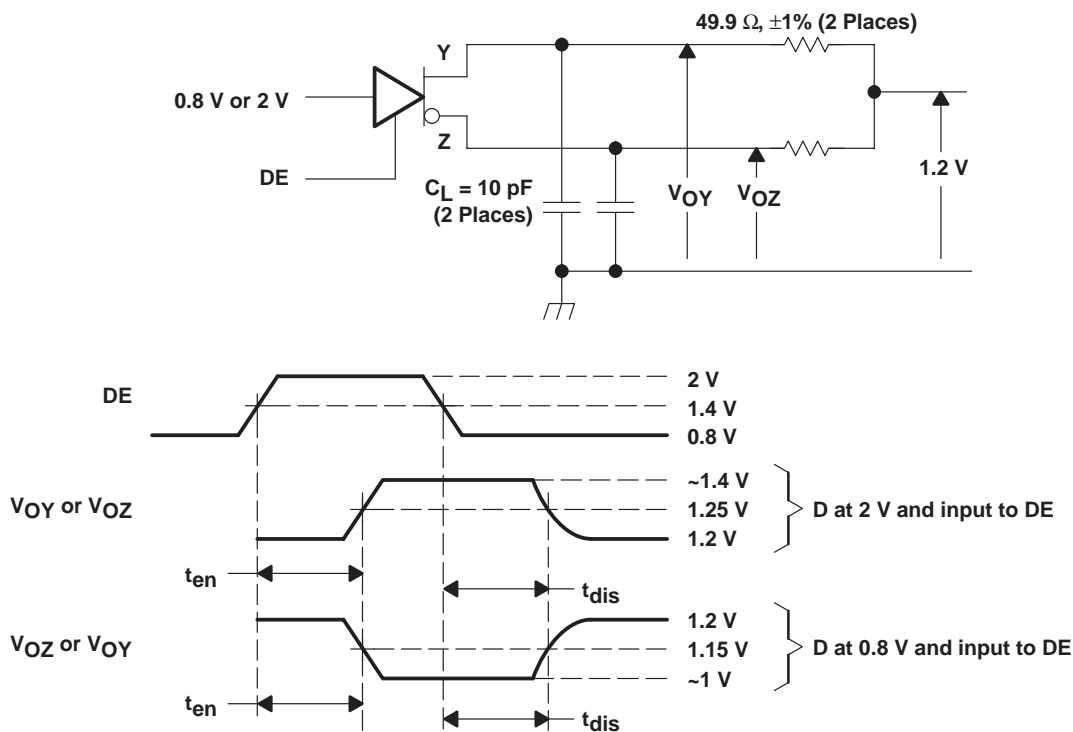
PARAMETER MEASUREMENT INFORMATION

driver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Enable and Disable Time Circuit and Definitions

SN65LVDS179-Q1, SN65LVDS180-Q1, SN65LVDS050-Q1, SN65LVDS051-Q1 HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

SGLS204 – SEPTEMBER 2003

PARAMETER MEASUREMENT INFORMATION

receiver

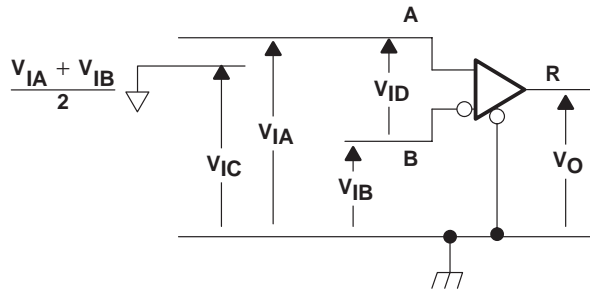


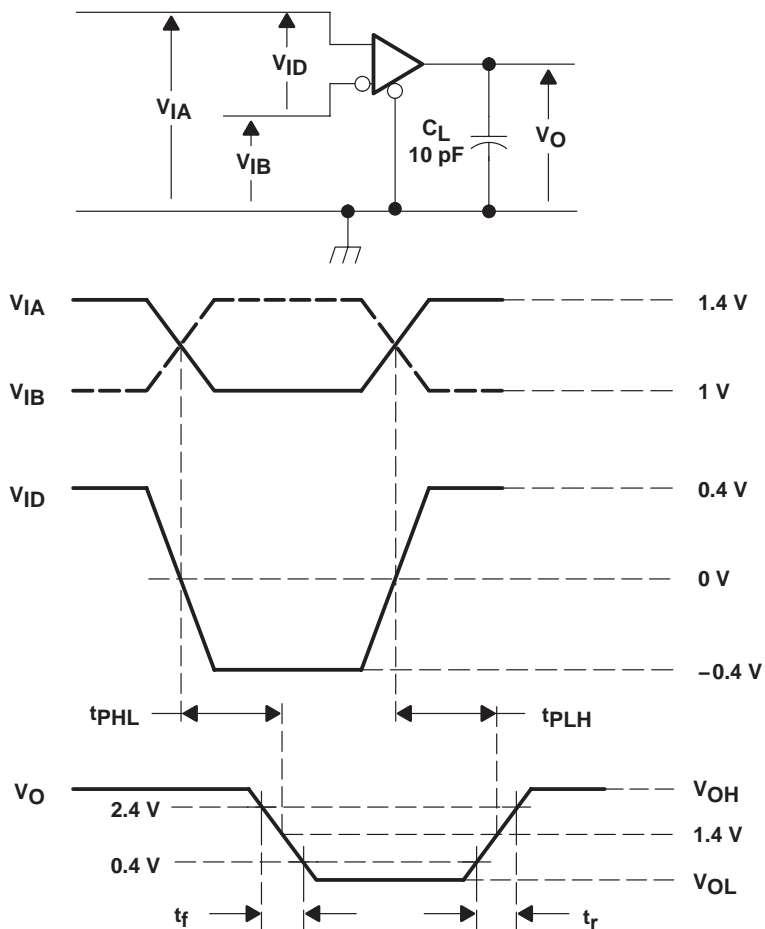
Figure 5. Receiver Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES (V)		RESULTING DIFFERENTIAL INPUT VOLTAGE (mV)	RESULTING COMMON-MODE INPUT VOLTAGE (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	-100	1.2
2.4	2.3	100	2.35
2.3	2.4	-100	2.35
0.1	0	100	0.05
0	0.1	-100	0.05
1.5	0.9	600	1.2
0.9	1.5	-600	1.2
2.4	1.8	600	2.1
1.8	2.4	-600	2.1
0.6	0	600	0.3
0	0.6	-600	0.3

PARAMETER MEASUREMENT INFORMATION

receiver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

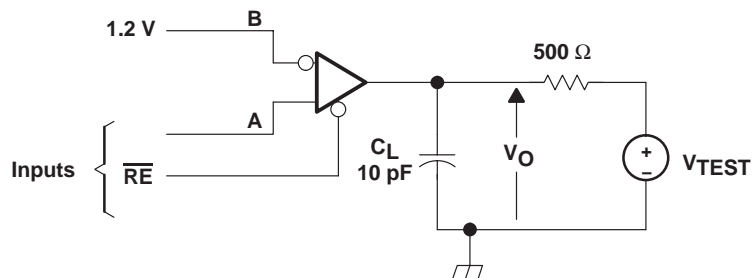
Figure 6. Timing Test Circuit and Waveforms

SN65LVDS179-Q1, SN65LVDS180-Q1, SN65LVDS050-Q1, SN65LVDS051-Q1 HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

SGLS204 – SEPTEMBER 2003

PARAMETER MEASUREMENT INFORMATION

receiver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

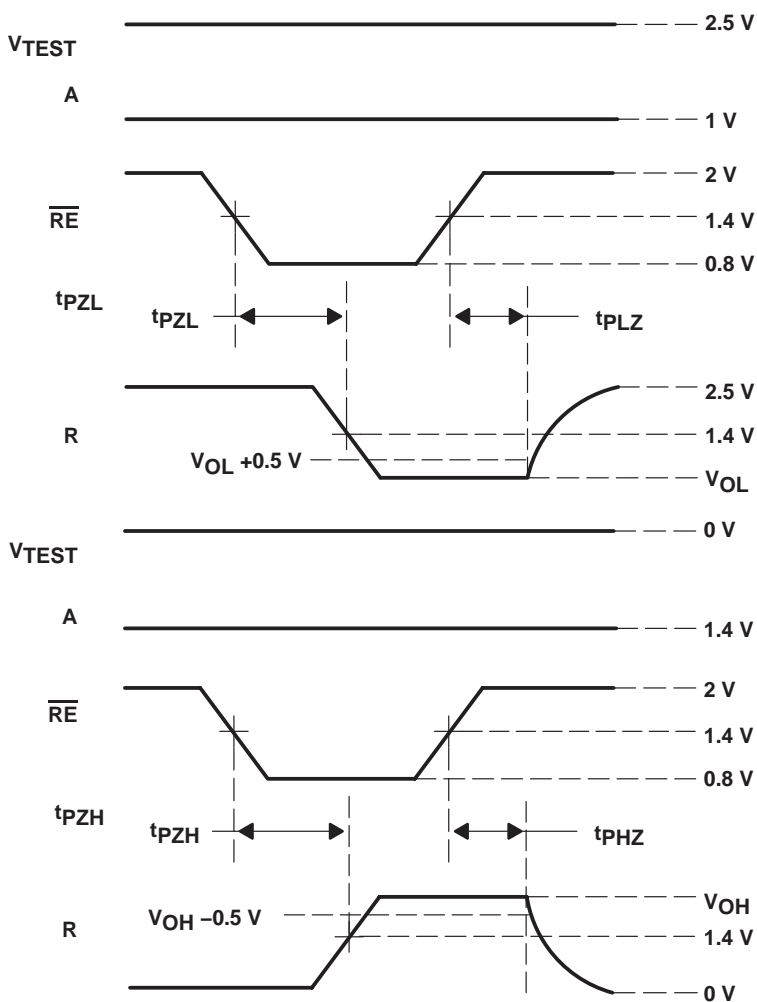


Figure 7. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

DISABLED DRIVER OUTPUT CURRENT
vs
OUTPUT VOLTAGE

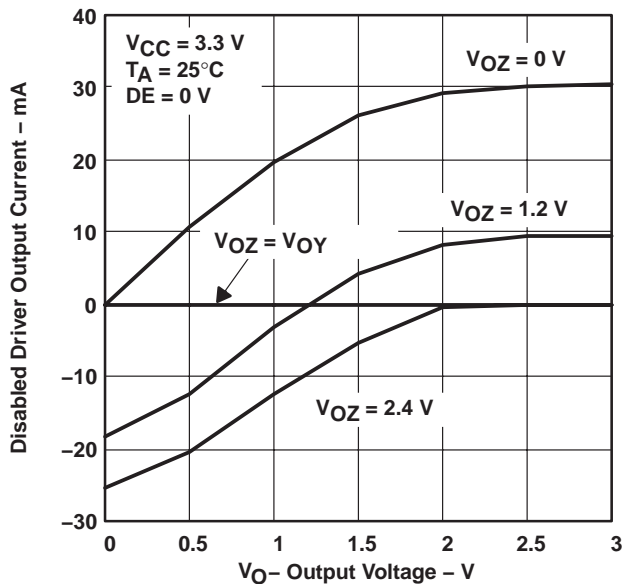


Figure 8

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

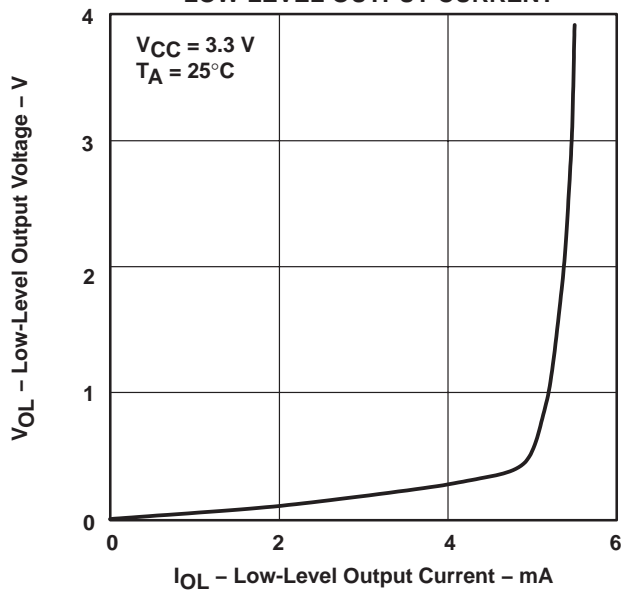


Figure 9

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

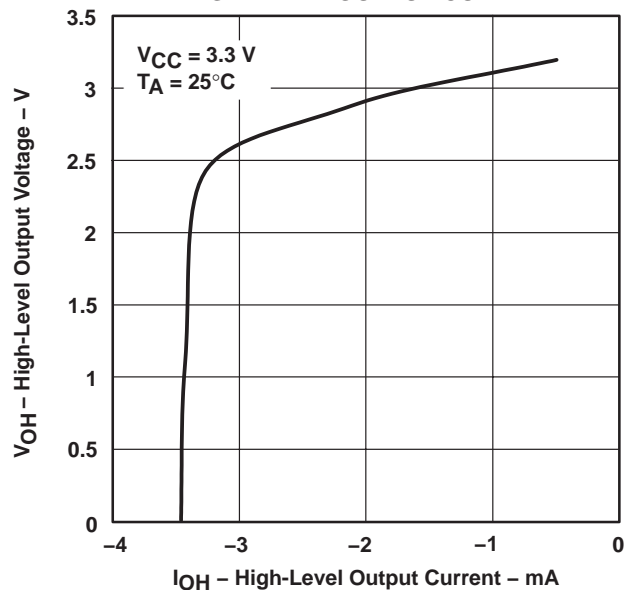


Figure 10

SN65LVDS179-Q1, SN65LVDS180-Q1, SN65LVDS050-Q1, SN65LVDS051-Q1 HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

SGLS204 – SEPTEMBER 2003

TYPICAL CHARACTERISTICS

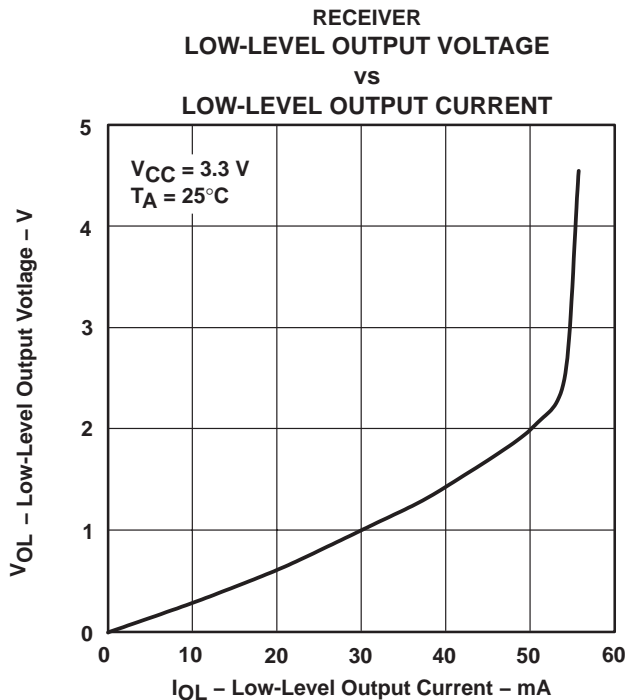


Figure 11

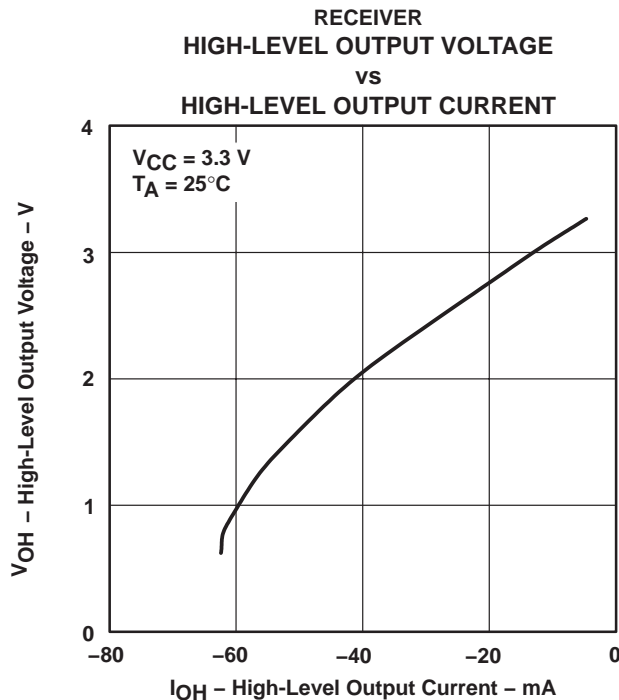


Figure 12

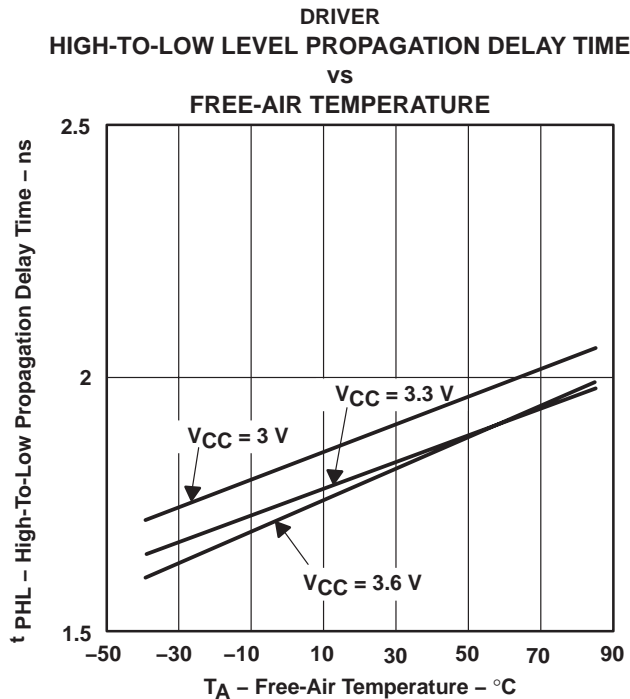


Figure 13

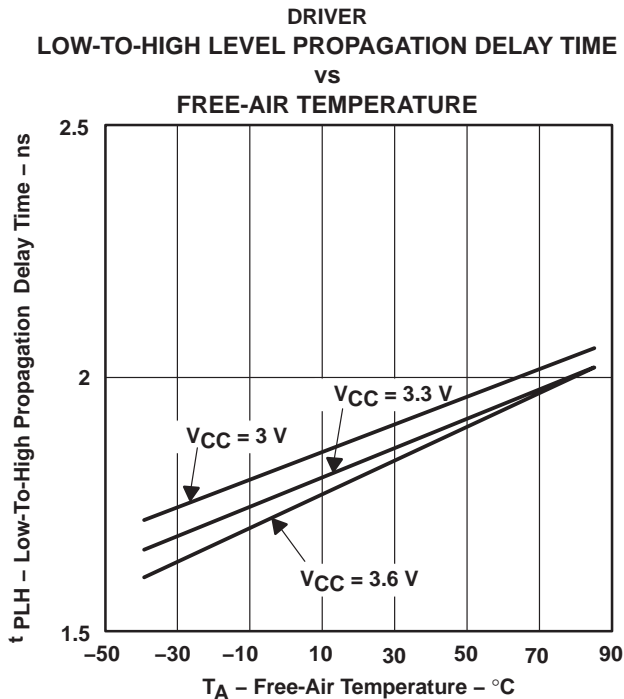


Figure 14



TYPICAL CHARACTERISTICS

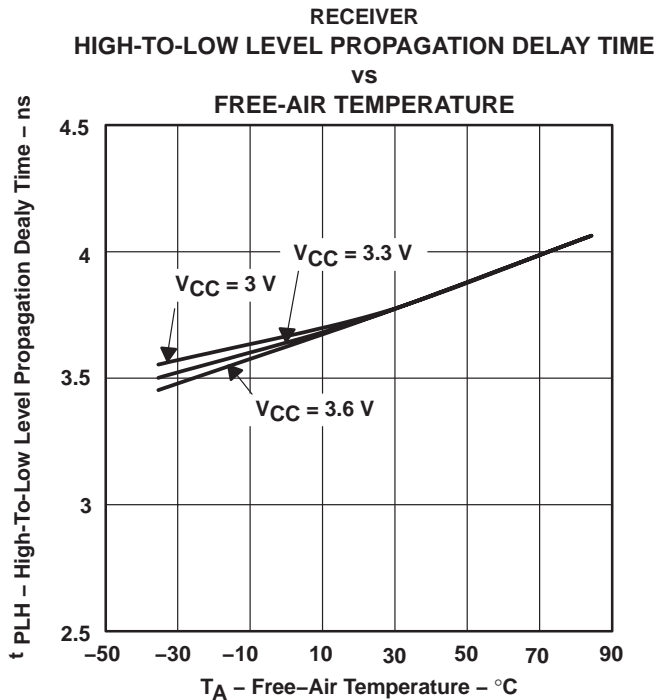


Figure 15

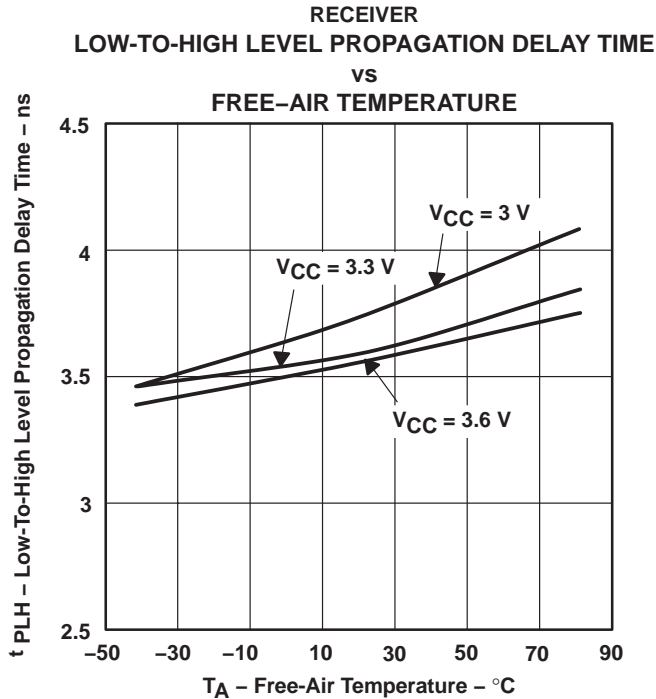


Figure 16

SN65LVDS179-Q1, SN65LVDS180-Q1, SN65LVDS050-Q1, SN65LVDS051-Q1 HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

SGLS204 – SEPTEMBER 2003

APPLICATION INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission. Ground differences are less than 1 V with a low common-mode output and balanced interface for very low noise emissions. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers maintain ECL speeds without the power and dual supply requirements.

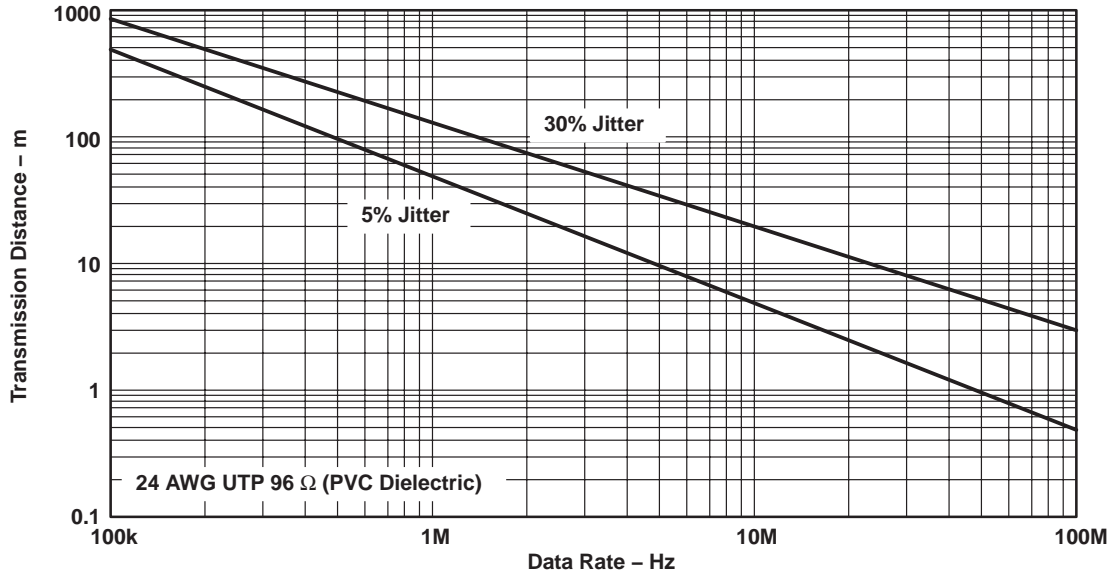


Figure 17. Data Transmission Distance Versus Rate

APPLICATION INFORMATION

fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between -100 mV and 100 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through $300\text{-k}\Omega$ resistors as shown in Figure 18. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

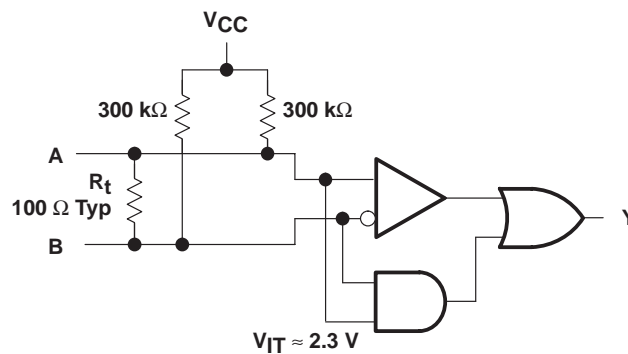


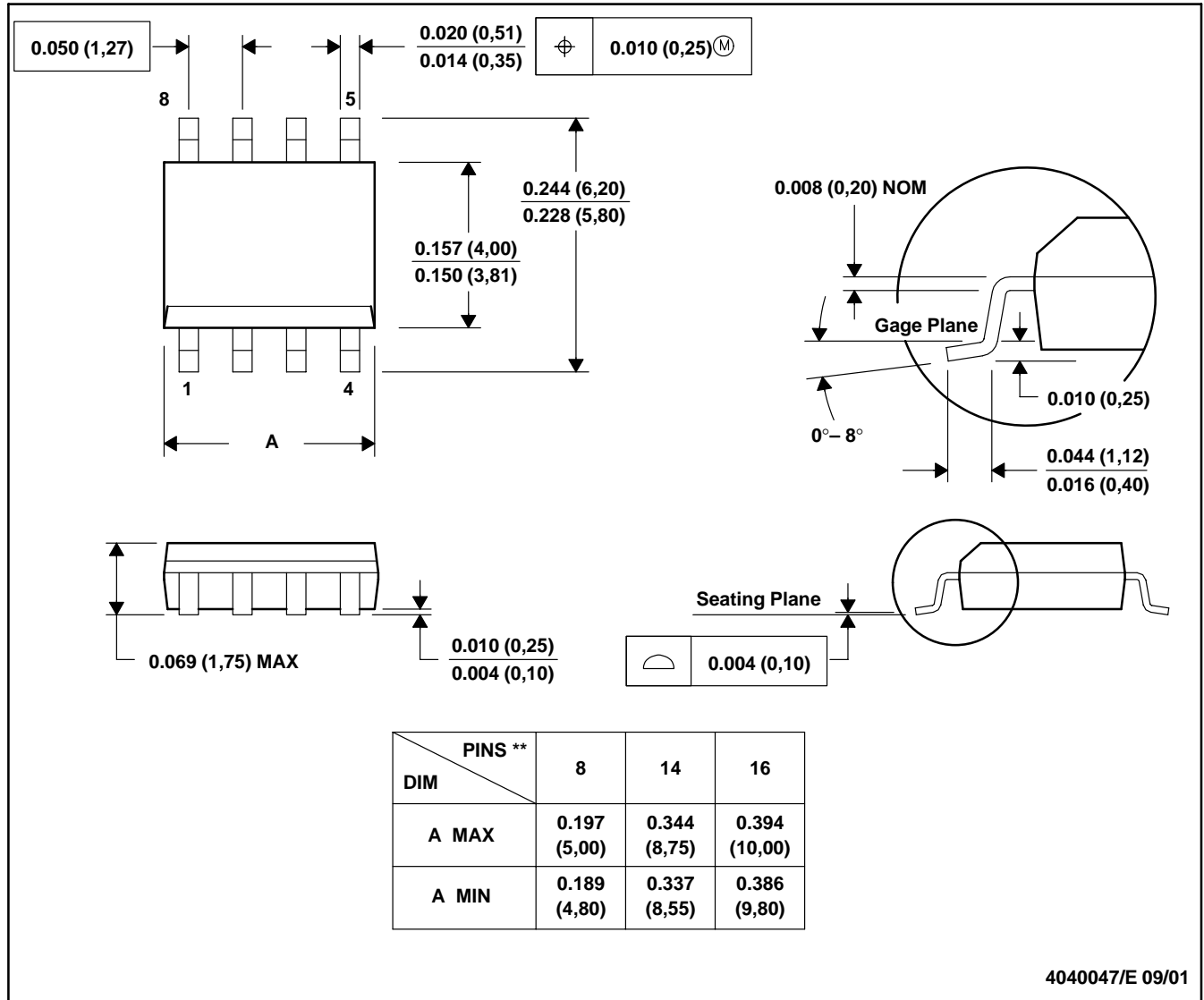
Figure 18. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, R_t , does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pull-up currents from the receiver and the fail-safe feature.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65LVDS051DRQ1	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN65LVDS051PWRQ1	ACTIVE	TSSOP	PW	16	2000	None	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS180DRQ1	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN65LVDS180PWRQ1	ACTIVE	TSSOP	PW	14	2000	None	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

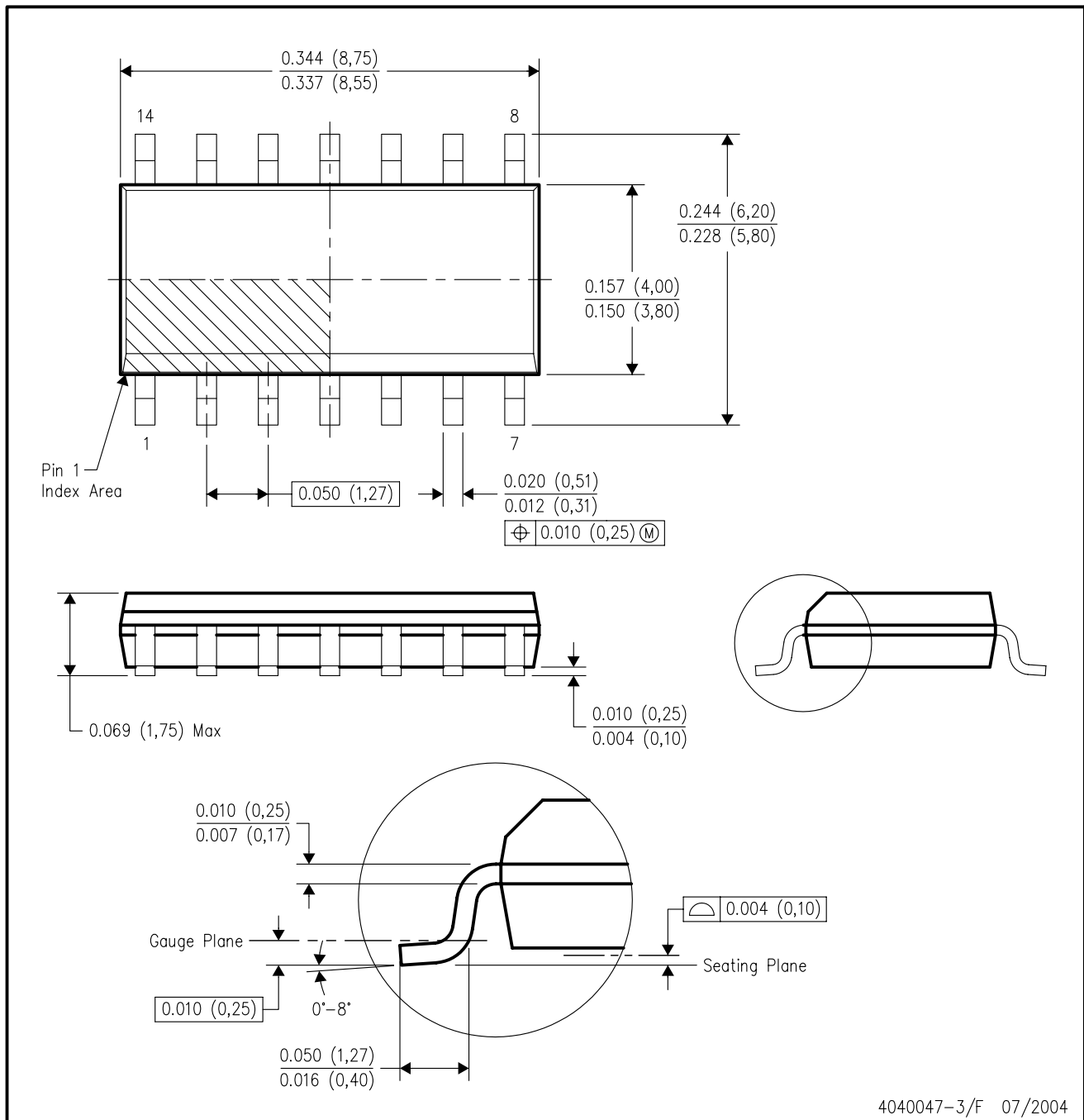
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265