

DUAL 4-PORT AND DUAL 8-PORT LVDS REPEATERS

FEATURES

- Two Line Receivers and Eight ('109) or Sixteen ('117) Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard
- Typical Data Signaling Rates to 400 Mbps or Clock Frequencies to 400 MHz
- Outputs Arranged in Pairs From Each Bank
- Enabling Logic Allows Individual Control of Each Driver Output Pair, Plus All Outputs
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load
- Electrically Compatible With LVDS, PECL, LVPECL, LVTTTL, LVCMOS, GTL, BTL, CTT, SSTL, or HSTL Outputs With External Termination Networks
- Propagation Delay Times < 4.5 ns
- Output Skew Less Than 550 ps Bank Skew Less Than 150 ps Part-to-Part Skew Less Than 1.5 ns
- Total Power Dissipation Typically < 500 mW With All Ports Enabled and at 200 MHz
- Driver Outputs or Receiver Input Equals High Impedance When Disabled or With $V_{CC} < 1.5$ V
- Bus-Pin ESD Protection Exceeds 12 kV
- Packaged in Thin Shrink Small-Outline Package With 20-Mil Terminal Pitch

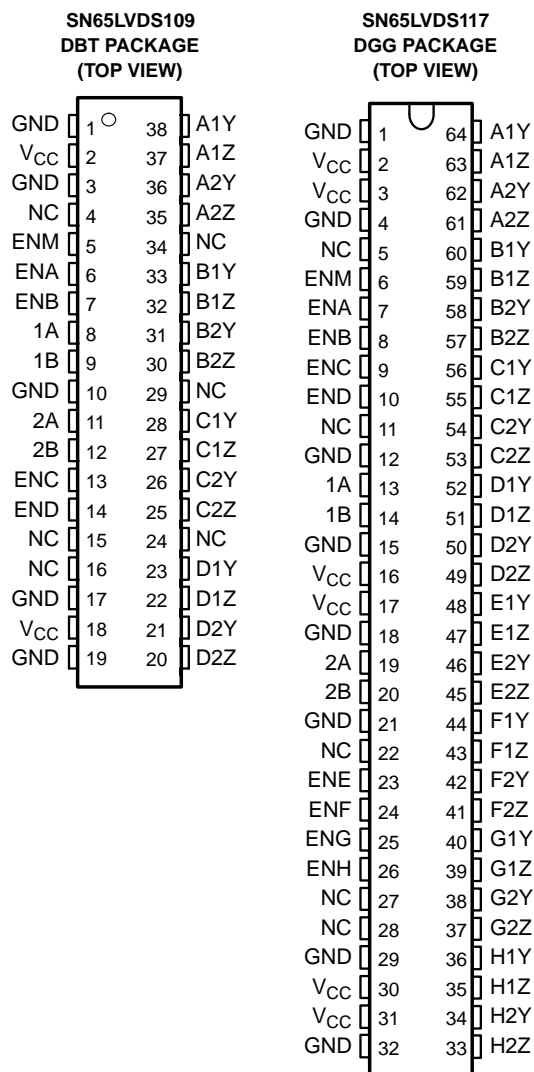
DESCRIPTION

The SN65LVDS109 and SN65LVDS117 are configured as two identical banks, each bank having one differential line receiver connected to either four ('109) or eight ('117) differential line drivers. The outputs are arranged in pairs having one output from each of the two banks. Individual output enables are provided for each pair of outputs and an additional enable is provided for all outputs.

The line receivers and line drivers implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS, as specified in EIA/TIA-644, is a data signaling technique that offers low power, low noise emission, high noise immunity, and high switching speeds. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

The intended application of these devices, and the LVDS signaling technique, is for point-to-point or point-to-multipoint (distributed simplex) baseband data transmission on controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same silicon substrate, along with the low pulse skew of balanced signaling, provides extremely precise timing alignment of the signals being repeated from the inputs. This is particularly advantageous for implementing system clock and data distribution trees.

The SN65LVDS109 and SN65LVDS117 are characterized for operation from -40°C to 85°C.

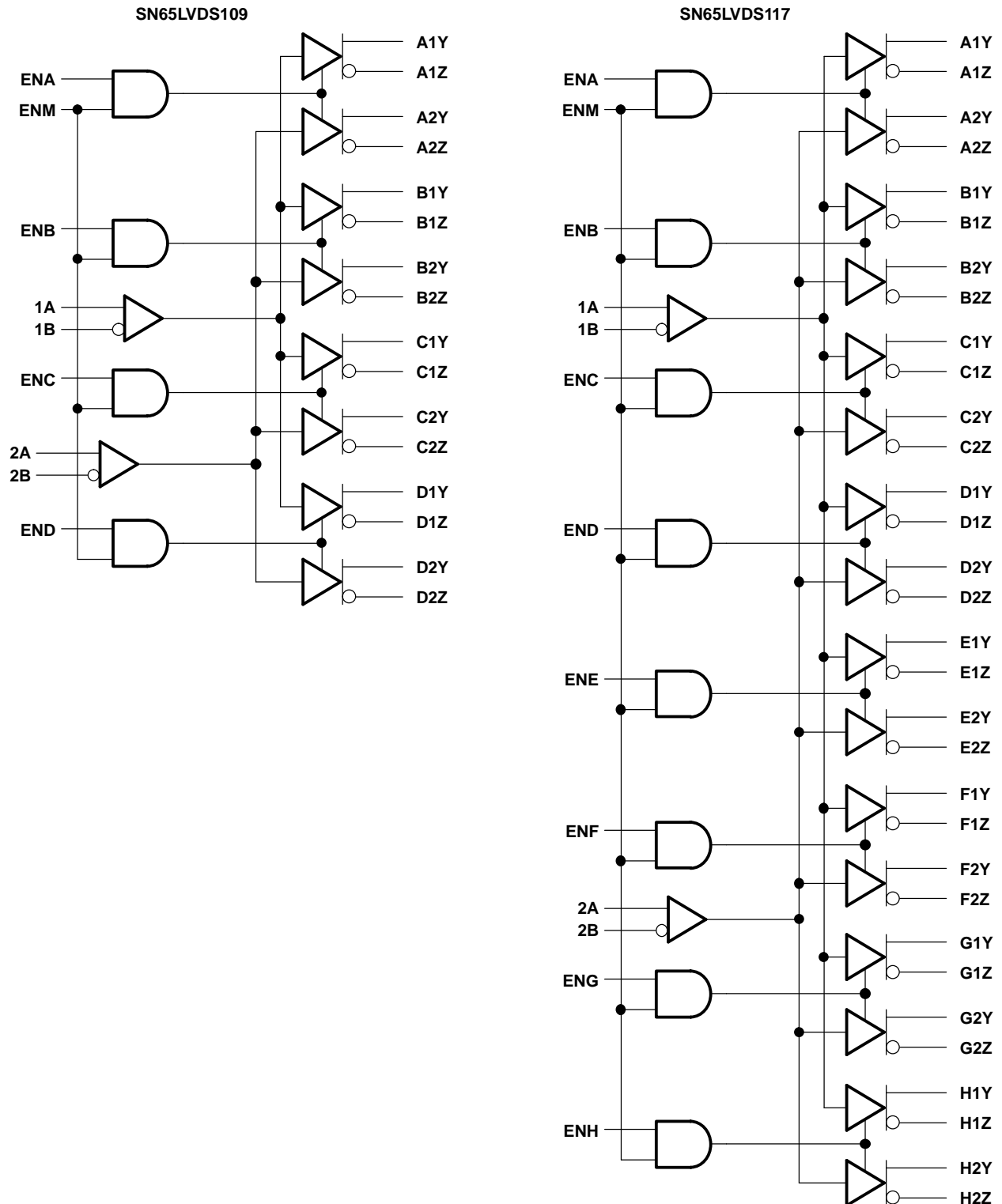


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LOGIC DIAGRAM (POSITIVE LOGIC)



SELECTION GUIDE TO LVDS SPLITTERS

The SN65LVDS109 and SN75LVDS117 are both members of a family of LVDS splitters and repeaters. A brief overview of the family is provided by Table 1.

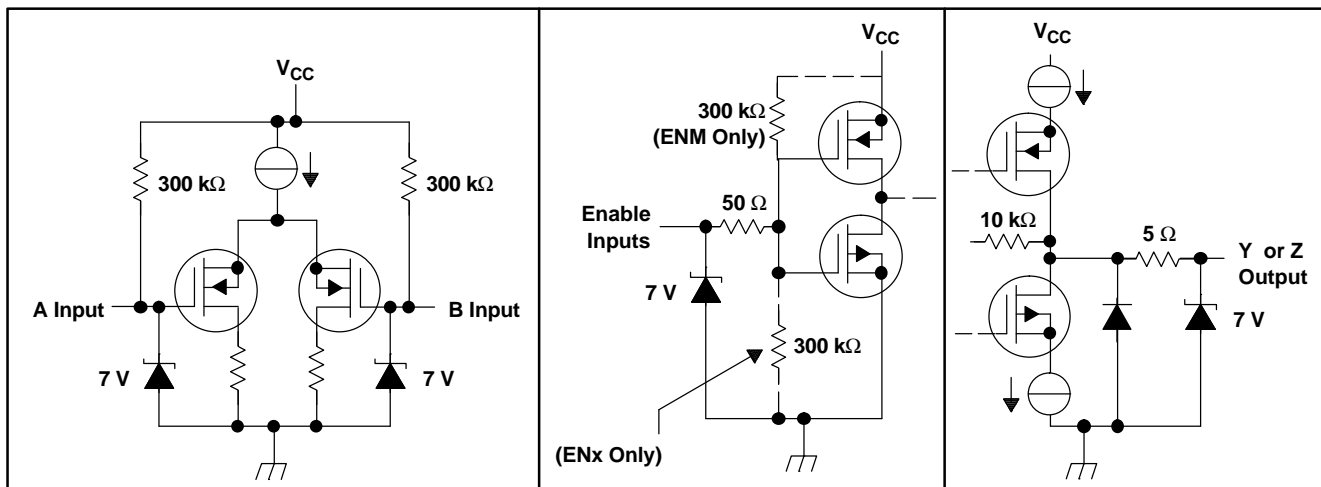
Table 1. LVDS SPLITTER AND REPEATER FAMILY

DEVICE	NUMBER OF INPUTS	NUMBER OF OUTPUTS	PACKAGE	COMMENTS
SN65LVDS104	1 LVDS	4 LVDS	16-pin D	4-Port LVDS repeater
SN65LVDS105	1 LVTTTL	4 LVDS	16-pin D	4-Port TTL-to-LVDS repeater
SN65LVDS108	1 LVDS	8 LVDS	38-pin DBT	8-Port LVDS repeater
SN65LVDS109	2 LVDS	8 LVDS	38-pin DBT	Dual 4-port LVDS repeater
SN65LVDS116	1 LVDS	16 LVDS	64-pin DGG	16-Port LVDS repeater
SN65LVDS117	2 LVDS	16 LVDS	64-pin DGG	Dual 8-Port LVDS repeater

FUNCTION TABLE

INPUTS			OUTPUTS	
$V_{ID} = V_A - V_B$	ENM	ENx	$\bar{x}Y$	$\bar{x}Z$
X	L	X	Z	Z
X	X	L	Z	Z
$V_{ID} \geq 100 \text{ mV}$	H	H	H	L
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	H	H	?	?
$V_{ID} \leq -100 \text{ mV}$	H	H	L	H

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		UNIT
Supply voltage range, V_{CC} ⁽²⁾		–0.5 V to 4 V
Input voltage range	Enable inputs	–0.5 V to 6 V
	A, B, Y or Z	–0.5 V to 4 V
Electrostatic discharge	A, B, Y, Z, and GND ⁽³⁾	Class 3, A:12 kV, B: 500 V
Continuous power dissipation		See Dissipation Rating Table
Storage temperature range		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
DBT	1277 mW	10.2 mW/°C	644 mW
DGG	2094 mW	16.7 mW/°C	1089 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common-mode)	0		$V_{CC} - 0.8$	V
T_A	Operating free-air temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 1 and Table 2			100	mV	
V_{ITH-}	Negative-going differential input voltage threshold				-100		
$ V_{OD} $	Differential output voltage magnitude	$R_L = 100 \Omega$, $V_{ID} = \pm 100$ mV, See Figure 1 and Figure 2	247	340	454	mV	
$\Delta V_{OD} $	Change in differential output voltage magnitude between logic states		-50		50		
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.37 5	V	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50		150	
I_{CC}	Supply current	SN65LVDS109	Enabled, $R_L = 100 \Omega$		46	64	mA
			Disabled		6	8	
		SN65LVDS117	Enabled, $R_L = 100 \Omega$		85	122	
			Disabled		6	8	
I_I	Input current (A or B inputs)	$V_I = 0$ V		-2	-20	μ A	
		$V_I = 2.4$ V		-1.2			
$I_{I(OFF)}$	Power-off input current (A or B inputs)	$V_{CC} = 1.5$ V, $V_I = 2.4$ V			20	μ A	
I_{IH}	High-level input current (enables)	$V_{IH} = 2$ V			20	μ A	
I_{IL}	Low-level input current (enables)	$V_{IL} = 0.8$ V			10	μ A	
I_{OS}	Short-circuit output current	V_{OY} or $V_{OZ} = 0$ V			± 24	mA	
		$V_{OD} = 0$ V			± 12		
I_{OZ}	High-impedance output current	$V_O = 0$ V or V_{CC}			± 1	μ A	
$I_{O(OFF)}$	Power-off output current	$V_{CC} = 1.5$ V, $V_O = 3.6$ V			± 1	μ A	
C_{IN}	Input capacitance (A or B inputs)	$V_I = 0.4 \sin(4E6\pi t) + 0.5$ V			5	pF	
C_O	Output capacitance (Y or Z outputs)	$V_I = 0.4 \sin(4E6\pi t) + 0.5$ V, Disabled			9.4		

(1) All typical values are at 25°C and with a 3.3-V supply.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$R_L = 100 \Omega, C_L = 10 \text{ pF}$, See Figure 4	1.6	2.8	4.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.6	2.8	4.5	
t_r	Differential output signal rise time		0.3	0.8	1.2	ns
t_f	Differential output signal fall time		0.3	0.8	1.2	
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $) ⁽²⁾		140	500		ps
$t_{sk(o)}$	Output skew ⁽³⁾		100	550		
$t_{sk(b)}$	Bank skew ⁽⁴⁾		40	150		ps
$t_{sk(pp)}$	Part-to-part skew ⁽⁵⁾			1.5		ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5	5.7	15		ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output		7.7	15		
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output		3.2	15		
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output		3.2	15		

- (1) All typical values are at 25°C and with a 3.3-V supply.
- (2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.
- (3) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of any outputs with both inputs tied together.
- (4) $t_{sk(b)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of the two outputs of any bank of a single device.
- (5) $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

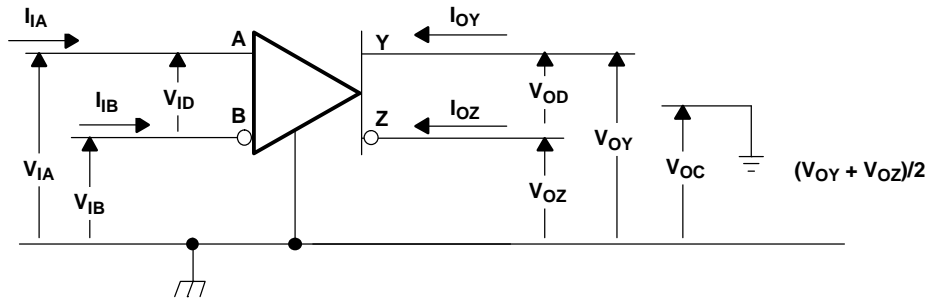


Figure 1. Voltage and Current Definitions

Table 2. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V _{IA}	V _{IB}	V _{ID}	V _{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	-100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	-100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	-100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	-600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	-600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	-600 mV	0.3 V

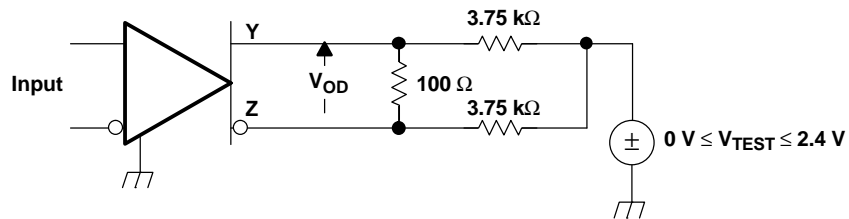
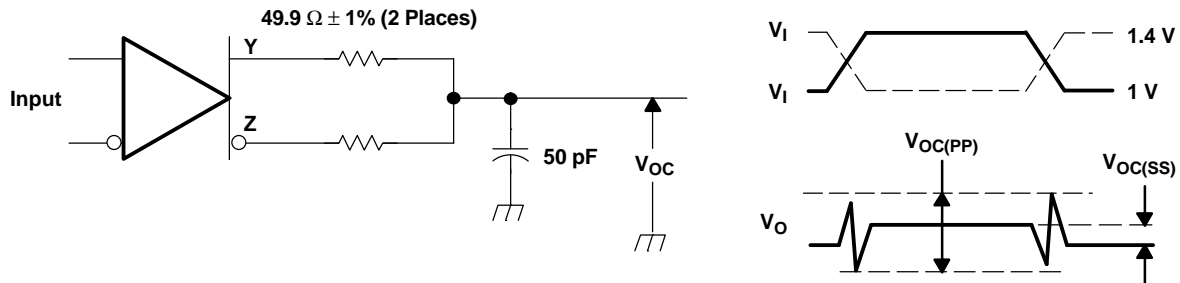
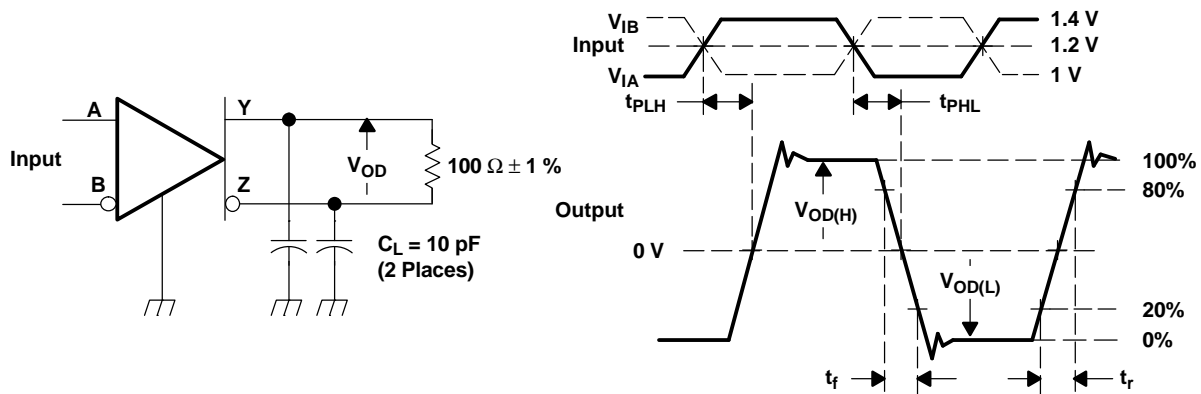


Figure 2. V_{OD} Test Circuit



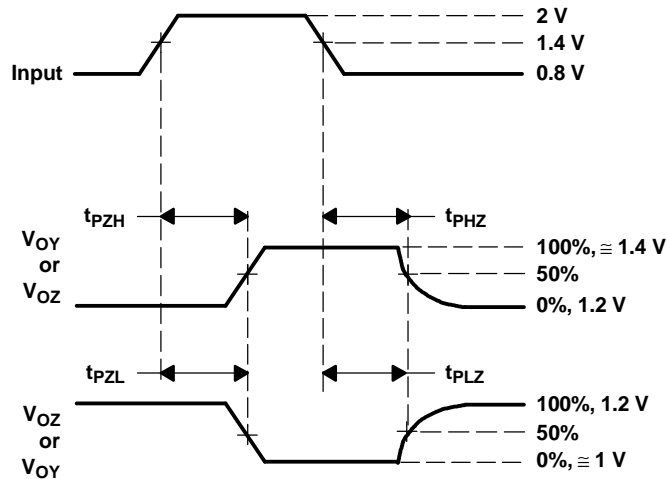
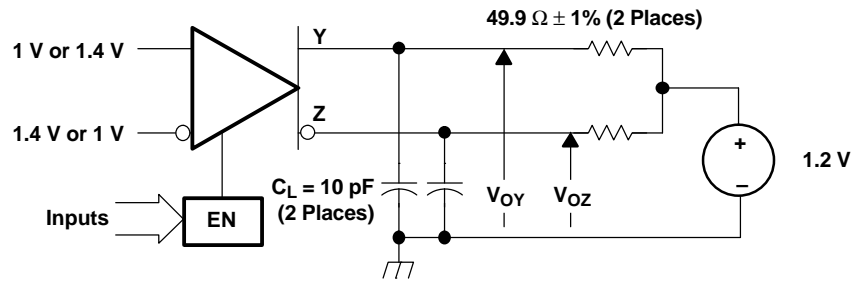
- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1 \text{ ns}$, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = $500 \pm 10 \text{ ns}$. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

TYPICAL CHARACTERISTICS

SN65LVDS109
SUPPLY CURRENT
VS
SWITCHING FREQUENCY

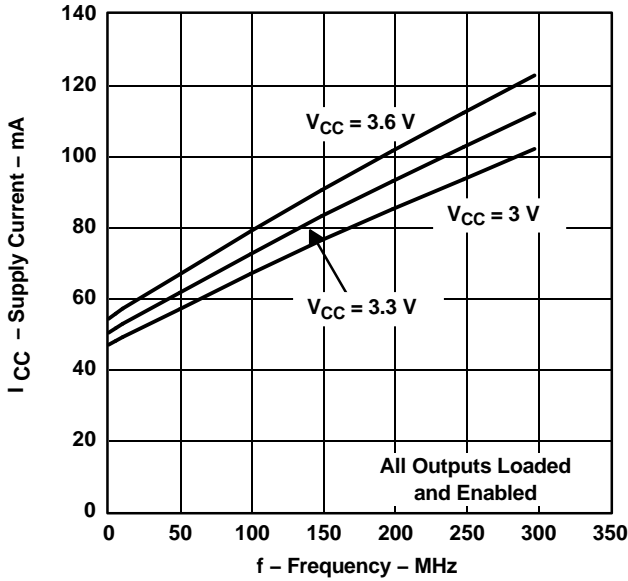


Figure 6.

SN65LVDS117
SUPPLY CURRENT
VS
SWITCHING FREQUENCY

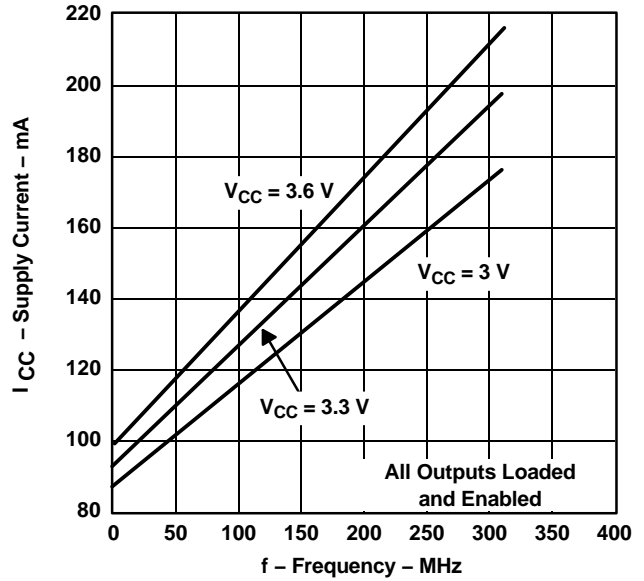


Figure 7.

LOW-TO-HIGH PROPAGATION DELAY TIME
VS
FREE-AIR TEMPERATURE

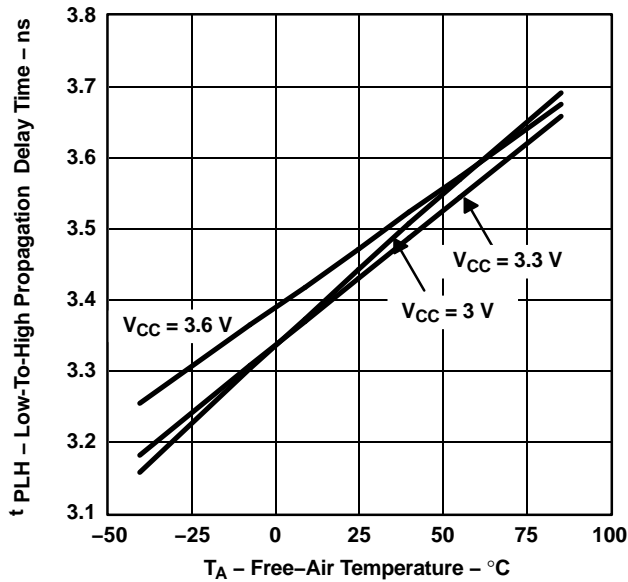


Figure 8.

HIGH-TO-LOW PROPAGATION DELAY TIME
VS
FREE-AIR TEMPERATURE

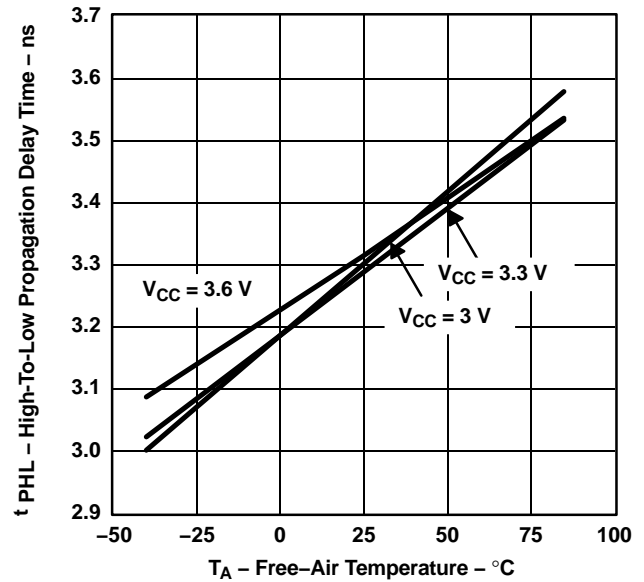
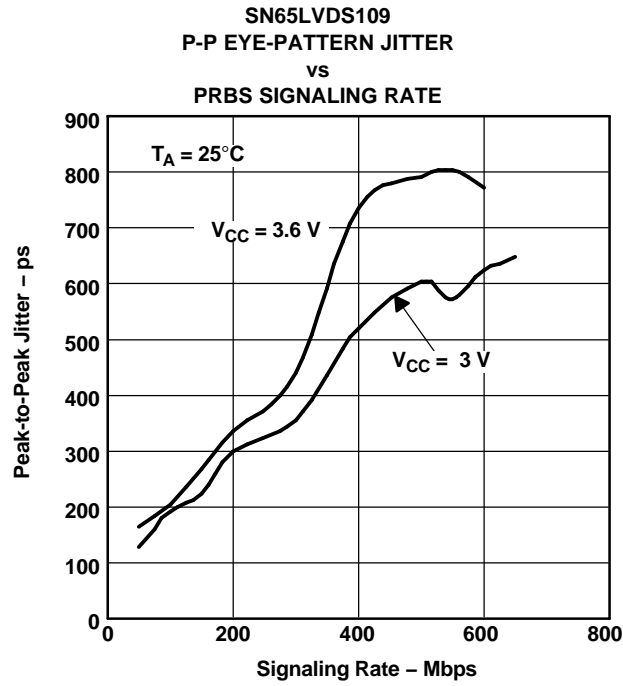


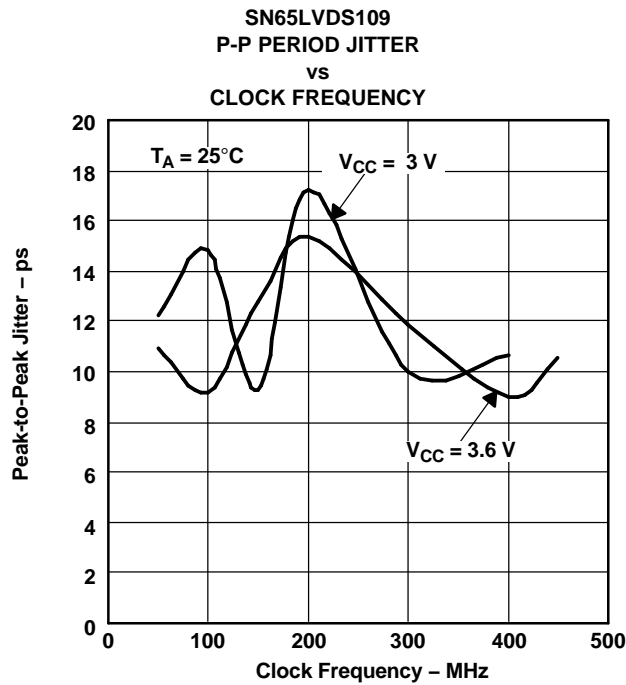
Figure 9.

TYPICAL CHARACTERISTICS (continued)



NOTES: Input: 2^{15} PRBS with peak-to-peak jitter < 100 ps at 100 Mbps, all outputs enabled and loaded with differential 100- Ω loads, worst-case output, supply decoupled with 0.1- μ F and 0.001- μ F ceramic 0603-style capacitors placed 1 cm from the device.

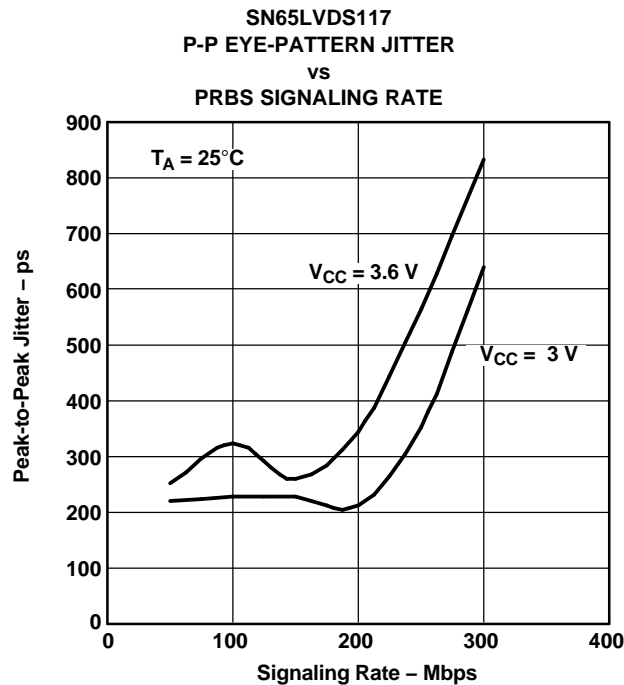
Figure 10.



NOTES: Input: 50% duty cycle square wave with jitter period < 10 ps at 100 MHz, all outputs enabled and loaded with differential 100- Ω loads, worst-case output, supply decoupled with 0.1- μ F and 0.001- μ F ceramic 0603-style capacitors 1 cm from the device.

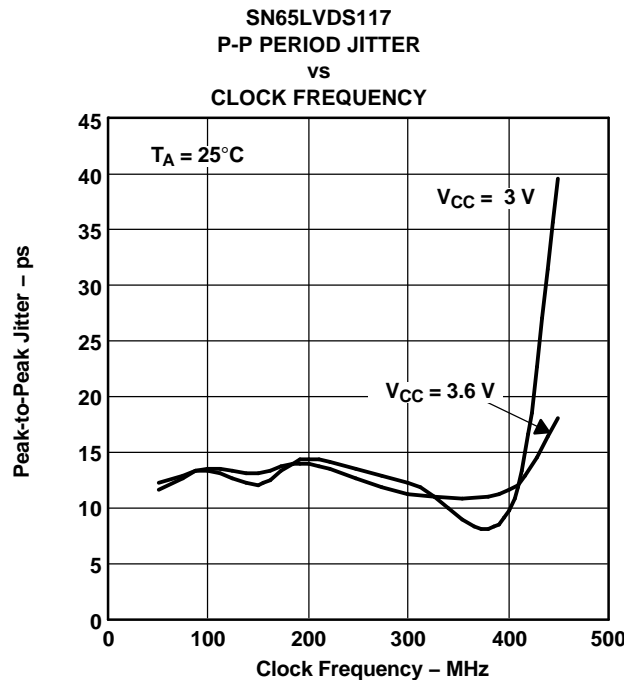
Figure 11.

TYPICAL CHARACTERISTICS (continued)



NOTES: Input: 2¹⁵ PRBS with peak-to-peak jitter < 115 ps at 100 Mbps, all outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-μF and 0.001-μF ceramic 0805-style capacitors 1 cm from the device.

Figure 12.



NOTES: Input: 50% duty cycle square wave with jitter period < 10 ps at 100 MHz, all outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-μF and 0.001-μF ceramic 0805-style capacitors 1 cm from the device.

Figure 13.

TYPICAL CHARACTERISTICS (continued)

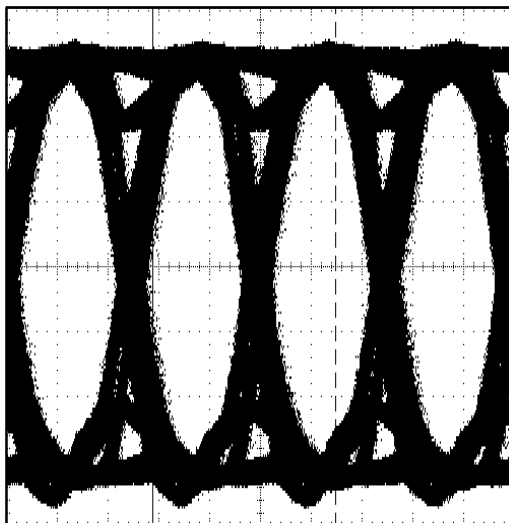


Figure 14. Typical Differential Eye Pattern at 400 Mbps

APPLICATION INFORMATION

FAIL SAFE

A common problem with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between -100 mV and 100 mV and within its recommended input common-mode voltage range. However, TI LVDS receivers handles the open-input circuit situation differently.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near V_{CC} through $300\text{-k}\Omega$ resistors as shown in Figure 15. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

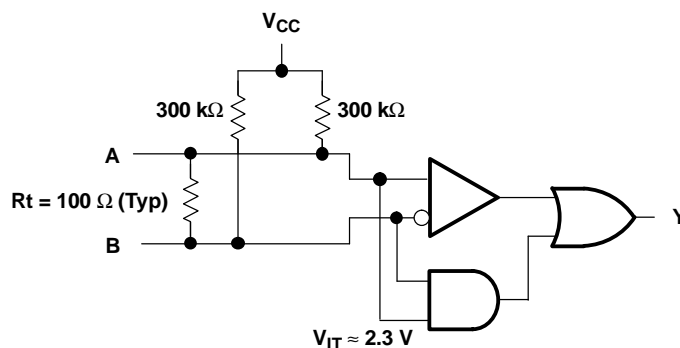


Figure 15. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100 mV differential input voltage magnitude. The presence of the termination resistor, R_t , does not affect the fail-safe function as long as it is connected as shown in Figure 15. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

CLOCK DISTRIBUTION

The SN65LVDS109 and SN65LVDS117 devices solve several problems common to the distribution of timing critical clock and data signals. These problems include:

- Excessive skew between the signals
- Noise pickup over long signaling paths
- High power consumption
- Control of which signal paths are enabled or disabled
- Elimination of radiation from unterminated lines

Buffering and splitting the two related signals on the same silicon die minimizes corruption of the timing relation between the two signals. Buffering and splitting the two signals in separate devices will introduce considerably higher levels of uncontrolled timing skew between the two signals. Higher speed operation and more timing tolerance for other components of the system is enabled by the tighter system timing budgets provided by the single die implementations of the SN65LVDS109 and SN65LVDS117.

The use of LVDS signaling technology for both the inputs and the outputs provides superior common-mode and noise tolerance compared to single-ended I/O technologies. This is particularly important because the signals that are being distributed must be transmitted over longer distances, and at higher rates, than can be accommodated with single-ended I/Os. In addition, LVDS consumes considerably less power than other high-performance differential signaling schemes.

APPLICATION INFORMATION (continued)

The enable inputs provided for each output pair may be used to turn on or off any of the paths. This function is required to prevent radiation of signals from the unterminated signal lines on open connectors, such as when boards or devices are being swapped in the end equipment. The individual bank enables are also required if redundant paths are being utilized for reliability reasons.

The diagram below shows how a pair of clock (C) and data (D) input signals is being identically repeated out two of the available output pairs. A third output pair is shown in the disabled state.

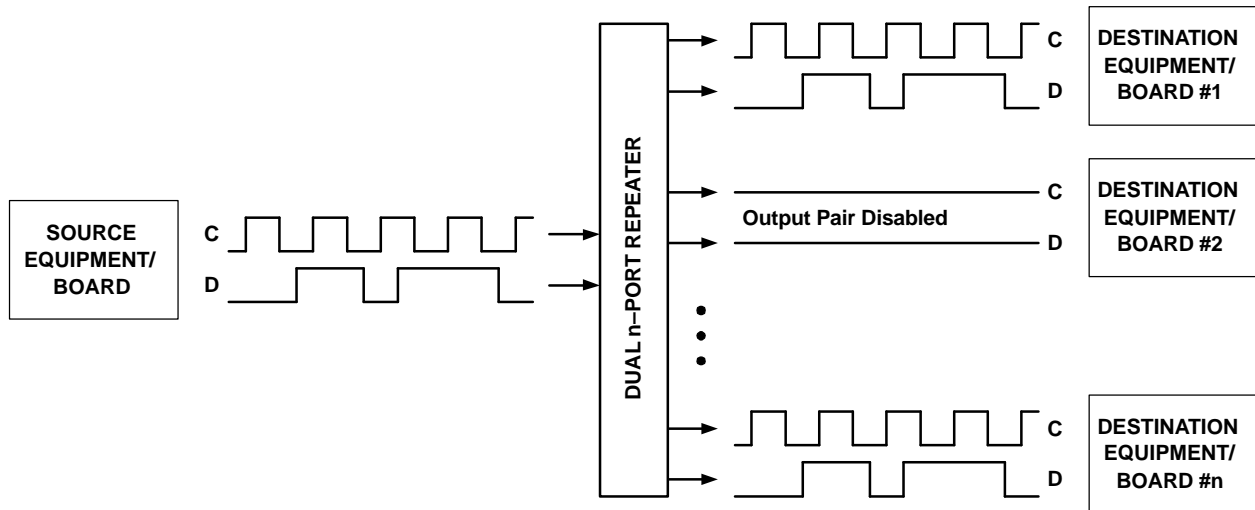


Figure 16. LVDS Repeating Splitter Application Example Showing Individual Path Control

INPUT LEVEL TRANSLATION

An LVDS receiver can be used to receive various other types of logic signals. Figure 17 through Figure 25 show the termination circuits for SSTL, HSTL, GTL, BTL, LVPECL, PECL, CMOS, and TTL.

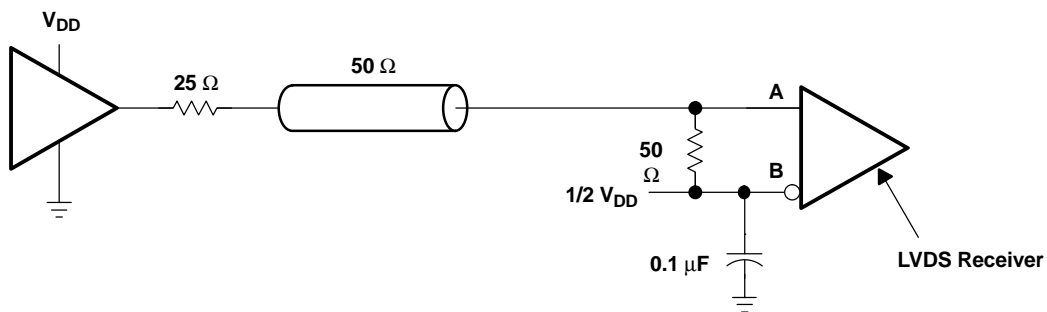


Figure 17. Stub-Series Terminated (SSTL) or High-Speed Transceiver Logic (HSTL)

APPLICATION INFORMATION (continued)

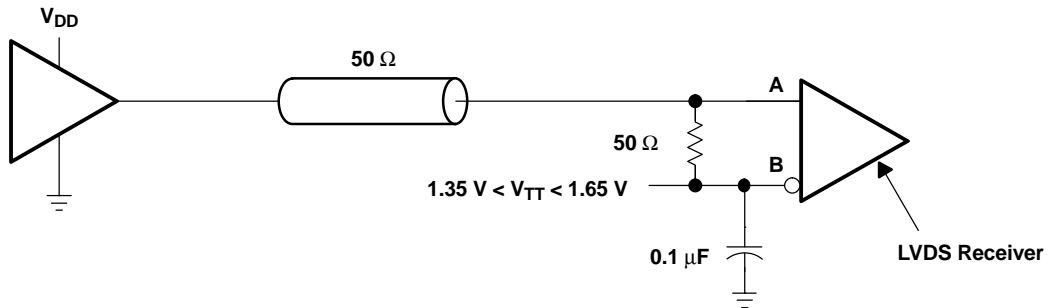


Figure 18. Center-Tap Termination (CTT)

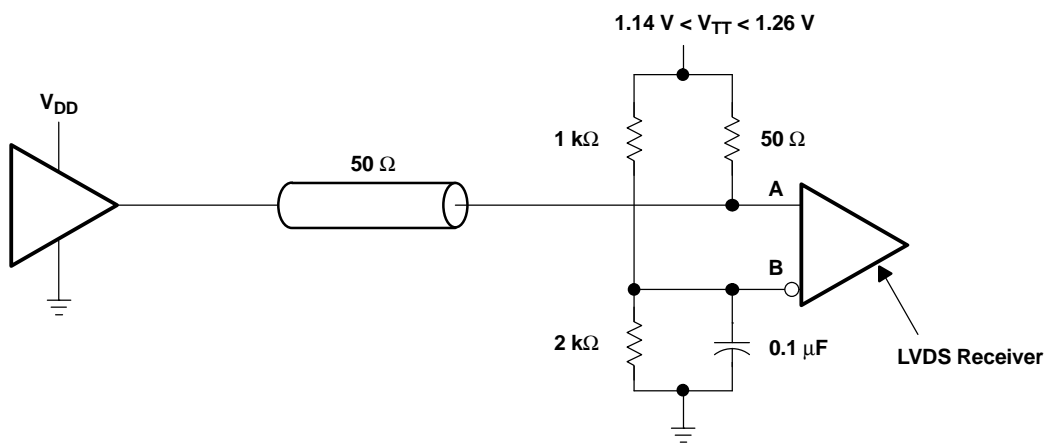


Figure 19. Gunning Transceiver Logic (GTL)

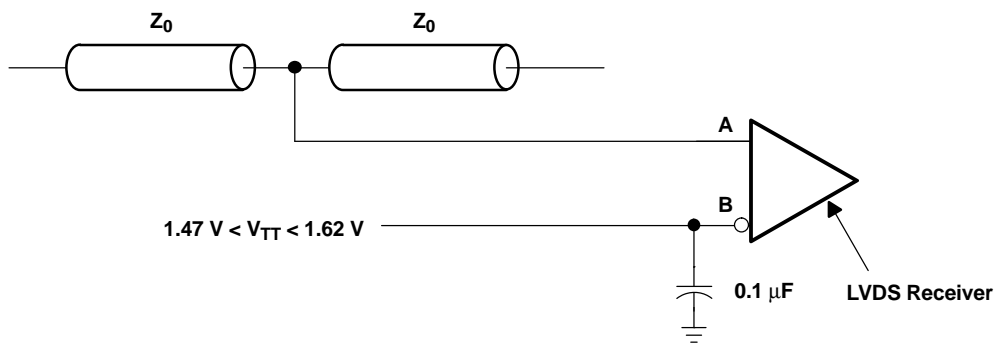


Figure 20. Backplane Transceiver Logic (BTL)

APPLICATION INFORMATION (continued)

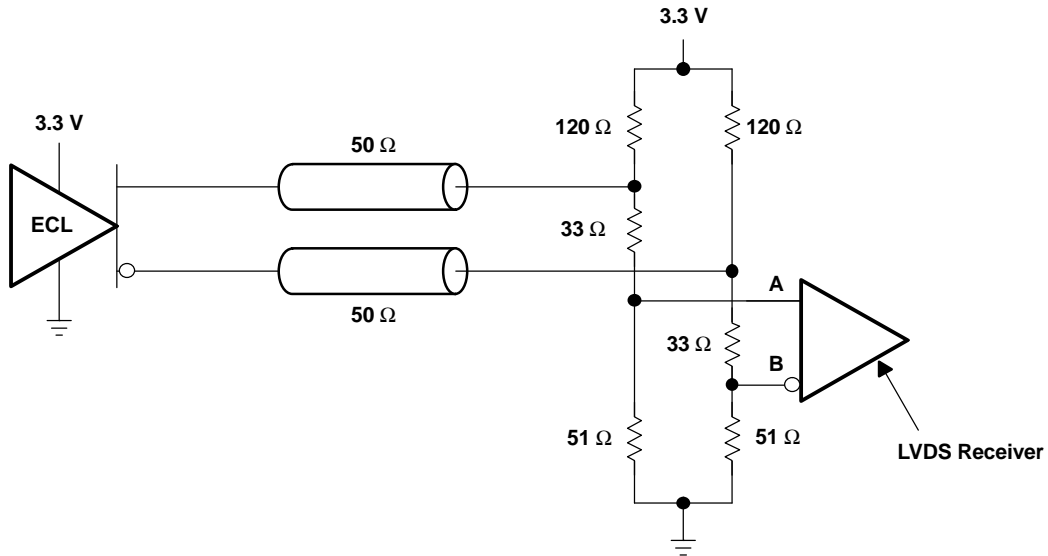


Figure 21. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

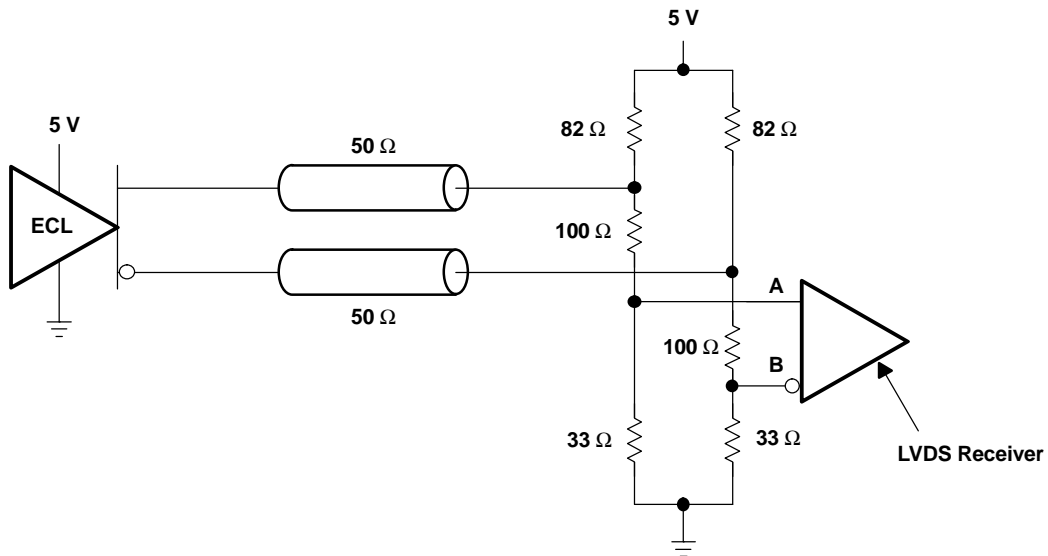


Figure 22. Positive Emitter-Coupled Logic (PECL)

APPLICATION INFORMATION (continued)

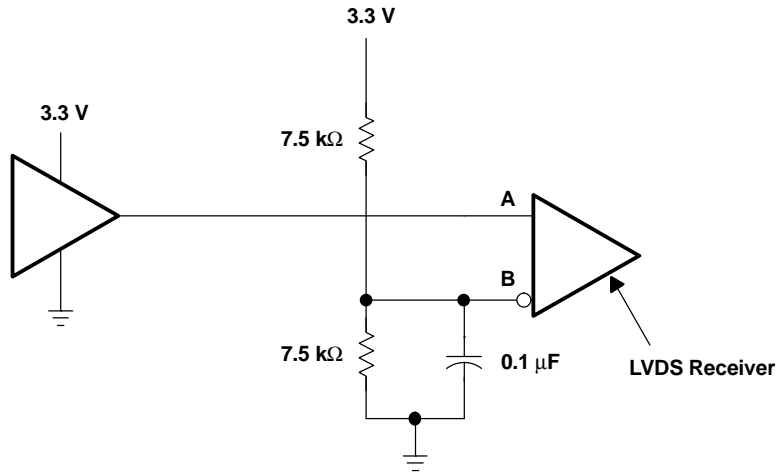


Figure 23. 3.3-V CMOS

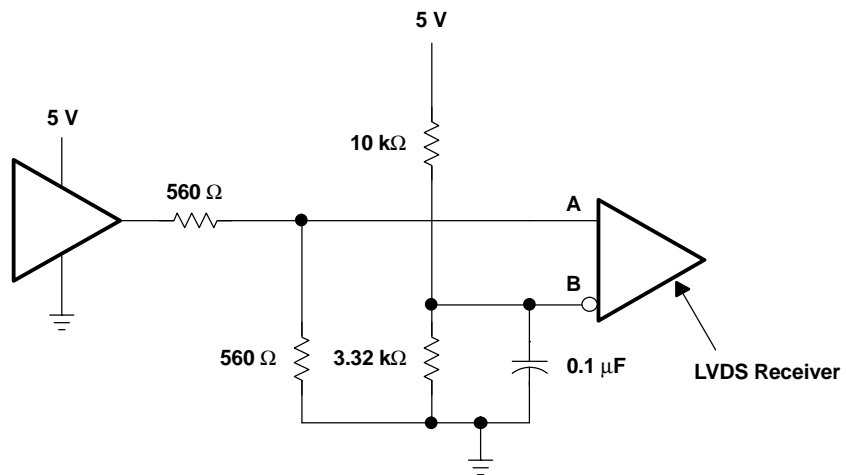


Figure 24. 5-V CMOS

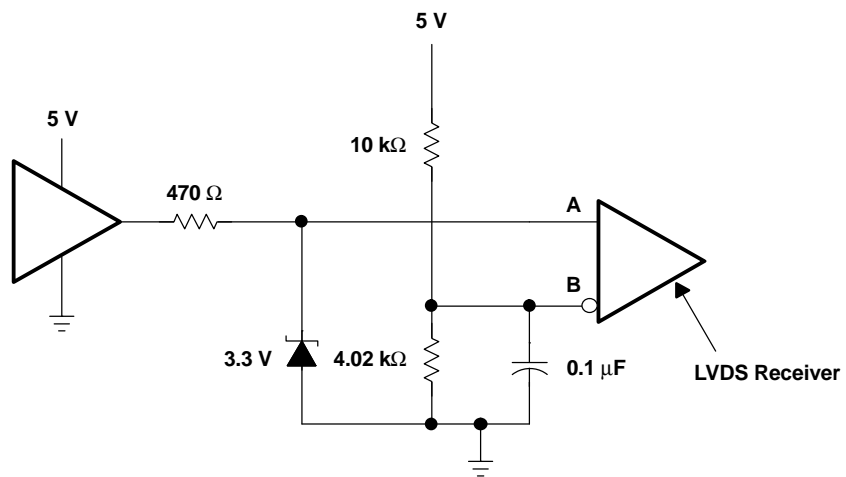


Figure 25. TTL

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65LVDS109DBT	ACTIVE	SM8	DBT	38	50	None	CU NIPDAU	Level-2-220C-1 YEAR
SN65LVDS109DBTR	ACTIVE	SM8	DBT	38	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
SN65LVDS109DBTRG4	PREVIEW	SM8	DBT	38	2000	None	Call TI	Call TI
SN65LVDS117DGG	ACTIVE	TSSOP	DGG	64	25	None	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS117DGGR	ACTIVE	TSSOP	DGG	64	2000	None	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS117DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

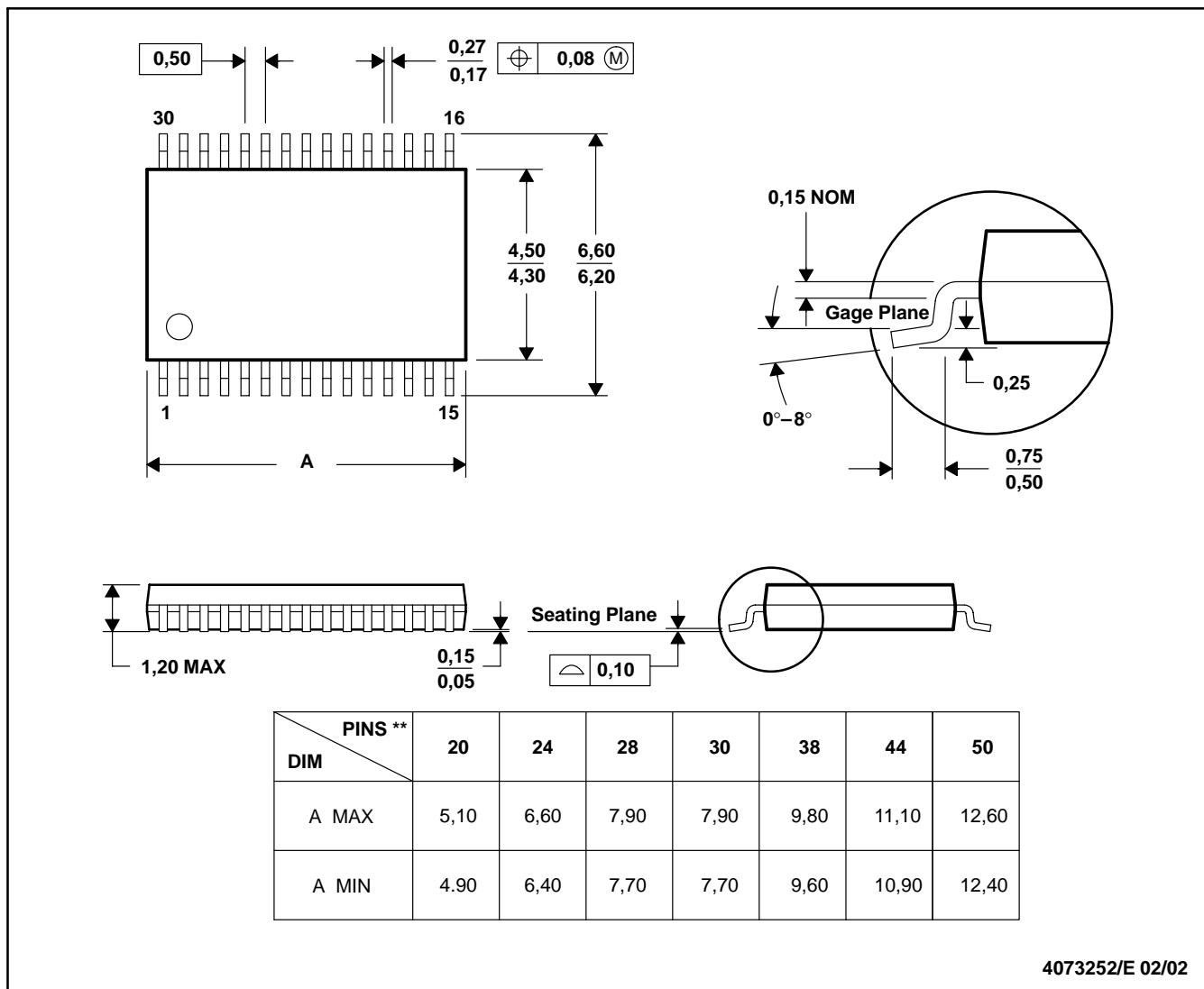
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DBT (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

30 PINS SHOWN



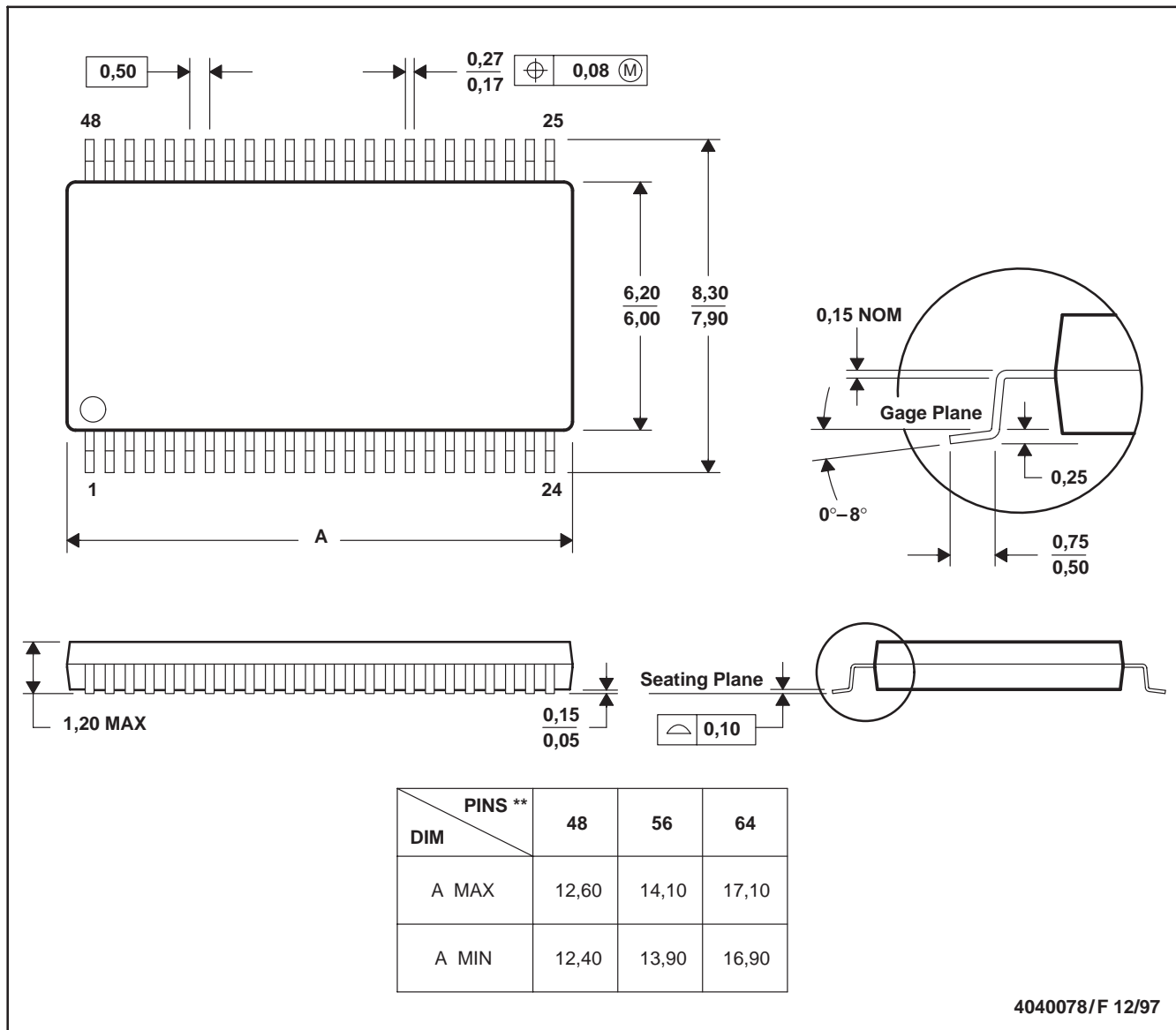
4073252/E 02/02

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-153

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265