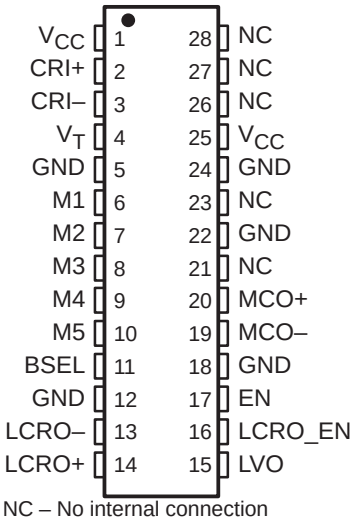
- **A Member of the MuxIt™ Serializer-Deserializer Building-Block Chip Family**
- **Pin Selectable Frequency Multiplier Ratios Between 4 and 40**
- **Input Clock Frequencies From 5 to 50 MHz**
- **Multiplied Clock Frequencies up to 400 MHz**
- **Internal Loop Filters and Low PLL-Jitter of 20 ps RMS Typical at 200 MHz**
- **LVDS Compatible Differential Inputs and Outputs Meet or Exceed the Requirements of ANSI EIA/TIA-644-A**
- **LVTTL Compatible Inputs Are 5 V Tolerant**
- **LVDS Inputs and Outputs ESD Protection Exceeds 12 kV HBM**
- **Operates From a Single 3.3 V Supply**
- **Packaged in 28-Pin Thin Shrink Small-Outline Package With 26 mil Terminal Pitch**

SN65LVDS150
PW PACKAGE
(Marked as 65LVDS150)



NC – No internal connection

description

The MuxIt is a family of general-purpose, multiple-chip building blocks for implementing parallel data serializers and deserializers. The system allows for wide parallel data to be transmitted through a reduced number of differential transmission lines over distances greater than can be achieved with a single-ended (e.g., LVTTL or LVCMOS) data interface. The number of bits multiplexed per transmission line is user selectable, allowing for higher transmission efficiencies than with other existing fixed ratio solutions. MuxIt utilizes the LVDS (TIA/EIA-644) low voltage differential signaling technology for communications between the data source and data destination.

The MuxIt family initially includes three devices supporting simplex communications; *The SN65LVDS150 Phase Locked Loop-Frequency Multiplier, The SN65LVDS151 Serializer-Transmitter,* and *The SN65LVDS152 Receiver-Deserializer.*

The SN65LVDS150 is a PLL based frequency multiplier designed for use with the other members of the MuxIt family of serializers and deserializers. The frequency multiplication ratio is pin selectable over a wide range of values from 4 through 40 to accommodate a broad spectrum of user needs. No external filter components are needed. A PLL lock indicator output is available which may be used to enable link data transfers.

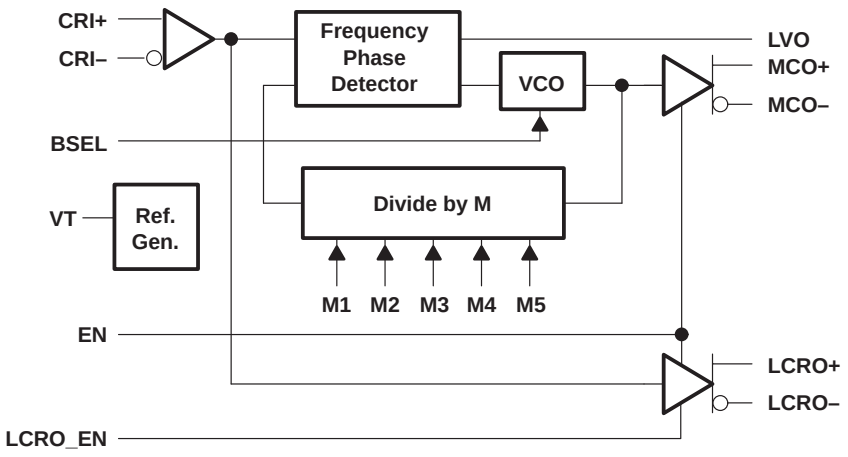
description (continued)

The design of the SN65LVDS150 allows it to be used at either the transmit end or the receive end of the MuxIt serial link. The differential clock reference input (CRI) is driven by the system's parallel data clock when at the source end of the link, or by the link clock when at the destination end of the link. The differential clock reference input may be driven by either an LVDS differential signal, or by a single ended clock of either polarity. For single-ended use the nonclocked input is biased to the logic threshold voltage. A $V_{CC}/2$ threshold reference, VT, is provided on a pin adjacent the differential CRI pins for convenience when the input is used in a single-ended mode.

The multiplied clock output (MCO) is an LVDS differential signal used to drive the high-speed shift registers in either the SN65LVDS151 serializer-transmitter or the SN65LVDS152 receiver-deserializer. The link clock reference output (LCRO) is an LVDS differential signal provided to the SN65LVDS151 serializer-transmitter for transmission over the link.

An internal power on reset and an enable input (EN) control the operation of the SN65LVDS150. When V_{CC} is below 1.5 V, or when EN is low, the device is in a low power disabled state and the MCO and LCRO differential outputs are in a high-impedance state. When V_{CC} is above 3 V and EN is high, the device and the two differential outputs are enabled and operating to specifications. The link clock reference output enable input (LCRO_EN) is used to turn off the LCRO output when it is not being used. A band select input (BSEL) is used to optimize the VCO performance as a function of M-clock frequencies and M multiplier that is being used: The f_{max} parameter in the switching characteristic table includes details on the MCO frequency and choices of BSEL and M.

block diagram

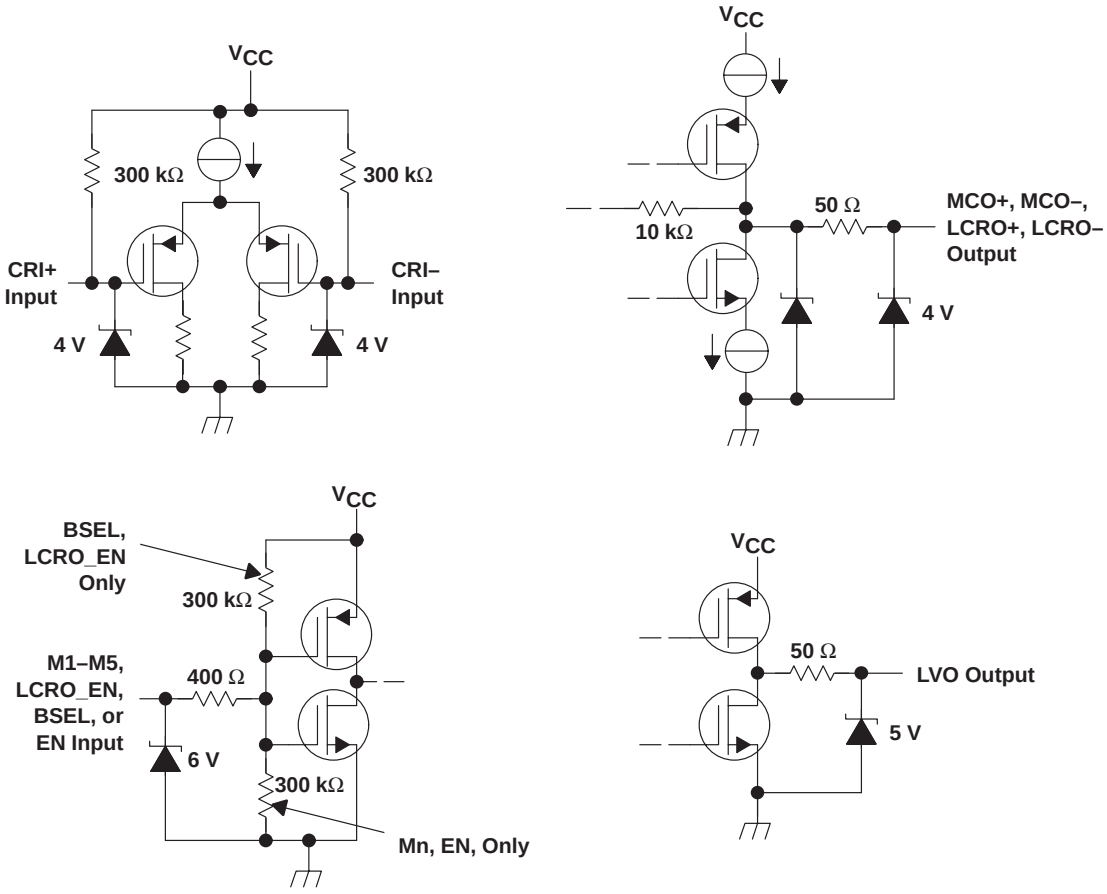


frequency multiplier value table

MULTIPLIER (m)	M1	M2	M3	M4	M5	RECOMMENDED f_{IN} (MHz)	
						BSEL = 0	BSEL = 1
4	L	L	L	L	L	$f_{IN} < 12.50$	$12.50 \le f_{IN}$
†	L	L	L	L	H	NA	NA
6	L	L	L	H	L	$f_{IN} < 8.33$	$8.33 \le f_{IN}$
†	L	L	L	H	H	NA	NA
8	L	L	H	L	L	$f_{IN} < 12.50$	$12.50 \le f_{IN}$
9	L	L	H	L	H	$f_{IN} < 11.11$	$11.11 \le f_{IN}$
10	L	L	H	H	L	$f_{IN} < 10.00$	$10.00 \le f_{IN}$
†	L	L	H	H	H	NA	NA
12	L	H	L	L	L	$f_{IN} < 8.3$	$8.3 \le f_{IN}$
13	L	H	L	L	H	$f_{IN} < 7.7$	$7.7 \le f_{IN}$
14	L	H	L	H	L	$f_{IN} < 7.14$	$7.14 \le f_{IN}$
15	L	H	L	H	H	$f_{IN} < 6.67$	$6.67 \le f_{IN}$
16	L	H	H	L	L	$f_{IN} < 6.25$	$6.25 \le f_{IN}$
17	L	H	H	L	H	$f_{IN} < 5.88$	$5.88 \le f_{IN}$
18	L	H	H	H	L	$f_{IN} < 5.56$	$5.56 \le f_{IN}$
19	L	H	H	H	H	$f_{IN} < 5.26$	$5.26 \le f_{IN}$
20	H	L	L	L	L	$f_{IN} = 5.00$	$5.00 \le f_{IN}$
22	H	L	L	L	H	NA	$5.00 \le f_{IN}$
24	H	L	L	H	L	NA	$5.00 \le f_{IN}$
26	H	L	L	H	H	NA	$5.00 \le f_{IN}$
28	H	L	H	L	L	NA	$5.00 \le f_{IN}$
30	H	L	H	L	H	NA	$5.00 \le f_{IN}$
32	H	L	H	H	L	NA	$5.00 \le f_{IN}$
34	H	L	H	H	H	NA	$5.00 \le f_{IN}$
36	H	H	L	L	L	NA	$5.00 \le f_{IN}$
38	H	H	L	L	H	NA	$5.00 \le f_{IN}$
40	H	H	L	H	L	NA	$5.00 \le f_{IN}$
†	H	H	L	H	H	NA	NA
†	H	H	H	L	L	NA	NA
†	H	H	H	L	H	NA	NA
†	H	H	H	H	L	NA	NA
†	H	H	H	H	H	NA	NA

H = high level, L= low level † = Reserved

equivalent input and output schematic diagrams



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	TYPE	DESCRIPTION
BSEL	11	I	LVTTL	Band select. Used to optimize VCO performance for minimum M-clock jitter: See recommended f_{max} in the frequency multiplier value table.
CRI+, CRI–	2, 3	I	LVDS	Clock reference input. This is the reference clock signal for the PLL frequency multiplier.
EN	17	I	LVTTL	Enable input. Used to disable the device to a low power state. A high level input enables the device, a low level input disables the device.
GND	5, 12, 18, 22, 24	I	NA	Circuit ground
LCRO–, LCRO+	13, 14	O	LVDS	Link clock reference output. This is the data block synchronization clock signal from the PLL frequency multiplier.
LCRO_EN	16	I	LVTTL	LCRO enable. Used to turn off the LCRO outputs when they are not used. A high level input enables the LCRO output; a low level input disables the LCRO output.
LVO	15	O	LVTTL	Lock/valid output. This is signal required for proper MuxIt system operation. It is to be directly connected to the LVI inputs of SN65LVDS151 or SN65LVDS152 devices. It is used to inhibit the operation of those devices until after the PLL has stabilized. It remains at a low level following a reset until the PLL has become phase locked. A low to high-level transition indicates phase lock has occurred.
M1–M5	6–10	I	LVTTL	Multiplier value selection inputs. These inputs determine the frequency multiplication ratio M.
MCO–, MCO+	19,20	O	LVDS	M-clock output. This is the high frequency multiplied clock output from the PLL frequency multiplier. It is used by the companion serializer or deserializer devices to synchronizes the transmission or reception of data
NC	21, 23, 26–28		NA	These pins are not connected and may be left open.
V_{CC}	1, 25		NA	Supply voltage
V_T	4		NA	Voltage reference. A $V_{CC}/2$ reference supplied for the unused CRI input when operated in a single-ended mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 4 V
Voltage range: EN, BSEL, LCRO_EN, or M1–M5 inputs . . . . . –0.5 V to 6 V
CRI input . . . . . –0.5 V to 4 V
LCRO±, MCO± outputs . . . . . –0.5 V to 4 V
Electrostatic discharge: Human body model (CRI±, LCRO±, MCO±,and GND (see Note 2) . . . . . ±12 kV
All pins . . . . . ±2 kV
Charged-device model (all pins) (see Note 3) . . . . . ±500 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.
2. Tested in accordance with JEDEC Standard 22, Test method A114-B.
3. Tested in accordance with JEDEC Standard 22, Test method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
PW	1207 mW	9.6 mW/°C	628 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}	EN, BSEL, LCRO_EN, M1 – M5	2			V
Low-level input voltage, V_{IL}				0.8	V
Magnitude of differential input voltage, $\|V_{ID}\|$	CRI	0.1		0.6	V
Common-mode input voltage, V_{IC}	CRI	$\frac{\|V_{ID}\|}{2}$		$2.4 - \frac{\|V_{ID}\|}{2}$	V
				$V_{CC} - 0.8$	
Operating free-air temperature, T_A		–40		85	°C

timing requirements

	MIN	TYP	MAX	UNIT
Input clock cycle time, $t_{c(1)}$	20		200	ns
High-level input clock pulse width duration, $t_{w(1)}$	0.4 $t_{c(1)}$		0.6 $t_{c(1)}$	
Input clock frequency, CRI, $f_{(clock)}$	5		50	MHz

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage		See Figure 1 and Table 1			100	mV
V_{IT-}	Negative-going differential input threshold voltage			–100			mV
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude		R_L = 100 Ω, See Figure 3	247	340	454	mV
$\Delta\|V_{OD(SS)}\|$	Change in steady-state differential output voltage magnitude between logic states		V_{ID} = ±100 mV, See Figures 2 and 3	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 4	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak change common-mode output voltage				50	150	mV
V_{OH}	High-level output voltage (LVO)		I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage (LVO)		I_{OL} = 8 mA			0.4	V
$V_{(T)}$	Threshold reference bias voltage		–100 µA ≤ I_O ≤ 100 µA	$\frac{V_{CC}}{2} - 0.15$		$\frac{V_{CC}}{2} + 0.15$	V
I_{CC}	Supply current		Enabled, R_L = 100 Ω, CRI± open		25	70	mA
			Disabled		2.5	6	
I_I	Input current (CRI inputs)		V_I = 0	–20		–2	µA
			V_I = 2.4 V	–1.2			
$I_{(ID)}$	Differential input current ($I_{IA} - I_{IB}$) (CRI inputs)		V_{IC} = 0.05 V or 2.35 V, V_{ID} = ±0.1 V	–2		2	µA
$I_{I(OFF)}$	Power-off input current (CRI inputs)		V_{CC} = 0 V, V_I = 3.6 V			20	µA
I_{IH}	High-level input current	M1–M5, EN	V_{IH} = 2 V			20	µA
		BSEL, LCRO_EN		–10			
I_{IL}	Low-level input current	M1–M5, EN	V_{IL} = 0.8 V			10	µA
		BSEL, LCRO_EN		–20			
I_{OS}	Short-circuit output current	MCO, LCRO	V_{O+} or = V_{O-} = 0 V	–10		10	mA
			V_{OD} = 0 V	–10		10	
I_{OZ}	High-impedance output current	MCO, LCRO	V_O = 0 V or V_{CC}	–5		5	µA
$I_{O(OFF)}$	Power-off output current		V_{CC} = 1.5 V , V_O = 3.6 V	–5		5	µA
C_I	Input capacitance (CRI inputs)		V_{ID} =[(0.4sin(4E6πt) = 0.5] V		3		pF

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	MCO output clock period jitter‡	p–p	EN = 1, BSEL = 1, LCRO_EN = 1, M = 40, f_I = 5 MHz		200		ps
		rms			20		
$t_{(lock)}$	Lock (stabilization time)§				0.2	1	ms
$t_{w(2)}$	Multiplied clock output pulse width		R_L = 100 Ω, C_L = 10 pF, See Figure 5	$0.4t_{c(2)}$		$0.6t_{c(2)}$	
t_r	Differential output signal rise time (MCO, LCRO)			0.3	0.6	1.5	ns
t_f	Differential output signal fall time (MCO, LCRO)			0.3	0.6	1.5	
$t_{(OS)}$	CRI↑ to MCO↑ offset time	f_I = 5 MHz, M = 4	R_L = 100 Ω, C_L = 10 pF, See Figure 6	–2.5	0	2.5	ns
		f_I = 10 MHz, M = 10		–1.5	0	1.5	
		f_I = 5 MHz, M = 40		–1.65	0	1.65	
t_d	MCO↑ before LCRO↑ , time delay	f_I = 5 MHz, M = 4	R_L = 100 Ω, C_L = 10 pF, See Figure 6	0.5	2.5	6	ns
		f_I = 10 MHz, M = 10		0.5	2.5	6	
		f_I = 5 MHz, M = 40		0.5	2.5	4.5	
f_{max}	Maximum MCO output frequency		BSEL =1, M = 4, 6	200			MHz
			BSEL =1, M ≠ 4, 6	400			
			BSEL =0, M = 4, 6	50			
			BSEL =0, M ≠ 4, 6	100			

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.
‡ Output clock jitter is the change in the output clock period from one cycle to the next cycle observed over 10,000 cycles with a source having less than 10 psec jitter rms.
§ Lock time is measured from the application of the clock reference input signal to the assertion of a high-level lock/valid output.

PARAMETER MEASUREMENT INFORMATION

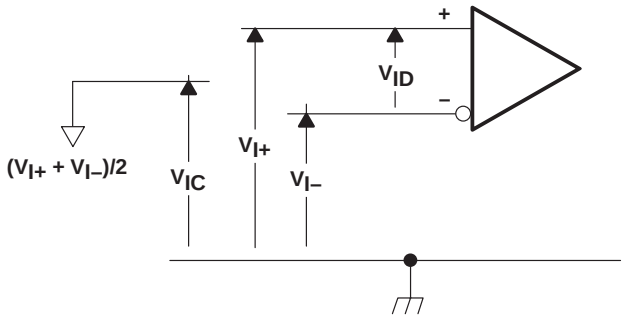


Figure 1. Receiver Input Voltage Definitions

PARAMETER MEASUREMENT INFORMATION

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
$V_{(IA)}$	$V_{(IB)}$	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V

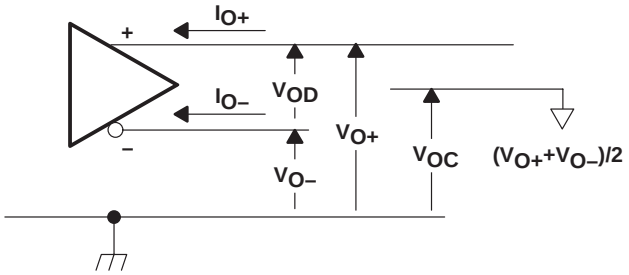


Figure 2. Driver Output Voltage and Current Definitions

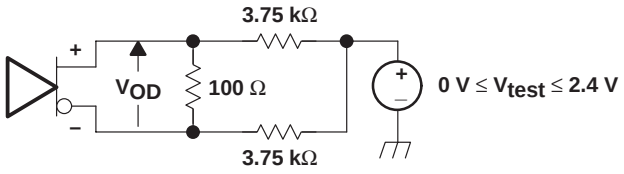
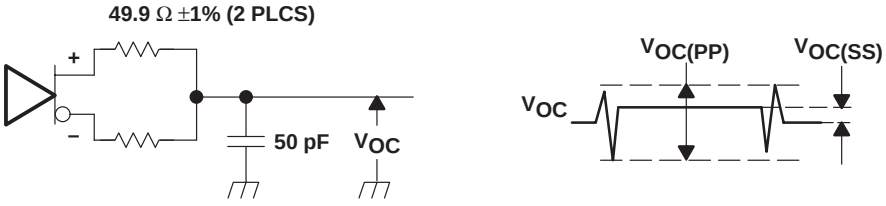


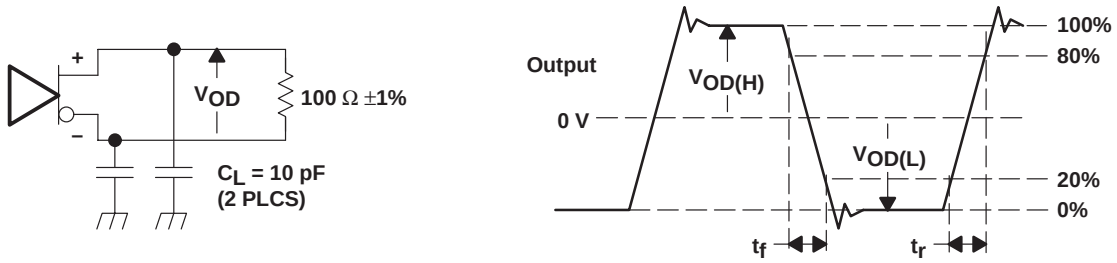
Figure 3. V_{OD} Test Circuit



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, Pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 5 GHz.

Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, Pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 5. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

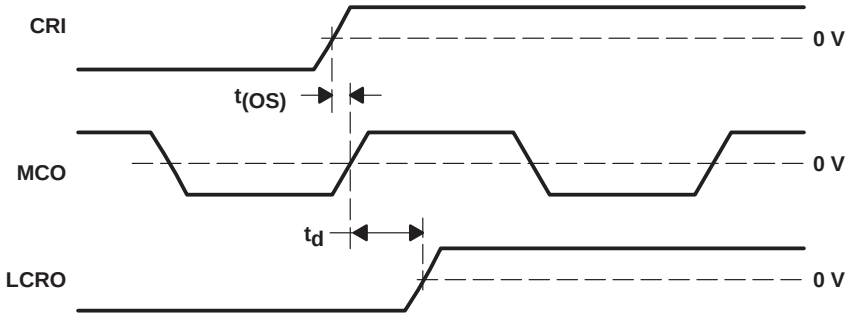


Figure 6. Output Timing Waveform Definitions

TYPICAL CHARACTERISTICS

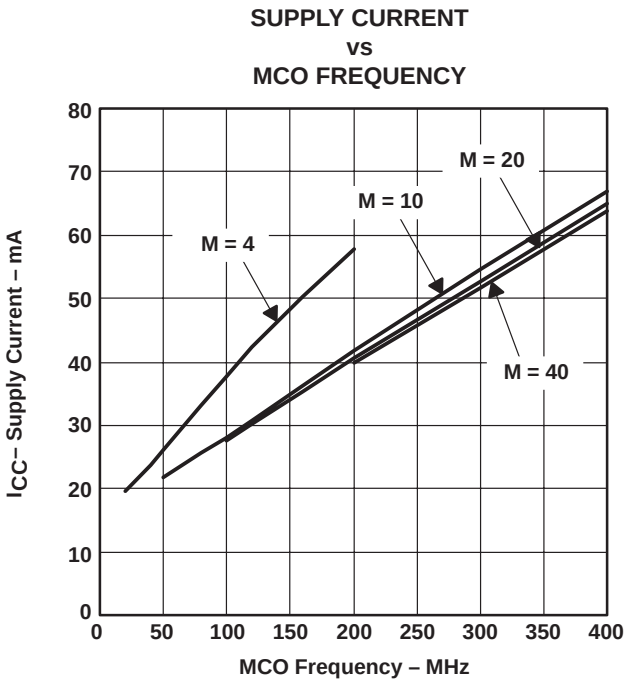


Figure 7

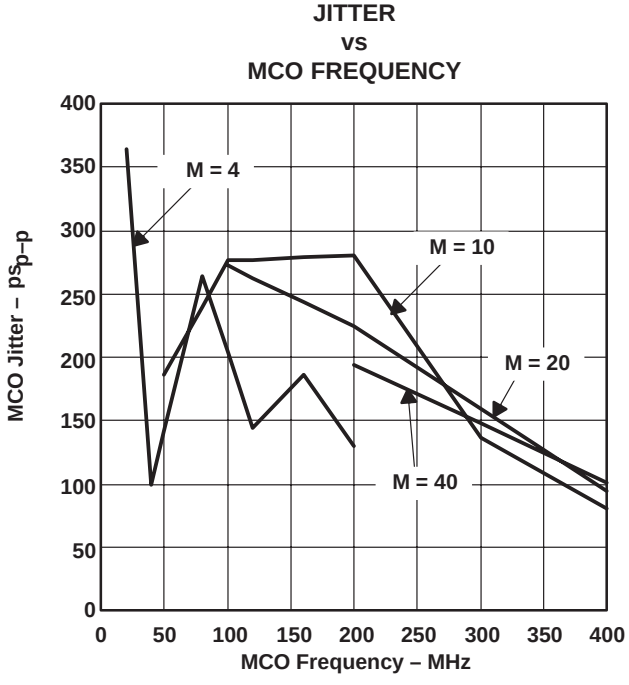


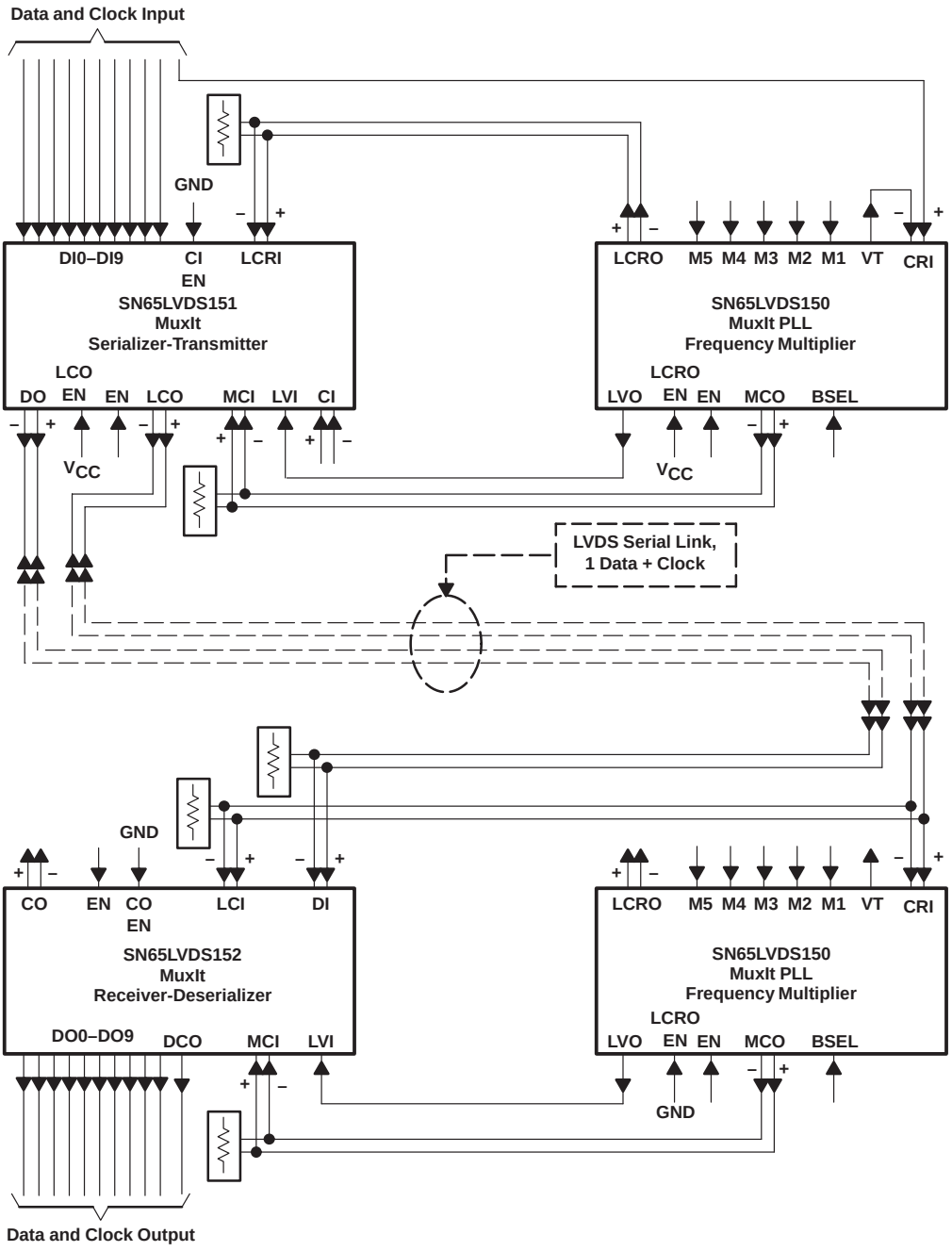
Figure 8

NOTE: M = Multiplying Value (see Page 3)

TYPICAL CHARACTERISTICS

basic applications examples

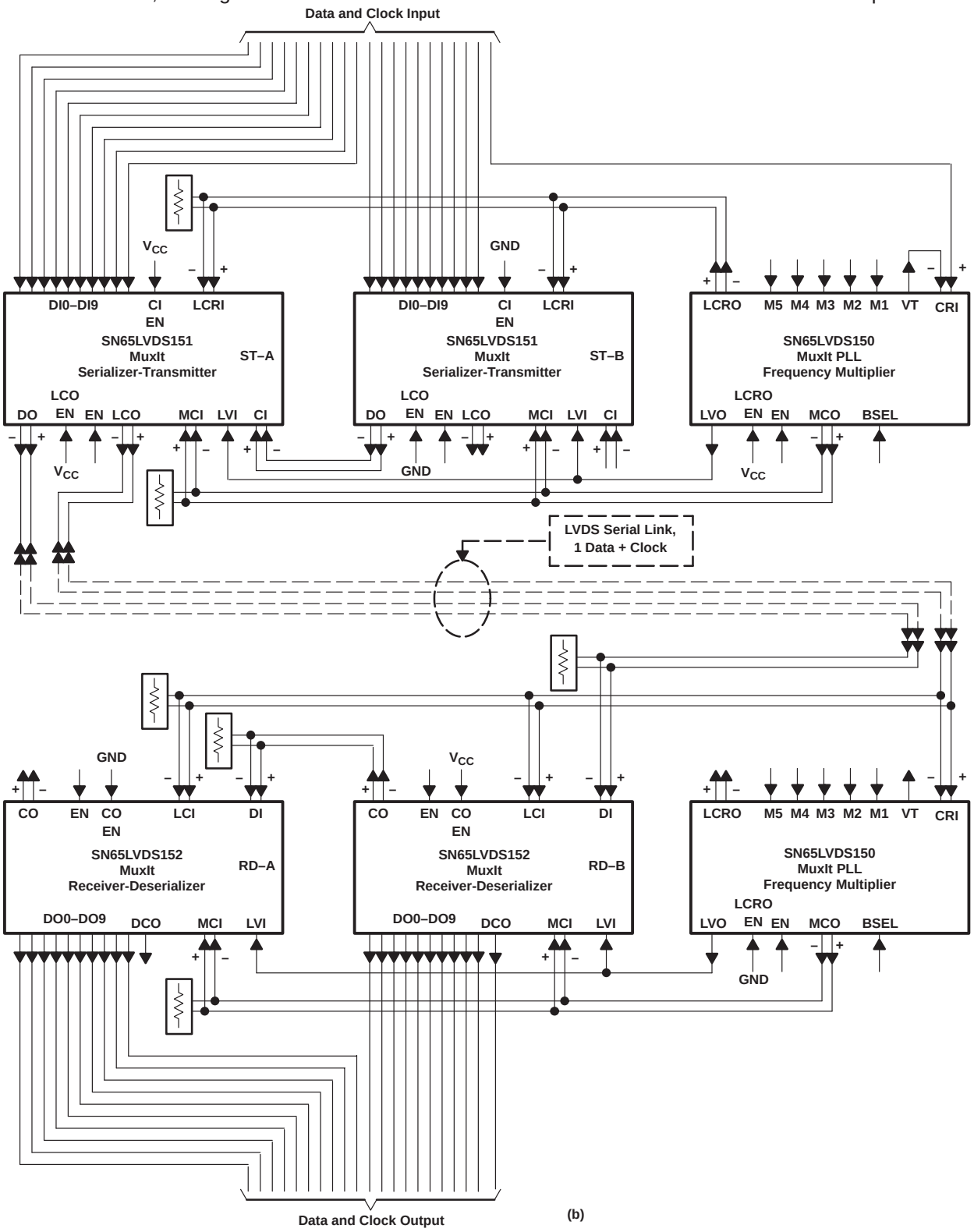
Parallel data path width between 4 and 10 bits, only one LVDS data link required.



(a)

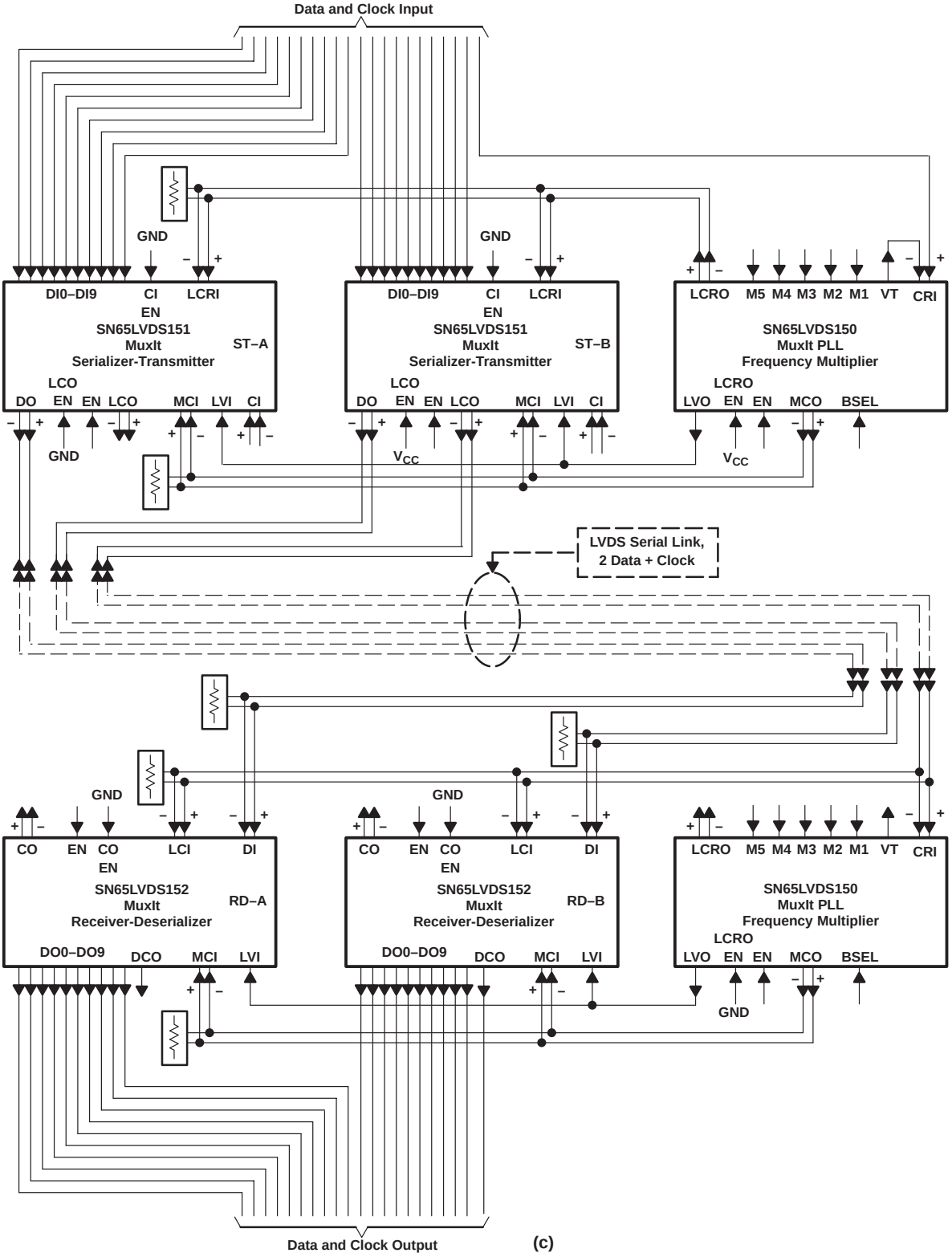
TYPICAL CHARACTERISTICS

Parallel data path width between 11 and 20 bits, aggregate data rate low enough to allow transmission over one LVDS data link, sharing of PLL-FM between serializer-transmitter and receiver-deserializer chips at each end.



TYPICAL CHARACTERISTICS

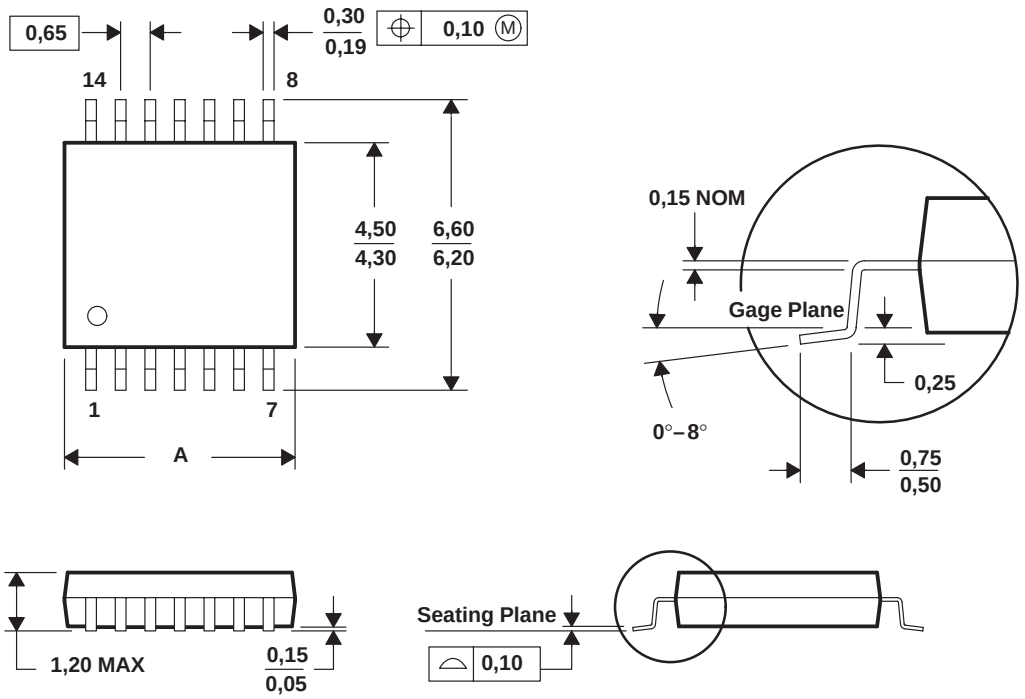
Parallel data path width between 11 and 20 bits, aggregate data rate requires transmission over two separate LVDS data links, sharing of PLL-FM between serializer-transceiver and receiver-deserializer chips at each end.



MECHANICAL INFORMATION

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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