



## 2.5-V/3.3-V OSCILLATOR GAIN STAGE/BUFFERS

### FEATURES

- Low-Voltage PECL Input and Low-Voltage PECL or LVDS Outputs
- Clock Rates to 1 GHz
  - 250-ps Output Transition Times
  - 0.12 ps Typical Intrinsic Phase Jitter
  - Less than 630 ps Propagation Delay Times
- 2.5-V or 3.3-V Supply Operation

- 2-mm x 2-mm Small-Outline No-Lead Package

### APPLICATIONS

- PECL-to-LVDS Translation
- Clock Signal Amplification

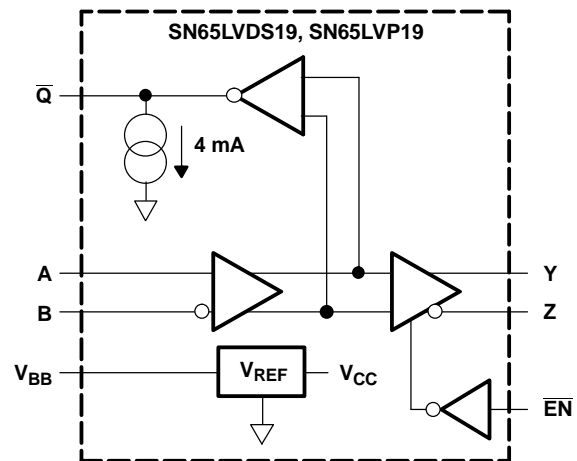
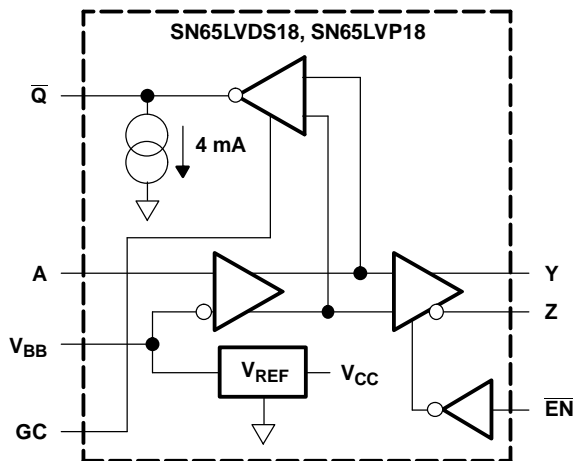
### DESCRIPTION

These four devices are high frequency oscillator gain stages supporting both LVPECL and LVDS on the high gain outputs in 3.3-V or 2.5-V systems. Additionally, provides the option of both single-ended input (PECL levels on the SN65LVx18) and fully differential inputs on the SN65LVx19.

The SN65LVx18 provides the user a Gain Control (GC) for controlling the  $\bar{Q}$  output from 300 mV to 860 mV either by leaving it open (NC), grounded, or tied to  $V_{CC}$ . (When left open, the  $\bar{Q}$  output defaults to 575 mV.) The  $\bar{Q}$  on the SN65LVx19 defaults to 575 mV as well.

Both devices provide a voltage reference ( $V_{BB}$ ) of typically 1.35 V below  $V_{CC}$  for use in receiving single-ended PECL input signals. When not used,  $V_{BB}$  should be unconnected or open.

All devices are characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### AVAILABLE OPTIONS

OUTPUT	PART NUMBER	CARRIER	PART MARKING
LVDS	SN65LVDS18DRFT	Tape and reel	ER
LVDS	SN65LVDS18DRFR	Tape and reel	ER
LVPECL	SN65LVP18DRFT	Tape and reel	EP
LVPECL	SN65LVP18DRFR	Tape and reel	EP
LVDS	SN65LVDS19DRFT	Tape and reel	ET
LVDS	SN65LVDS19DRFR	Tape and reel	ET
LVPECL	SN65LVP19DRFT	Tape and reel	ES
LVPECL	SN65LVP19DRFR	Tape and reel	ES

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	UNIT
$V_{CC}$ Supply voltage <sup>(2)</sup>	–0.5 V to 4 V
$V_I$ Input voltage	–0.5 V to $V_{CC} + 0.5$ V
$V_O$ Output voltage	–0.5 V to $V_{CC} + 0.5$ V
$I_O$ $V_{BB}$ output current	±0.5 mA
HBM electrostatic discharge <sup>(3)</sup>	±3 kV
CDM electrostatic discharge <sup>(4)</sup>	±1500 V
Continuous power dissipation	See Power Dissipation Ratings Table

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground (see Figure 1).
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A-7
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101

### DISSIPATION RATINGS

PACKAGE	$T_A < 25^\circ\text{C}$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
DRF	403 mW	4.0 mW/°C	161 mW

### RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply Voltage	2.375		3.6	V
$V_{IH}$ High-level input voltage to $\overline{EN}$	2		$V_{CC}$	V
$V_{IAH}$ or $V_{IBH}$ High-level input voltage to A or B	1.2		$V_{CC}$	V
$V_{IL}$ Low-level input voltage to $\overline{EN}$	0		0.8	V
$V_{IAL}$ or $V_{IBL}$ Low-level input voltage to A or B	0		$V_{CC} - 0.08$	V
$I_{BB}$ $V_{BB}$ output current	–400 <sup>(1)</sup>		400	μA
$R_L$ Differential load resistance, SN65LVDS18/19	90		132	Ω
$T_A$ Operating free-air temperature	–40		85	°C

- (1) The algebraic convention, where the least positive (more negative) value is designated minimum, is used in this data sheet.

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
I <sub>CC</sub>	Supply current, SN65LVDS18/19	R <sub>L</sub> = 100 Ω, $\overline{EN}$ at 0 V, Other inputs open		30	36	mA
	Supply current, SN65LVP18/19	Outputs unloaded, $\overline{EN}$ at 0 V, Other inputs open		17	22	
V <sub>BB</sub>	Reference voltage <sup>(2)</sup>	I <sub>BB</sub> = -400 μA	V <sub>CC</sub> - 1.44	V <sub>CC</sub> - 1.35	V <sub>CC</sub> - 1.25	V
I <sub>IH</sub>	High-level input current, $\overline{EN}$	V <sub>I</sub> = 2 V	-20		20	μA
I <sub>IAH</sub> or I <sub>IBH</sub>	High-level input current, A or B	V <sub>I</sub> = V <sub>CC</sub>	-20		20	
I <sub>IL</sub>	Low-level input current, $\overline{EN}$	V <sub>I</sub> = 0.8 V	-20		20	
I <sub>IAL</sub> or I <sub>IBL</sub>	Low-level input current, A or B	V <sub>I</sub> = GND	-20		20	
<b>SN65LVDS18/19 Y AND Z OUTPUT CHARACTERISTICS</b>						
V <sub>OD</sub>	Differential output voltage magnitude,  V <sub>OY</sub> - V <sub>OZ</sub>	See Figure 1 and Figure 2	247	340	454	mV
Δ V <sub>OD</sub>	Change in differential output voltage magnitude between logic states		50			
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage (see Figure 3)		1.125		1.375	V
ΔV <sub>OC(SS)</sub>	Change in steady-state common-mode output voltage between logic states	See Figure 3	-50		50	mV
V <sub>OC(PP)</sub>	Peak-to-peak common-mode output voltage		50		100	
I <sub>OYZ</sub> or I <sub>OZZ</sub>	High-impedance output current	$\overline{EN}$ at V <sub>CC</sub> , V <sub>O</sub> = 0 V or V <sub>CC</sub>	-1		1	μA
I <sub>OYS</sub> or I <sub>OZS</sub>	Short-circuit output current	$\overline{EN}$ at 0 V, V <sub>OY</sub> or V <sub>OZ</sub> = 0 V	-50		50	mA
I <sub>OS(D)</sub>	Differential short-circuit output current,  I <sub>OY</sub> - I <sub>OZ</sub>	$\overline{EN}$ at 0 V, V <sub>OY</sub> = V <sub>OZ</sub>	-12		12	
<b>SN65LVP18/19 Y AND Z OUTPUT CHARACTERISTICS</b>						
V <sub>OYH</sub> or V <sub>OZH</sub>	High-level output voltage	3.3 V; 50 Ω from Y and Z to V <sub>CC</sub> - 2 V	V <sub>CC</sub> - 1.13		V <sub>CC</sub> - 0.85	V
V <sub>OYL</sub> or V <sub>OZL</sub>	Low-level output voltage		V <sub>CC</sub> - 1.87		V <sub>CC</sub> - 1.61	
V <sub>OYL</sub> or V <sub>OZL</sub>	Low-level output voltage		V <sub>CC</sub> - 1.92		V <sub>CC</sub> - 1.61	
V <sub>OD</sub>	Differential output voltage magnitude,  V <sub>OH</sub> - V <sub>OL</sub>		0.6	0.8	1	
I <sub>OYZ</sub> or I <sub>OZZ</sub>	High-impedance output current	$\overline{EN}$ at V <sub>CC</sub> , V <sub>O</sub> = 0 V or V <sub>CC</sub>	-1		1	μA
<b><math>\overline{Q}</math> OUTPUT CHARACTERISTICS (see Figure 1)</b>						
V <sub>OH</sub>	High-level output voltage	$\overline{Q}$ Output open		V <sub>CC</sub> - 0.94		V
V <sub>OL</sub>	Low-level output voltage	GC Tied to GND, $\overline{Q}$ Output open		V <sub>CC</sub> - 1.22		V
		GC Open, $\overline{Q}$ Output open		V <sub>CC</sub> - 1.52		
		GC Tied to V <sub>CC</sub> , $\overline{Q}$ Output open		V <sub>CC</sub> - 1.82		
V <sub>OD</sub>	Differential output voltage magnitude,  V <sub>OH</sub> - V <sub>OL</sub>	GC Tied to GND		300		mV
		GC Open		575		
		CGT Tied to V <sub>CC</sub>		860		

(1) Typical values are at roomtemperature and with a V<sub>CC</sub> of 3.3V.

(2) Single-ended input operation is limited to V<sub>CC</sub> ≥ 3.0 V.

## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PD}$	Propagation delay time, $t_{PLH}/t_{PHL}$	A to $\bar{Q}$	See Figure 4	340	460	ps
		D to Y and Z		460	630	
$t_{SK(P)}$	Pulse skew, $ t_{PLH} - t_{PHL} $				20	
$t_{SK(PP)}$	Part-to-part skew <sup>(2)</sup>	$V_{CC} = 3.3\text{ V}$			80	ps
		$V_{CC} = 2.5\text{ V}$			130	
$t_r$	20%-to-80% differential signal rise time	LVDS, See Figure 4		140	250	ps
		LVPECL, See Figure 4		190	300	
$t_f$	20%-to-80% differential signal fall time	LVDS, See Figure 4		140	250	ps
		LVPECL, See Figure 4		210	300	
$t_{jit(per)}$	RMS period jitter <sup>(3)</sup>	2-GHz 50%-duty-cycle square-wave input, See Figure 5		2	4	ps
$t_{jit(cc)}$	Peak cycle-to-cycle jitter <sup>(4)</sup>			17	24	
$t_{jit(ph)}$	Intrinsic phase jitter	1 GHz		0.12		ps
$t_{PHZ}$	Propagation delay time, high-level-to-high-impedance output	See Figure 6			30	ns
$t_{PLZ}$	Propagation delay time, low-level-to-high-impedance output				30	
$t_{PZH}$	Propagation delay time, high-impedance-to-high-level output				30	
$t_{PZL}$	Propagation delay time, high-impedance-to-low-level output				30	

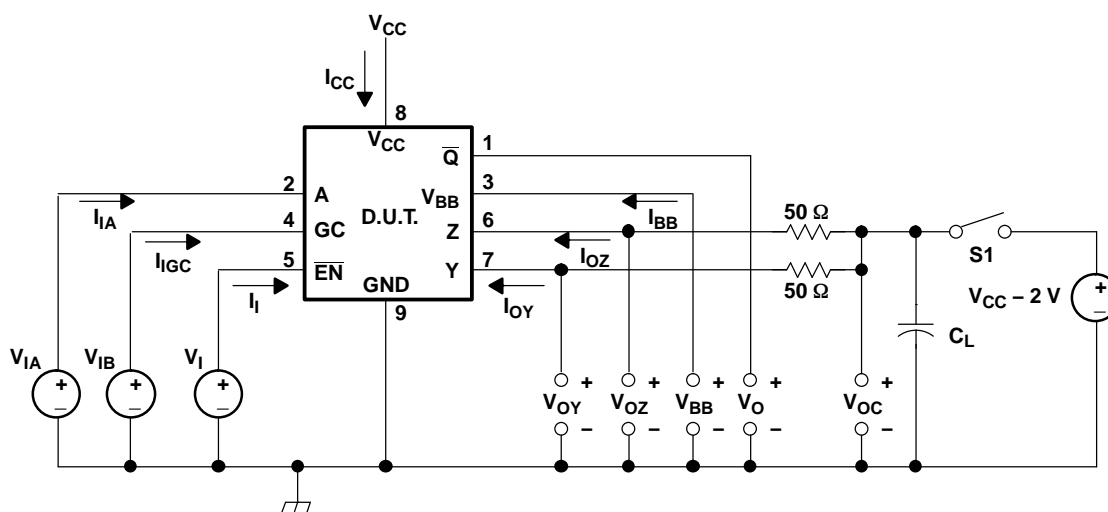
(1) Typical values are at roomtemperature and with a  $V_{CC}$  of 3.3V.

(2) Part-to-part skew is themagnitude of the difference in propagation delay times between any specifiedterminals of two devices when both devices operate with the same supplyvoltages, at the same temperature, and have identical packages and testcircuits.

(3) Period jitter is thedeviation in cycle time of a signal with respect to the ideal period over arandom sample of 100,000 cycles.

(4) Cycle-to-cycle jitter is thevariation in cycle time of a signal between adjacent cycles, over a randomsample of 1,000 adjacent cycle pairs.

## PARAMETER MEASUREMENT INFORMATION

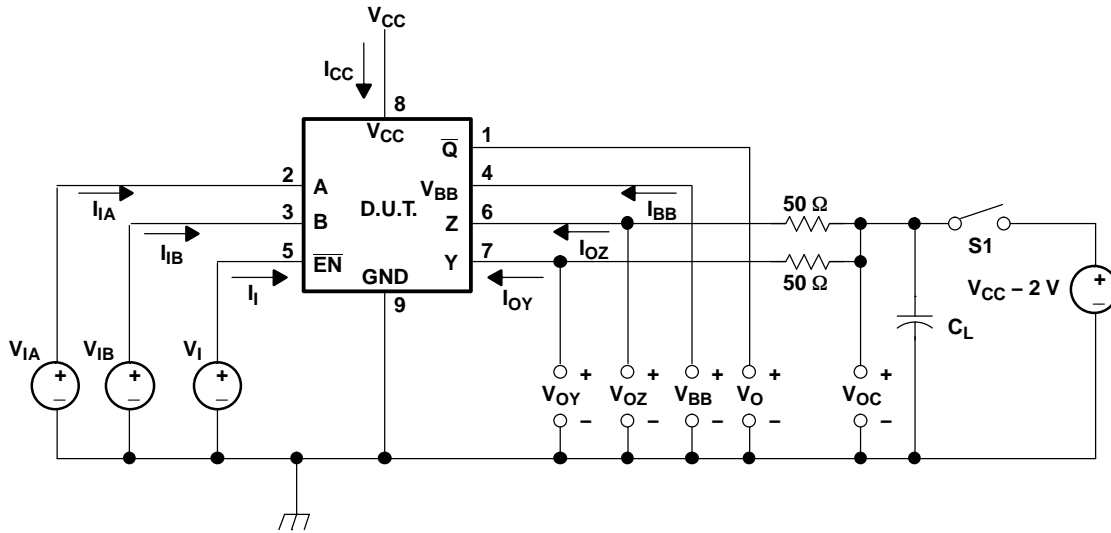


(1)  $C_L$  is the instrumentation and test fixture capacitance.

(2) S1 is open for the SN65LVDS18 and closed for the SN65LVP18.

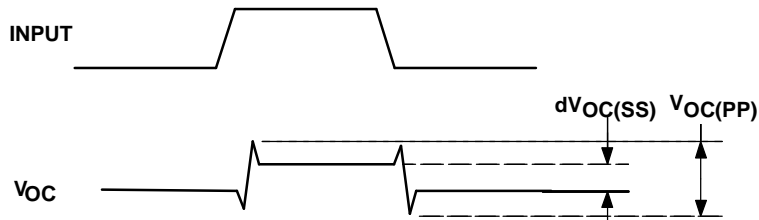
**Figure 1. Output Voltage Test Circuit and Voltage and Current Definitions for LVDS/LVP18**

**PARAMETER MEASUREMENT INFORMATION (continued)**

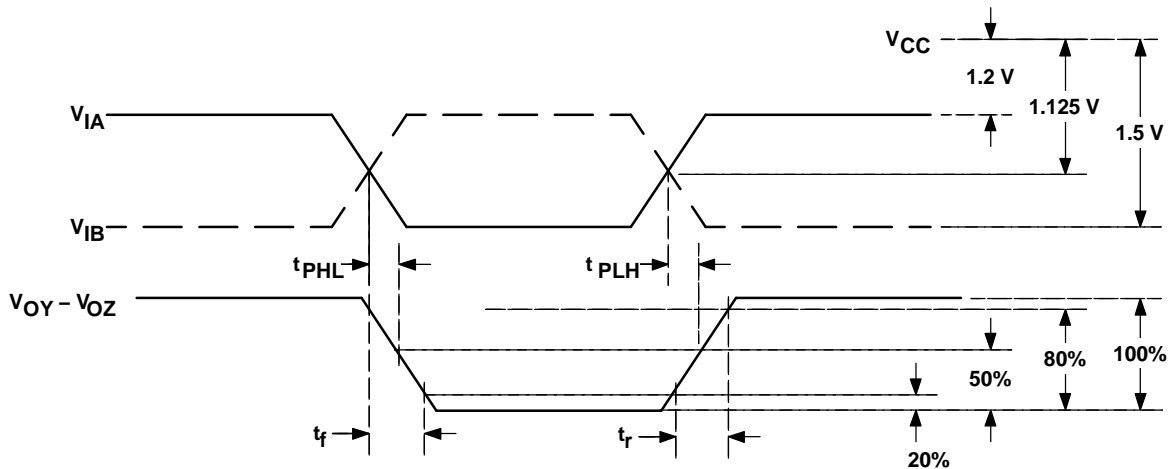


- (1)  $C_L$  is the instrumentation and test fixture capacitance.
- (2) S1 is open for the SN65LVDS19 and closed for the SN65LVP19.

**Figure 2. Output Voltage Test Circuit and Voltage and Current Definitions for LVDS/LVP19**



**Figure 3.  $V_{OC}$  Definitions**



**Figure 4. Propagation Delay and Transition Time Test Waveforms**

PARAMETER MEASUREMENT INFORMATION (continued)

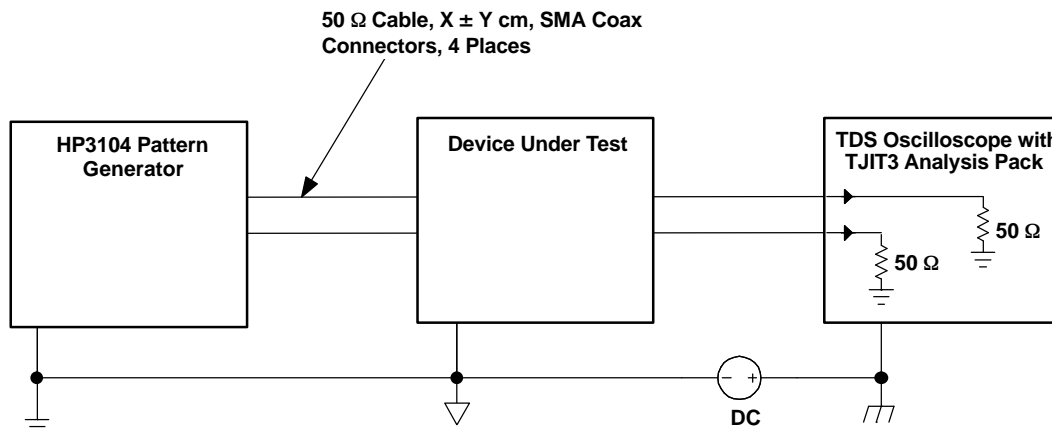


Figure 5. Jitter Measurement Setup

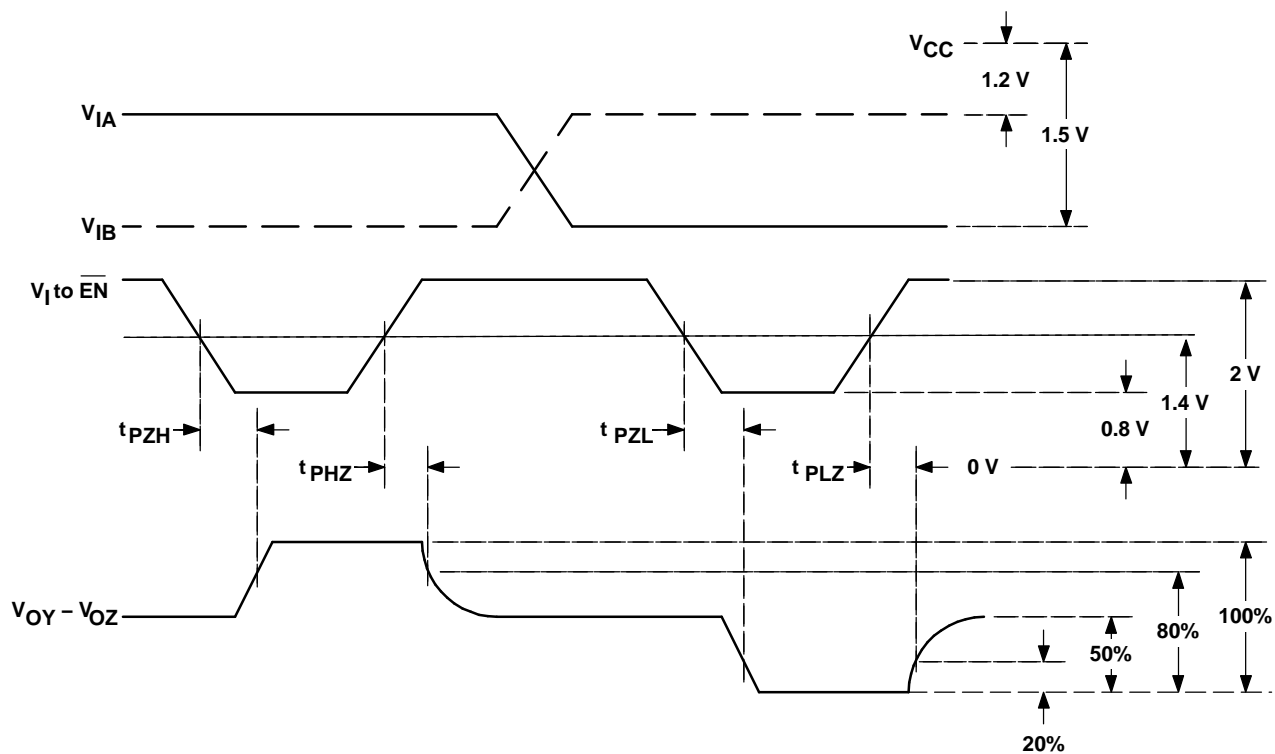


Figure 6. Enable and Disable Time Test Waveforms

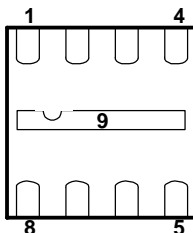
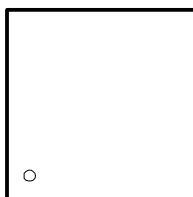
**DEVICE INFORMATION**

**FUNCTION TABLE <sup>(1)</sup>**

SN65LVDS18, SN65LVP18					SN65LVDS19, SN65LVP19					
A	$\overline{EN}$	$\overline{Q}$	Y	Z	A	B	$\overline{EN}$	$\overline{Q}$	Y	Z
H	L	L	H	L	H	H	L	?	?	?
L	L	H	L	H	L	H	L	H	L	H
X	H	?	Z	Z	H	L	L	L	H	L
Open	L	?	?	?	L	L	L	?	?	?
X	Open	?	?	?	X	X	H	?	Z	Z
					Open	Open	L	?	?	?
					X	X	Open	?	?	?

(1) H = high, L = low, Z = high impedance, ? = indeterminate

**DRF PACKAGE  
TOP VIEW**



**BOTTOM VIEW**

**Package Pin Assignments – Numerical Listing**

SN65LVDS18, SN65LVP18		SN65LVDS19, SN65LVP19	
PIN	SIGNAL	PIN	SIGNAL
1	$\overline{Q}$	1	$\overline{Q}$
2	A	2	A
3	$V_{BB}$	3	B
4	GC	4	$V_{BB}$
5	$\overline{EN}$	5	$\overline{EN}$
6	Z	6	Z
7	Y	7	Y
8	$V_{CC}$	8	$V_{CC}$
9	GND	9	GND

TYPICAL CHARACTERISTICS

SUPPLY CURRENT  
VS  
FREQUENCY

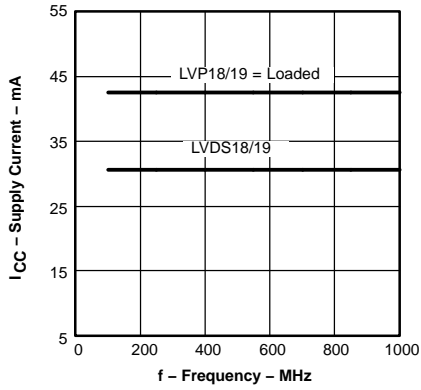


Figure 7.

SUPPLY CURRENT  
VS  
FREE-AIR TEMPERATURE

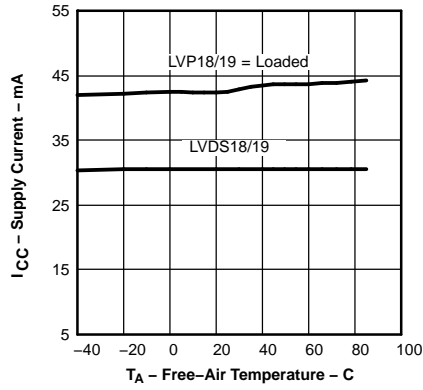


Figure 8.

LVDS18/19 RISE/FALL TIME  
VS  
FREE-AIR TEMPERATURE

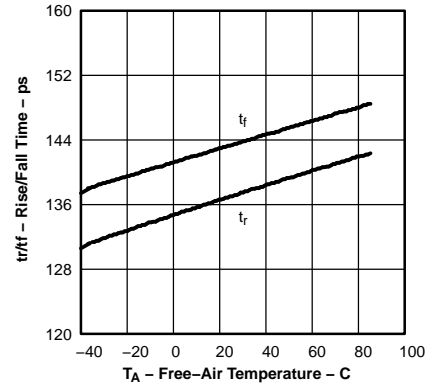


Figure 9.

LVP18/19 RISE/FALL TIME  
VS  
FREE-AIR TEMPERATURE

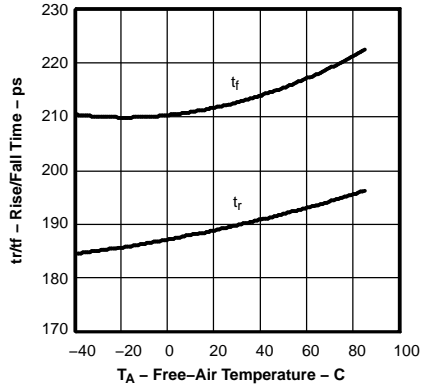


Figure 10.

LVDS18/19 PROPAGATION DELAY  
VS  
FREE-AIR TEMPERATURE

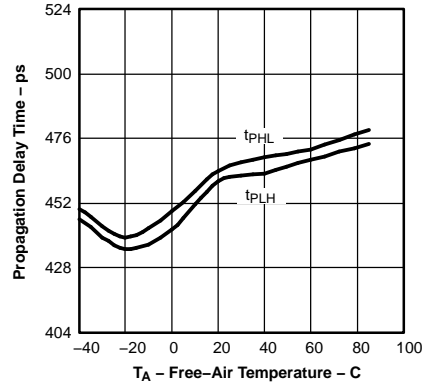


Figure 11.

PERIOD JITTER  
VS  
FREQUENCY

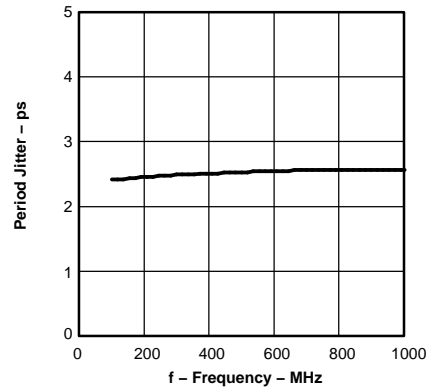


Figure 12.

CYCLE-TO-CYCLE JITTER  
VS  
FREQUENCY

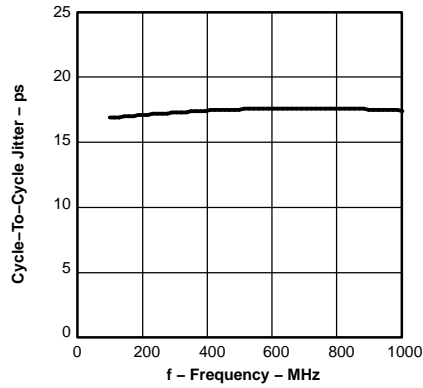
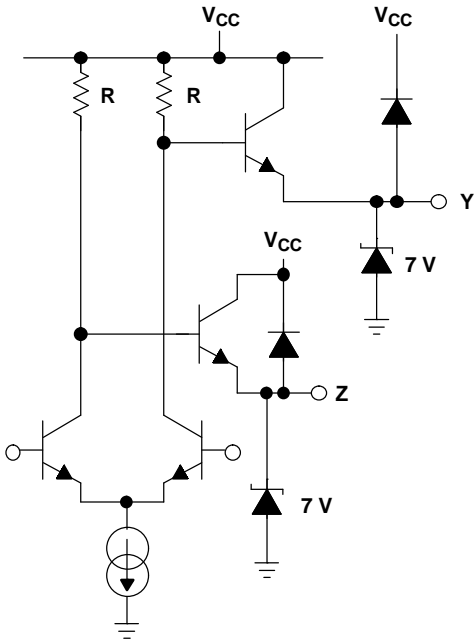


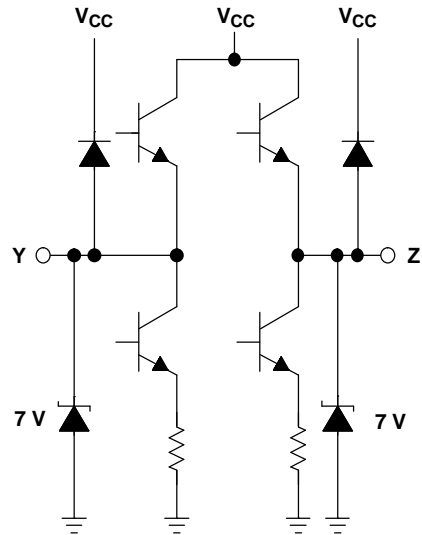
Figure 13.

**EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS**

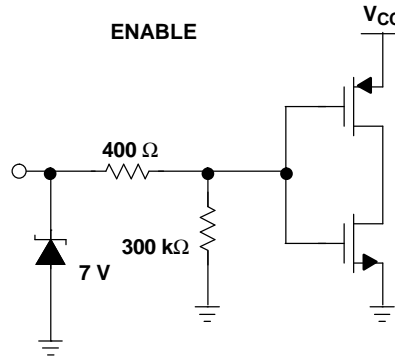
**OUTPUT LVP18/19**



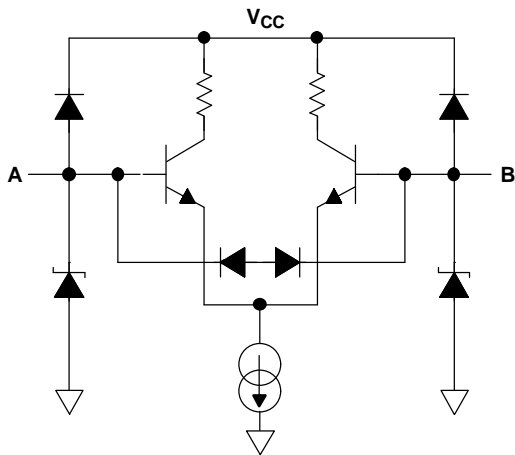
**OUTPUT LVDS18/19**



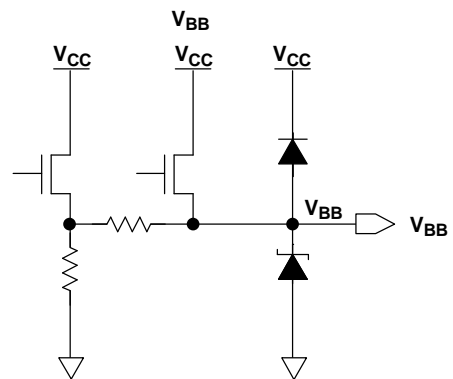
**ENABLE**



**INPUT**



**OUTPUT**



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN65LVDS18DRFR	ACTIVE	SON	DRF	8	3000	None	CU NIPD	Level-1-220C-UNLIM
SN65LVDS18DRFT	ACTIVE	SON	DRF	8	250	None	CU NIPD	Level-1-220C-UNLIM
SN65LVDS19DRFR	ACTIVE	SON	DRF	8	3000	None	CU NIPD	Level-1-220C-UNLIM
SN65LVDS19DRFT	ACTIVE	SON	DRF	8	250	None	CU NIPD	Level-1-220C-UNLIM
SN65LVP18DRFR	ACTIVE	SON	DRF	8	3000	None	CU NIPD	Level-1-220C-UNLIM
SN65LVP18DRFT	ACTIVE	SON	DRF	8	250	None	CU NIPD	Level-1-220C-UNLIM
SN65LVP19DRFR	ACTIVE	SON	DRF	8	3000	None	CU NIPD	Level-1-220C-UNLIM
SN65LVP19DRFT	ACTIVE	SON	DRF	8	250	None	CU NIPD	Level-1-220C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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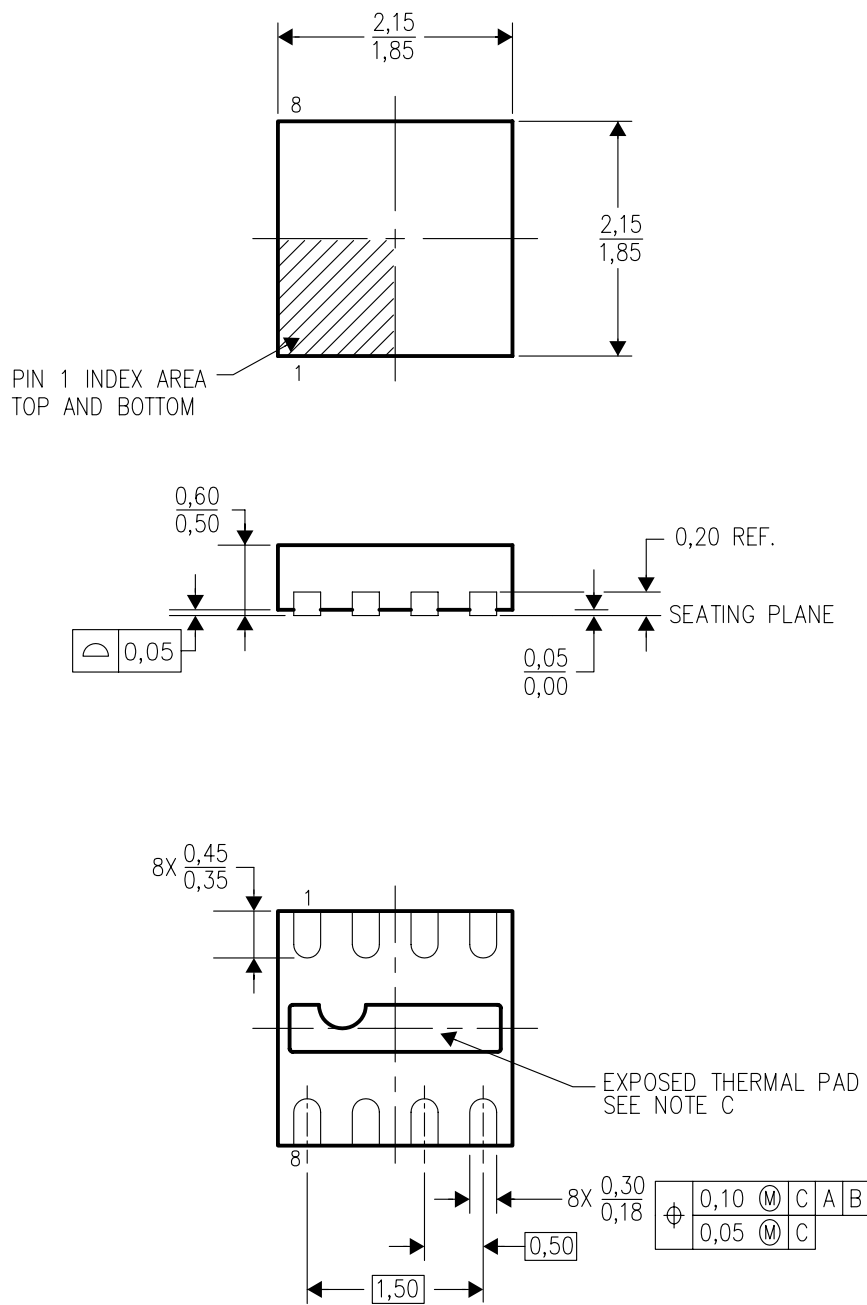
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DRF (S-PDSO-N8)

PLASTIC SMALL OUTLINE



4205287/C 06/04

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
  - D. Falls within JEDEC MO-229.

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