LVPECL AND LVDS REPEATER/TRANSLATOR WITH ENABLE

FEATURES

- **Low-Voltage PECL Input and Low-Voltage PECL or LVDS Outputs**
- **Signaling Rates to 4 Gbps or Clock Rates to 2 GHz**
  - **120-ps Output Transition Times**
  - **Less than 45 ps Total Jitter**
  - **Less than 630 ps Propagation Delay Times**
- **2.5-V or 3.3-V Supply Operation**
- **2-mm x 2-mm Small-Outline No-Lead Package**

APPLICATIONS

- **PECL-to-LVDS Translation**
- **Data or Clock Signal Amplification**

DESCRIPTION

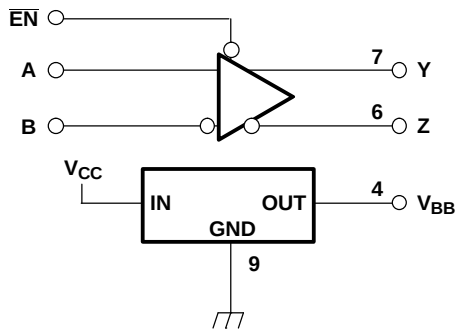
The SN65LVDS20 and SN65LVP20 are a high-speed differential receiver and driver connected as a repeater. The receiver accepts low-voltage positive-emitter-coupled logic (PECL) at signaling rates up to 4 Gbps and repeats it as either an LVDS or PECL output signal. The signal path through the device is differential for low radiated emissions and minimal added jitter.

The outputs of the SN65LVDS20 are LVDS levels as defined by TIA/EIA-644-A. The outputs of the SN65LVDP20 are compatible with low-voltage PECL levels. A low-level input to $\overline{EN}$ enables the outputs. A high-level input puts the output into a high-impedance state. Both outputs are designed to drive differential transmission lines with nominally 100-Ω characteristic impedance.

Both devices provide a voltage reference (V_{BB}) of typically 1.35 V below V_{CC} for use in receiving single-ended PECL input signals. When not used, V_{BB} should be unconnected or open.

All devices are characterized for operation from -40°C to 85°C.

FUNCTION DIAGRAM



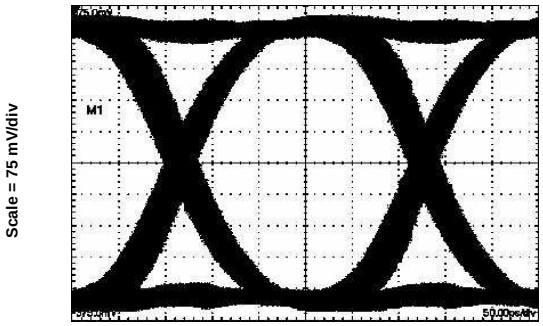


Figure 1. SN65LVDS20 Output Eye Pattern With 4-Gbps PRBS Input

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

OUTPUT	PART NUMBER	CARRIER	PART MARKING
LVDS	SN65LVDS20DRFT	Tape and reel : 250 pcs	E8
LVDS	SN65LVDS20DRFR	Tape and reel : 3000 pcs	E8
PECL	SN65LVP20DRFT	Tape and reel : 250 pcs	E7
PECL	SN65LVP20DRFR	Tape and reel : 3000 pcs	E7

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNIT
V_{CC}	Supply voltage (2)	-0.5 V to 4 V
V_I	Input voltage	-0.5 V to V_{CC} + 0.5 V
V_O	Output voltage	-0.5 V to V_{CC} + 0.5 V
I_O	V_{BB} output current	±0.5 mA
	HBM electrostatic discharge (3)	±3 kV
	CDM electrostatic discharge (4)	±1500 V
	Continuous power dissipation	See Power Dissipation Ratings Table

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground (see Figure 2).
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A-7
(4) Tested in accordance with JEDEC Standard 22, Test Method C101

DISSIPATION RATINGS

PACKAGE	T_A < 25°C POWER RATING	OPERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
DRF	403 mW	4.0 mW/°C	161 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	2.375		3.6	V
V_{IH}	High-level input voltage to $\overline{EN}$	2		V_{CC}	V
V_{IAH} or V_{IBH}	High-level input voltage to A or B	1.2		V_{CC}	V
V_{IL}	Low-level input voltage to $\overline{EN}$	0		0.8	V
V_{IAL} or V_{IBL}	Low-level input voltage to A or B	0		V_{CC} - 0.08	V
I_{BB}	V_{BB} output current	-400 (1)		400	µA
R_L	Differential load resistance, SN65LVDS20	90		132	Ω
$1/T_{UI}$	Signaling rate			4	Gbps
T_A	Operating free-air temperature	-40		85	°C

(1) The algebraic convention, where the least positive (more negative) value is designated minimum, is used in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current, SN65LVDS20	R_L = 100 Ω, $\overline{EN}$ at 0 V, Other inputs open		35	45	mA
	Supply current, SN65LVP20	Outputs unloaded, $\overline{EN}$ at 0 V, Other inputs open		19	24	
P_D	Device power dissipation, SN65LVDS20	R_L = 100 Ω, $\overline{EN}$ at 0 V, 2-GHz 50%-duty-cycle square-wave input		116	160	mW
	Device power dissipation, SN65LVP20	50 Ω from Y and Z to V_{CC} - 2 V, $\overline{EN}$ at 0 V, 2-GHz 50%-duty-cycle square-wave input		63	86	
V_{BB}	Reference voltage	I_{BB} = ±400 µA	V_{CC} - 1.44	V_{CC} - 1.35	V_{CC} - 1.25	V
I_{IH}	High-level input current, $\overline{EN}$	V_I = 2 V	-20		20	µA
I_{IAH} or I_{IBH}	High-level input current, A or B	V_I = V_{CC}	-20		20	
I_{IL}	Low-level input current, $\overline{EN}$	V_I = 0.8 V	-20		20	
I_{IAL} or I_{IBL}	Low-level input current, A or B	V_I = GND	-20		20	
SN65LVDS20 OUTPUT CHARACTERISTICS (see Figure 2)						
$\|V_{OD}\|$	Differential output voltage magnitude, $\|V_{OY} - V_{OZ}\|$	See Figure 2	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states				50	
$V_{OC(SS)}$	Steady-state common-mode output voltage (see Figure 3)		1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 3	-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	100	
I_{OYZ} or I_{OZZ}	High-impedance output current	$\overline{EN}$ at V_{CC}, V_O = 0 V or V_{CC}	-1		1	µA
I_{OYS} or I_{OZS}	Short-circuit output current	$\overline{EN}$ at 0 V, V_{OY} or V_{OZ} = 0 V	-62		62	mA
$I_{OS(D)}$	Differential short-circuit output current, $\|I_{OY} - I_{OZ}\|$	$\overline{EN}$ at 0 V, V_{OY} = V_{OZ}	-12		12	
SN65LVP20 OUTPUT CHARACTERISTICS (see Figure 2)						
V_{OYH} or V_{OZH}	High-level output voltage	3.3 V; 50 Ω from Y and Z to V_{CC} - 2 V	V_{CC} - 1.05		V_{CC} - 0.82	V
V_{OYL} or V_{OZL}	Low-level output voltage		V_{CC} - 1.83		V_{CC} - 1.57	
V_{OYL} or V_{OZL}	Low-level output voltage	2.5 V; 50 Ω from Y and Z to V_{CC} - 2 V	V_{CC} - 1.88		V_{CC} - 1.57	
$\|V_{OD}\|$	Differential output voltage magnitude, $\|V_{OH} - V_{OL}\|$		0.6	0.8	1	
I_{OYZ} or I_{OZZ}	High-impedance output current	$\overline{EN}$ at V_{CC}, V_O = 0 V or V_{CC}	-1		1	µA

(1) Typical values are at room temperature and with a V_{CC} of 3.3 V.

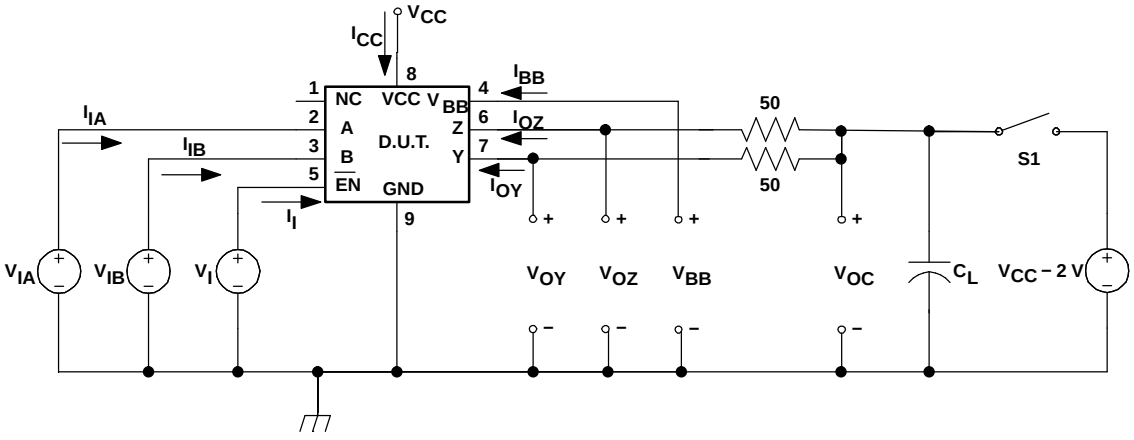
SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Differential propagation delay time, low-to-high-level output	See Figure 2 and Figure 4	300	450	630	ps
t_{PHL}	Differential propagation delay time, high-level-to-low-level output		300	450	630	
$t_{SK(P)}$	Pulse skew, $\lvert t_{PLH} - t_{PHL} \rvert$				20	
$t_{SK(PP)}$	Part-to-part skew (2)	V_{CC} = 3.3 V			80	ps
		V_{CC} = 2.5 V			130	
t_r	20%-to-80% differential signal rise time	LVDS, See Figure 2 and Figure 4		85	115	ps
		LVPECL, See Figure 2 and Figure 4		92	120	
t_f	20%-to-80% differential signal fall time	LVDS, See Figure 2 and Figure 4		85	115	ps
		LVPECL, See Figure 2 and Figure 4		92	120	
$t_{jit(per)}$	RMS period jitter(3)	2-GHz 50%-duty-cycle square-wave input, See Figure 5		2	3	ps
$t_{jit(cc)}$	Peak cycle-to-cycle jitter (4)			13	16	
$t_{jit(p-p)}$	Peak-to-peak jitter	LVDS; 4 Gbps PRBS, 2^{23}- 1 run length, See Figure 5		37	45	ps
$t_{jit(ph)}$	Intrinsic phase jitter	155.52 MHz		0.62		ps
		622.08 MHz		0.14		
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 2 and Figure 6			30	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				30	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output				30	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output				30	

(1) Typical values are at room temperature and with a V_{CC} of 3.3 V.
(2) Part-to-part skew is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 100,000 cycles.
(4) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles, over a random sample of 1,000 adjacent cycle pairs.

PARAMETER MEASUREMENT INFORMATION



1. C_L is the instrumentation and test fixture capacitance.
2. S1 is open for the SN65LVDS20 and closed for the SN65LVP20.

Figure 2. Output Voltage Test Circuit and Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

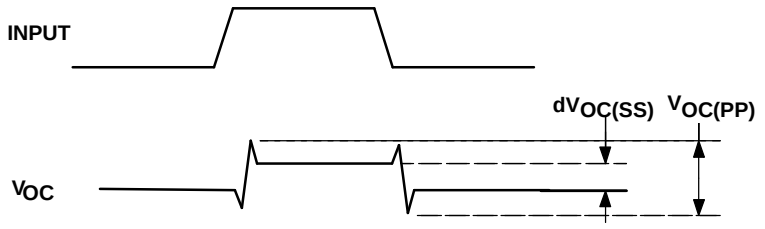


Figure 3. V_{OC} Definitions

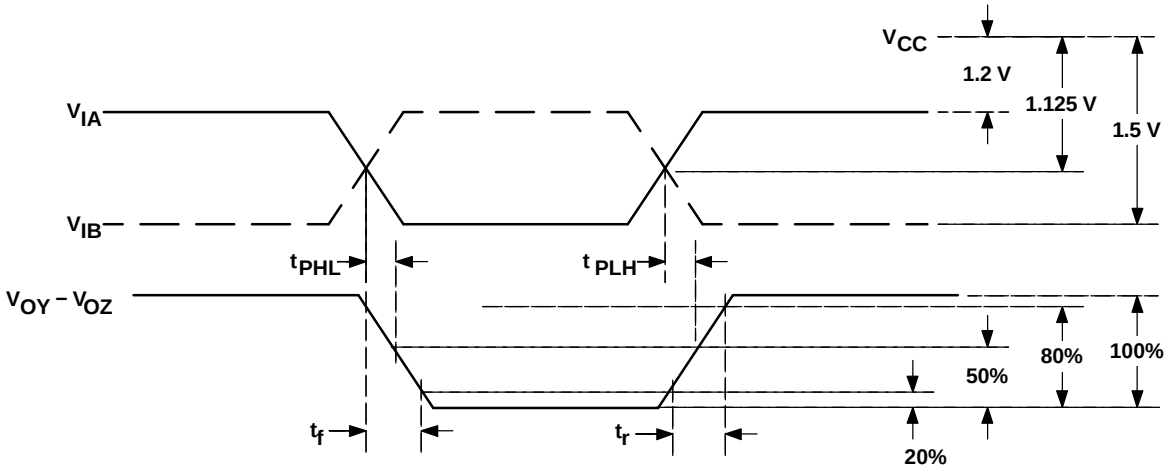


Figure 4. Propagation Delay and Transition Time Test Waveforms

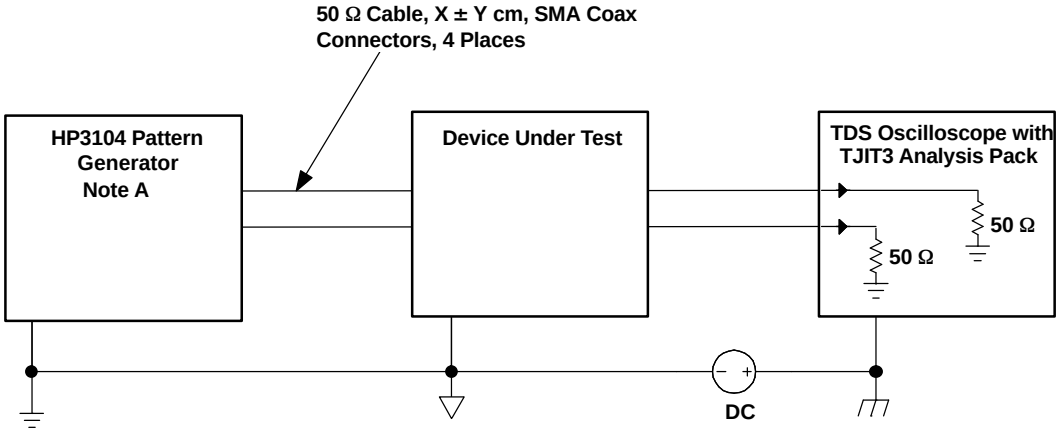


Figure 5. Jitter Measurement Setup

PARAMETER MEASUREMENT INFORMATION (continued)

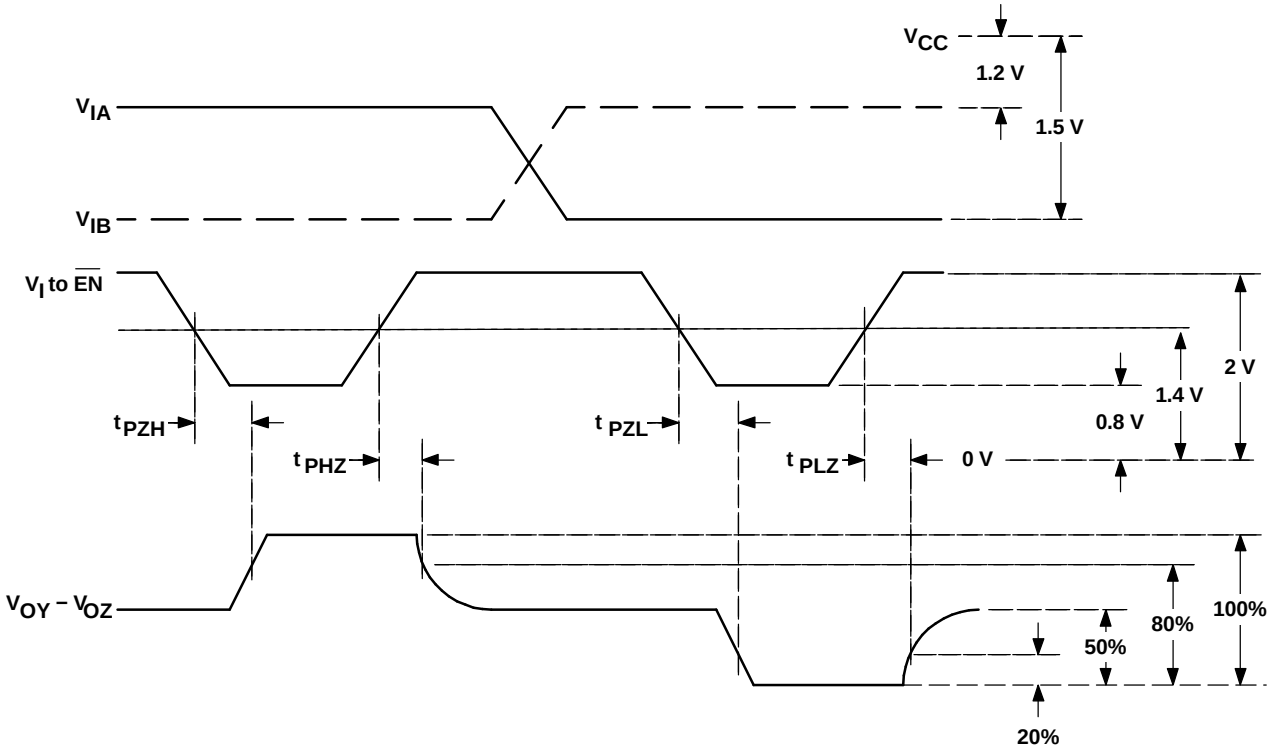


Figure 6. Enable and Disable Time Test Waveforms

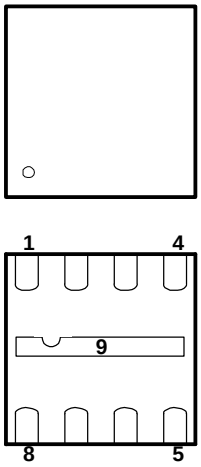
DEVICE INFORMATION

FUNCTION TABLE(1)

A	B	$\overline{EN}$	Y	Z
H	H	L	?	?
L	H	L	L	H
H	L	L	H	L
L	L	L	?	?
X	X	H	Z	Z
Open	Open	L	?	?
X	X	Open	?	?

(1) H = high, L = low, Z = high impedance, ? = indeterminate

TOP VIEW



BOTTOM VIEW

Package Pin Assignments - Numerical Listing

PIN	SIGNAL	PIN	SIGNAL
1	NC	6	Z
2	A	7	Y
3	B	8	V_{CC}
4	V_{BB}	9	GND
5	$\overline{EN}$		

Package Pin Assignments - Alphabetical Listing

SIGNAL	PIN	SIGNAL	PIN
A	2	V_{BB}	4
B	3	V_{CC}	8
$\overline{EN}$	5	Y	7
GND	9	Z	6
NC	1		

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

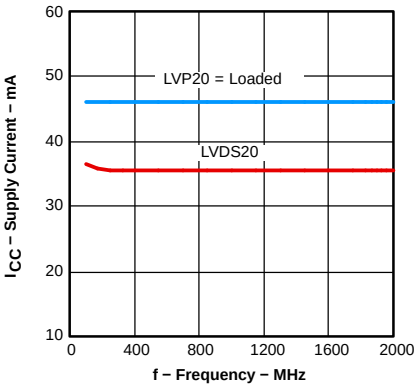


Figure 7.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

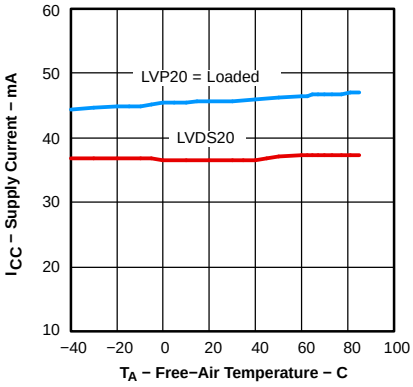


Figure 8.

DIFFERENTIAL OUTPUT VOLTAGE vs FREQUENCY

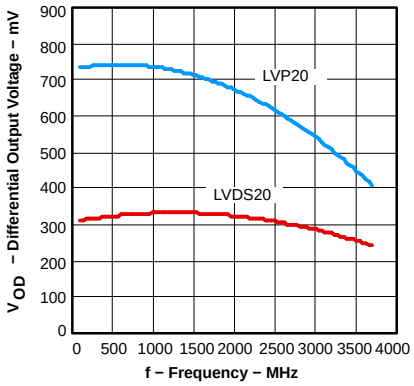


Figure 9.

LVDS20 RISE/FALL TIME vs FREE-AIR TEMPERATURE

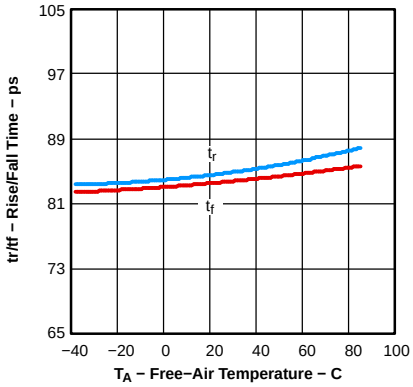


Figure 10.

LVP20 RISE/FALL TIME vs FREE-AIR TEMPERATURE

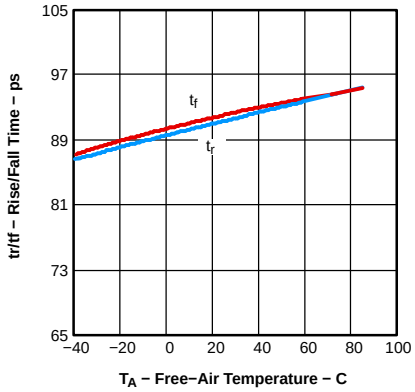


Figure 11.

LVDS20 PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

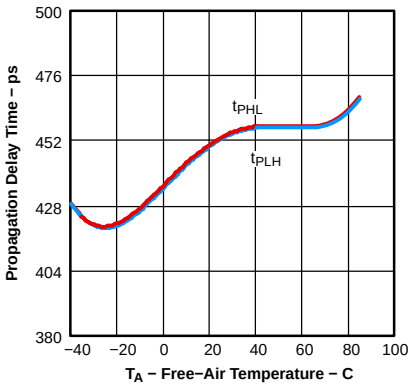


Figure 12.

TYPICAL CHARACTERISTICS (continued)

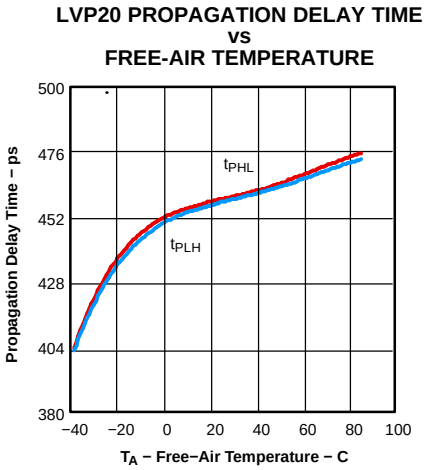


Figure 13.

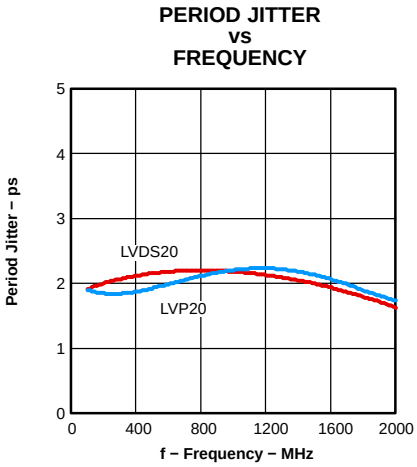


Figure 14.

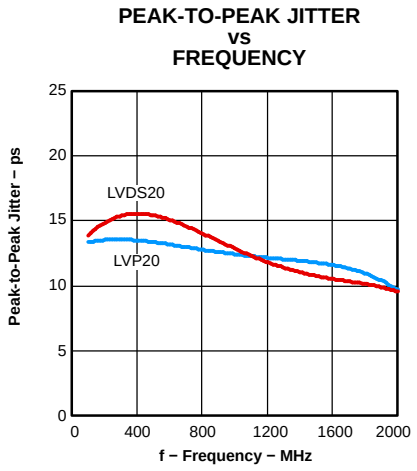


Figure 15.

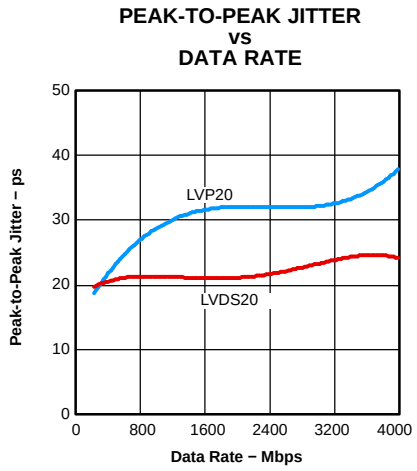


Figure 16.

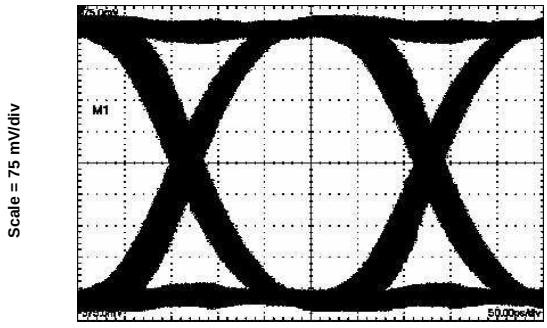


Figure 17. LVDS20 4-Gbps, 2^{23} - 1 PRBS

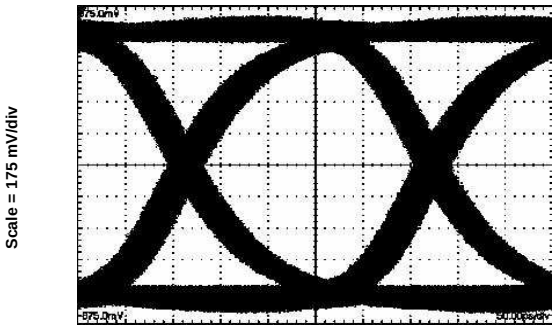


Figure 18. LVP20 4-Gbps, 2^{23} - 1 PRBS

TYPICAL CHARACTERISTICS (continued)

PHASE NOISE OF SN65LVP20

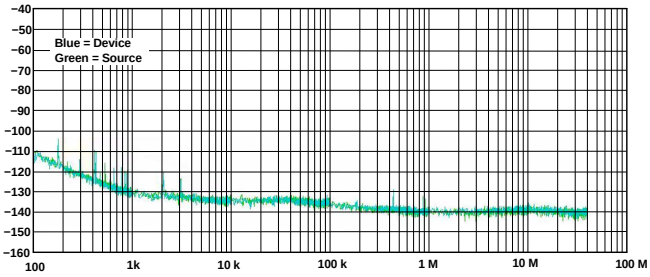


Figure 19. Frequency Offset From 155.52 MHz Carrier

PHASE NOISE OF SN65LVP20

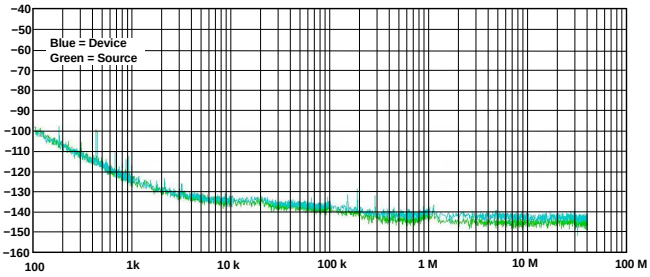
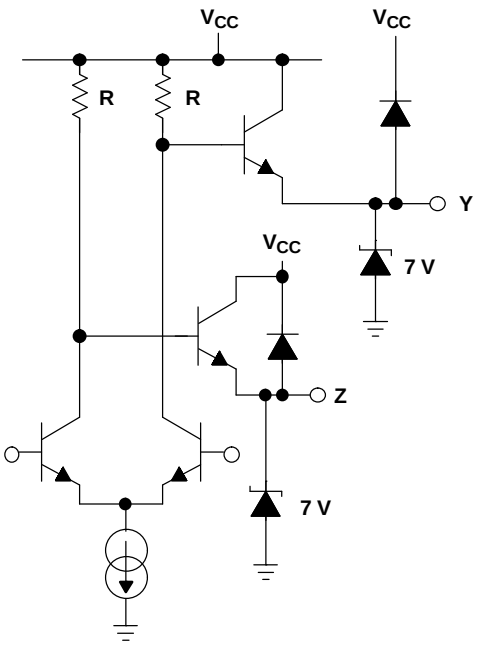


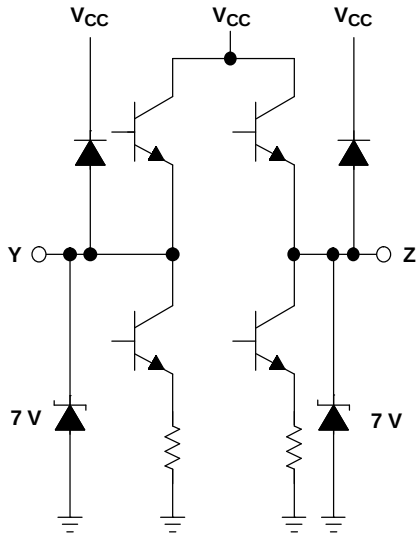
Figure 20. Frequency Offset From 622.08 MHz Carrier

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

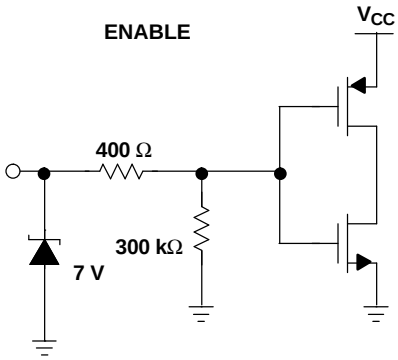
OUTPUT LVP20



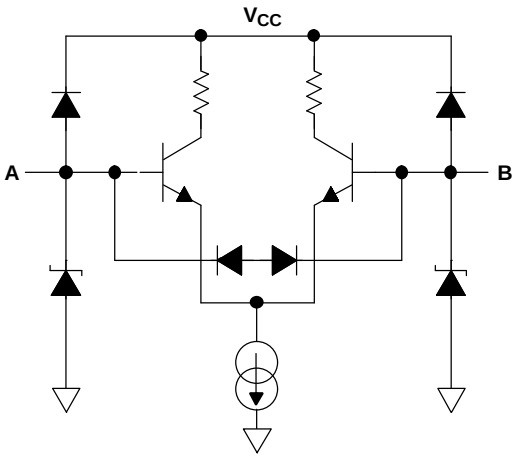
OUTPUT LVDS20



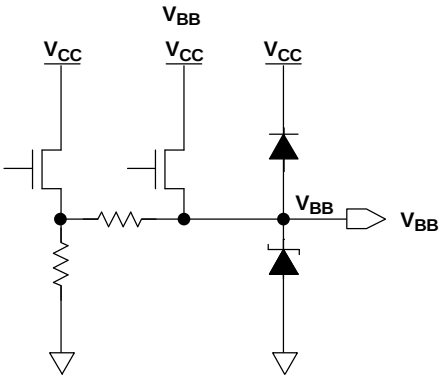
ENABLE



INPUT



OUTPUT



PACKAGING INFORMATION

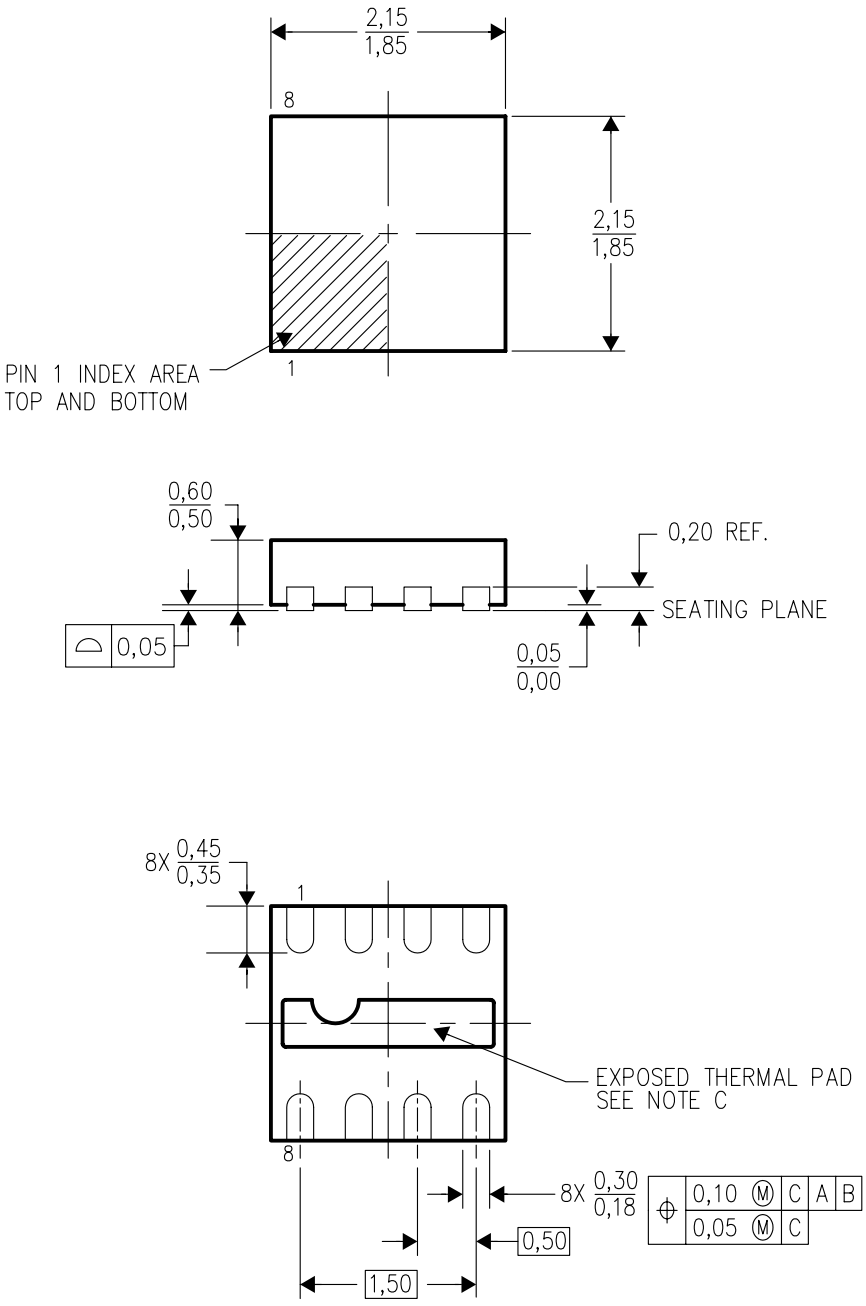
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LVDS20DRFR	ACTIVE	SON	DRF	8	3000	None	CU NIPD	Level-1-220C-UNLIM
SN65LVDS20DRFT	ACTIVE	SON	DRF	8	250	None	CU NIPD	Level-1-220C-UNLIM
SN65LVP20DRFR	ACTIVE	SON	DRF	8	3000	None	CU NIPD	Level-1-220C-UNLIM
SN65LVP20DRFT	ACTIVE	SON	DRF	8	250	None	CU NIPD	Level-1-220C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

DRF (S–PDSO–N8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
D. Falls within JEDEC MO–229.

IMPORTANT NOTICE

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