

SN65LVDS387, SN75LVDS387, SN65LVDS389 SN75LVDS389, SN65LVDS391, SN75LVDS391 HIGH-SPEED DIFFERENTIAL LINE DRIVERS

SLLS362D – SEPTEMBER 1999 – REVISED MAY 2001

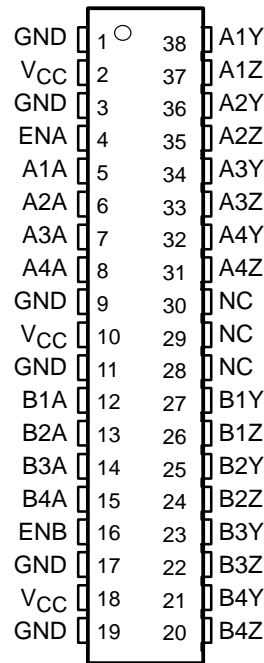
- Four ('391), Eight ('389) or Sixteen ('387) Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard
- Designed for Signaling Rates† up to 630 Mbps With Very Low Radiation (EMI)
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load
- Propagation Delay Times Less Than 2.9 ns
- Output Skew Is Less Than 150 ps
- Part-to-Part Skew Is Less Than 1.5 ns
- 35-mW Total Power Dissipation in Each Driver Operating at 200 MHz
- Driver Is High Impedance When Disabled or With $V_{CC} < 1.5$ V
- SN65' Version Bus-Pin ESD Protection Exceeds 15 kV
- Packaged in Thin Shrink Small-Outline Package With 20-mil Terminal Pitch
- Low-Voltage TTL (LVTTTL) Logic Inputs Are 5-V Tolerant

description

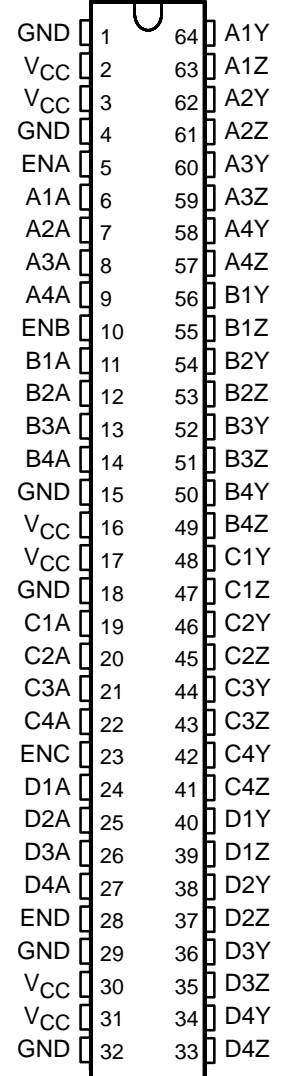
This family of four, eight, and sixteen differential line drivers implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the sixteen current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

The intended application of this device and signaling technique is for point-to-point and multidrop baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media can be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with the companion 16- or 8-channel receivers, the SN65LVDS386 or SN65LVDS388, over 300 million data transfers per second in single-edge clocked systems are possible with very little power. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

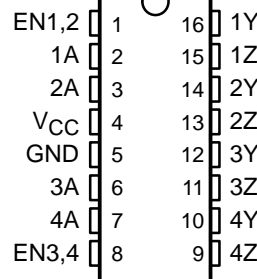
'LVDS389
DBT PACKAGE
(TOP VIEW)



'LVDS387
DGG PACKAGE
(TOP VIEW)



'LVDS391
D OR PW PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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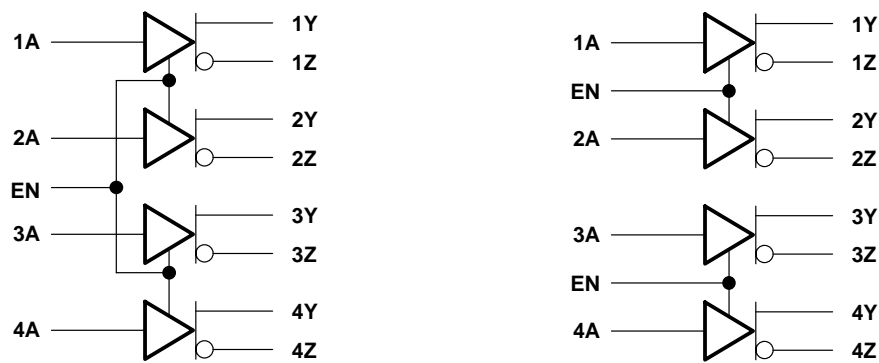
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description (continued)

When disabled, the driver outputs are high impedance. Each driver input (A) and enable (EN) have an internal pulldown that will drive the input to a low level when open circuited.

The SN65LVDS387, SN65LVDS389, and SN65LVDS391 are characterized for operation from -40°C to 85°C . The SN75LVDS387, SN75LVDS389, and SN75LVDS391 are characterized for operation from 0°C to 70°C .

logic diagram (positive logic)



(1/4 of 'LVDS387 or 1/2 of 'LVDS389 shown)

('LVDS391 shown)

AVAILABLE OPTIONS

PART NUMBER†	TEMPERATURE RANGE	NO. OF DRIVERS	BUS-PIN ESD
SN65LVDS387DGG	-40°C to 85°C	16	15 kV
SN75LVDS387DGG	0°C to 70°C	16	4 kV
SN65LVDS389DBT	-40°C to 85°C	8	15 kV
SN75LVDS389DBT	0°C to 70°C	8	4 kV
SN65LVDS391D	-40°C to 85°C	4	15 kV
SN75LVDS391D	0°C to 70°C	4	4 kV
SN65LVDS391PW	-40°C to 85°C	4	15 kV
SN75LVDS391PW	0°C to 70°C	4	4 kV

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., SN65LVDS387DGGR).

DRIVER FUNCTION TABLE

INPUT	ENABLE	OUTPUTS	
A	EN	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z
OPEN	H	L	H

H = high-level, L = low-level, X = irrelevant,
Z = high-impedance (off)

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electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OD}	Differential output voltage magnitude	R _L = 100 Ω, See Figure 1 and Figure 2	247	340	454	mV
Δ V _{OD}	Change in differential output voltage magnitude between logic states		-50		50	
V _{OC(SS)}	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between logic states		-50		50	mV
V _{OC(PP)}	Peak-to-peak common-mode output voltage			50	150	mV
I _{CC}	Supply current	'LVDS387	Enabled, R _L = 100 Ω, V _{IN} = 0.8 V or 2 V	85	95	mA
		'LVDS389		50	70	
		'LVDS391		20	26	
		'LVDS387	Disabled, V _{IN} = 0 V or V _{CC}	0.5	1.5	
		'LVDS389		0.5	1.5	
		'LVDS391		0.5	1.3	
I _{IH}	High-level input current	V _{IH} = 2 V		3	20	μA
I _{IL}	Low-level input current	V _{IL} = 0.8 V		2	10	μA
I _{OS}	Short-circuit output current	V _{OY} or V _{OZ} = 0 V			±24	mA
		V _{OD} = 0 V			±12	mA
I _{OZ}	High-impedance output current	V _O = 0 V or V _{CC}			±1	μA
I _{O(OFF)}	Power-off output current	V _{CC} = 1.5 V, V _O = 2.4 V			±1	μA
C _{IN}	Input capacitance	V _I = 0.4 sin(4E6πt) + 0.5 V		5		pF
C _O	Output capacitance	V _I = 0.4 sin(4E6πt) + 0.5 V, Disabled		9.4		pF

† All typical values are at 25°C and with a 3.3-V supply.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	R _L = 100 Ω, C _L = 10 pF, See Figure 4	0.9	1.7	2.9	ns
t _{PHL}	Propagation delay time, high-to-low-level output		0.9	1.6	2.9	ns
t _r	Differential output signal rise time		0.4	0.8	1	ns
t _f	Differential output signal fall time		0.4	0.8	1	ns
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})			150	500	ps
t _{sk(o)}	Output skew‡			80	150	ps
t _{sk(pp)}	Part-to-part skew§				1.5	ns
t _{PZH}	Propagation delay time, high-impedance-to-high-level output		See Figure 5	6.4		15
t _{PZL}	Propagation delay time, high-impedance-to-low-level output	5.9			15	ns
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output	3.5			15	ns
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output	4.5			15	ns

† All typical values are at 25°C and with a 3.3-V supply.

‡ t_{sk(o)} is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.

§ t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of any two devices characterized in this data sheet when both devices operate with the same supply voltage, at the same temperature, and have the same test circuits.



PARAMETER MEASUREMENT INFORMATION

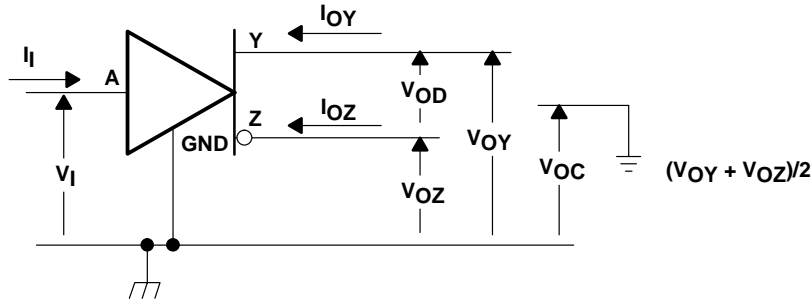


Figure 1. Voltage and Current Definitions

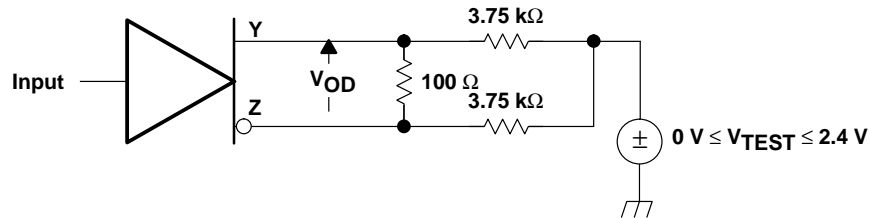
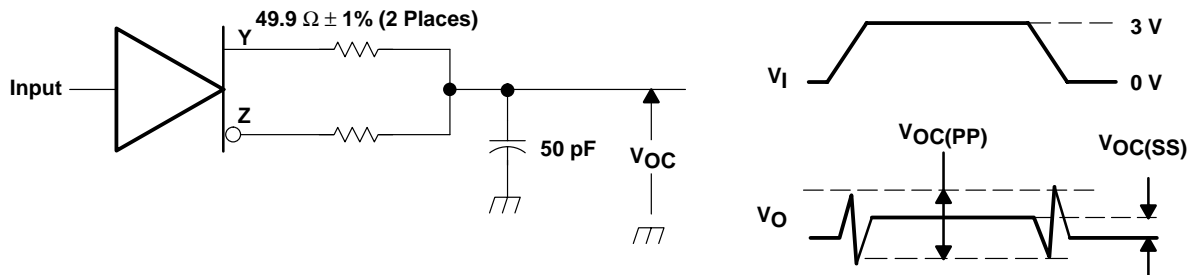
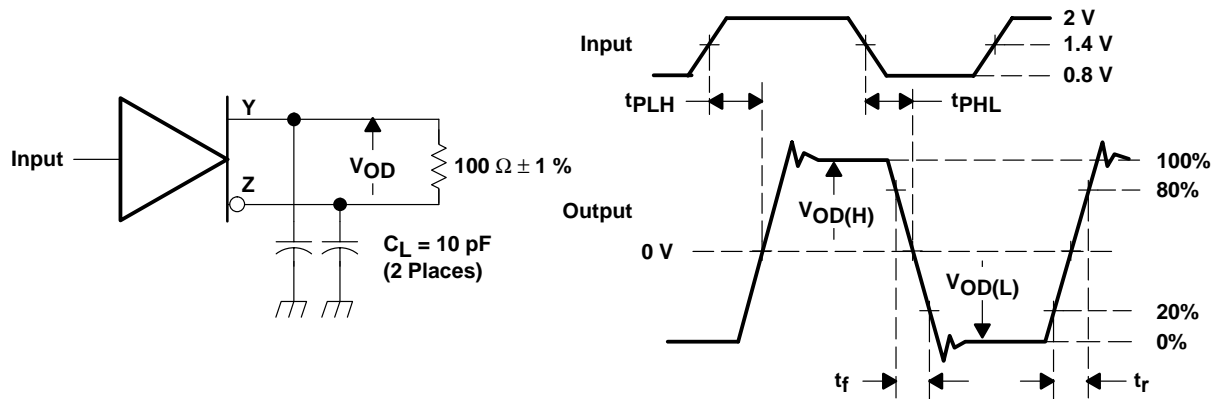


Figure 2. VOD Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



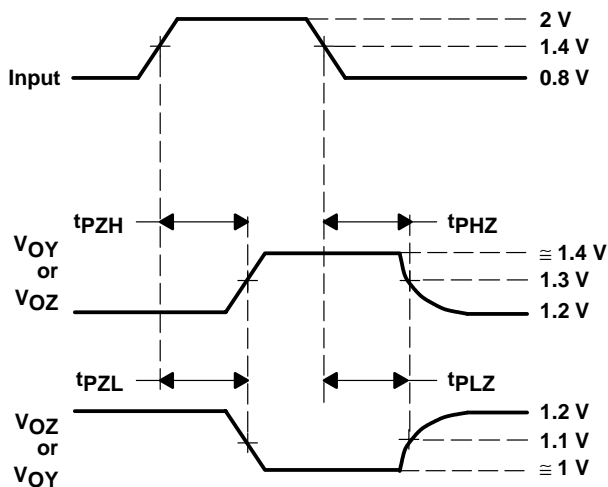
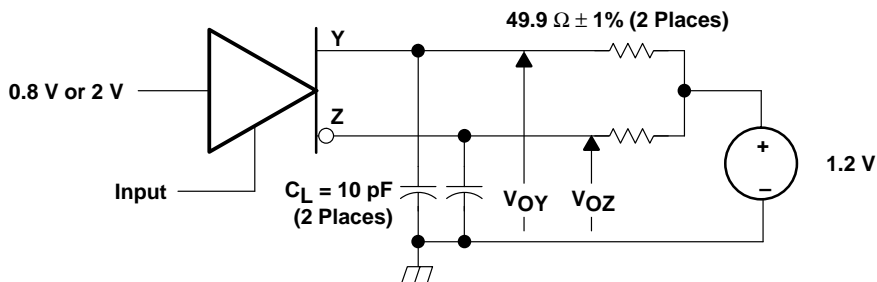
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

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PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

TYPICAL CHARACTERISTICS

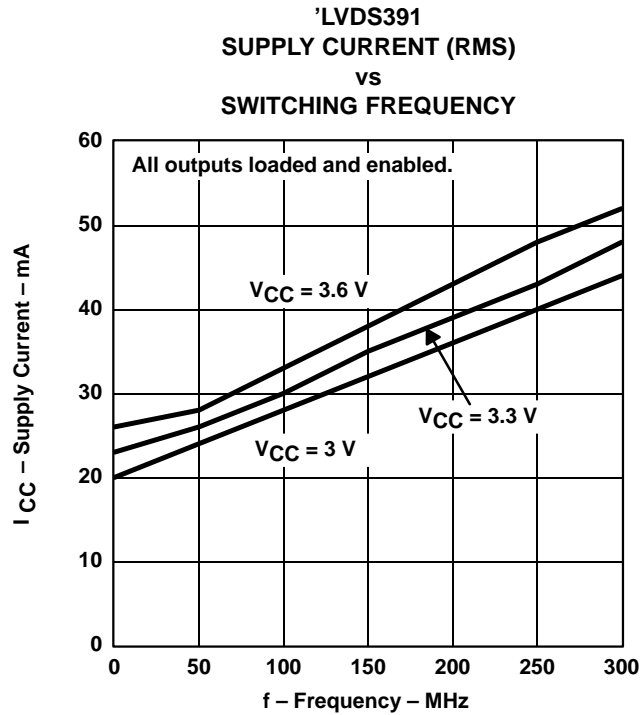


Figure 6

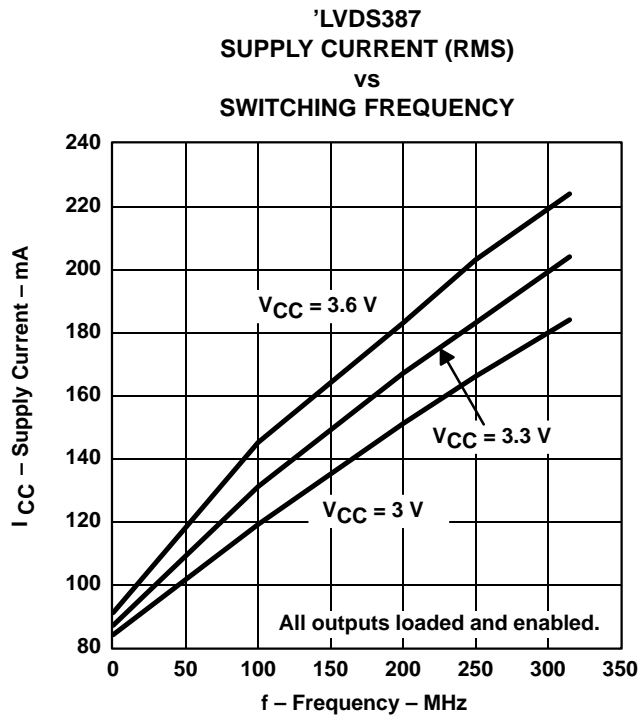


Figure 7

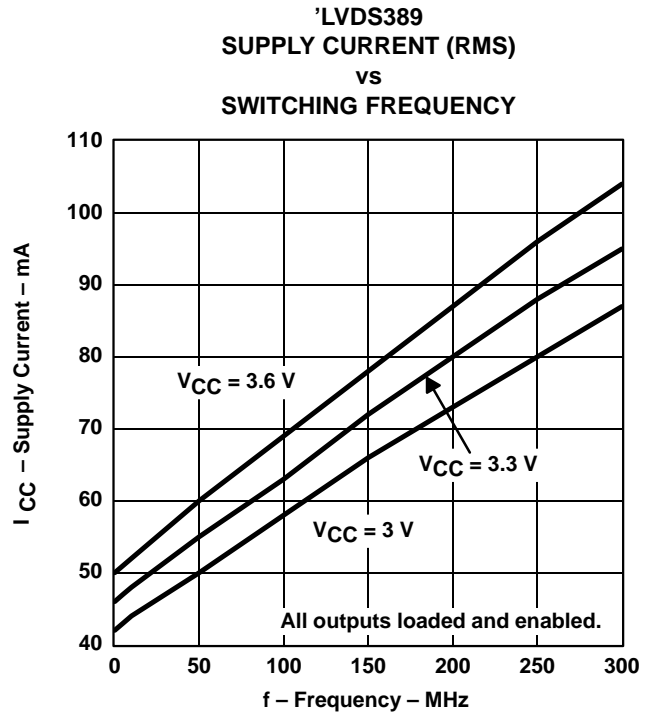


Figure 8

TYPICAL CHARACTERISTICS

LOW-TO-HIGH PROPAGATION DELAY TIME
 vs
 FREE-AIR TEMPERATURE

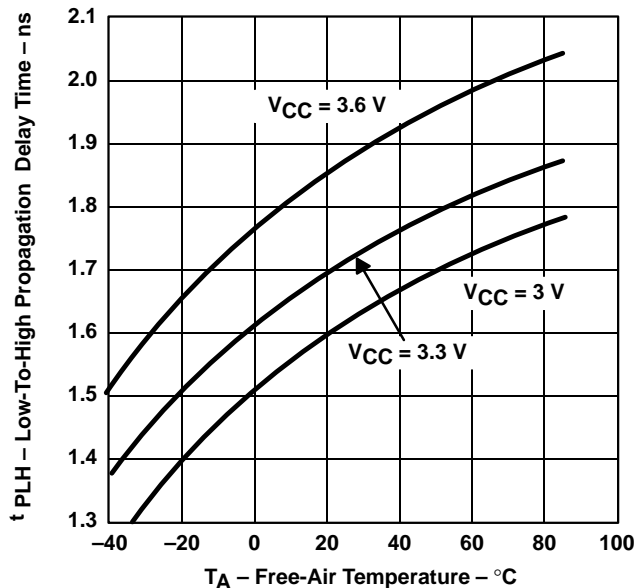


Figure 9

HIGH-TO-LOW PROPAGATION DELAY TIME
 vs
 FREE-AIR TEMPERATURE

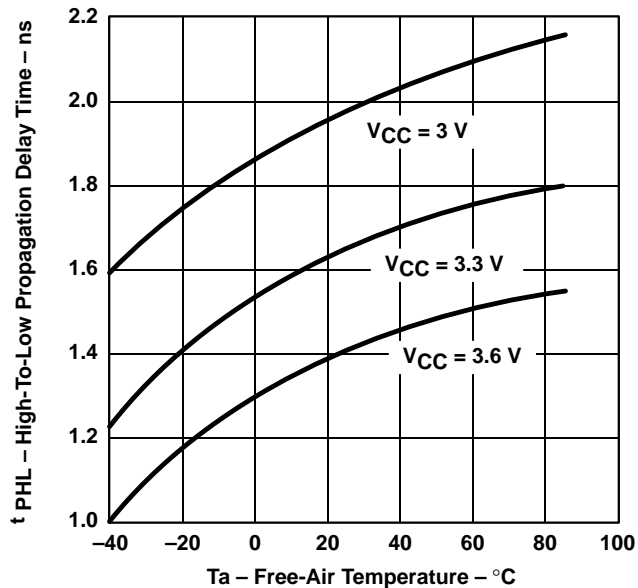


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
 vs
 LOW-LEVEL OUTPUT CURRENT

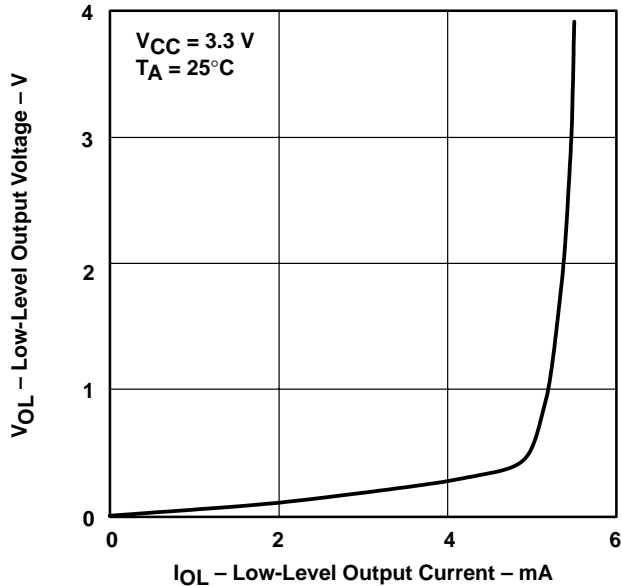


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
 vs
 HIGH-LEVEL OUTPUT CURRENT

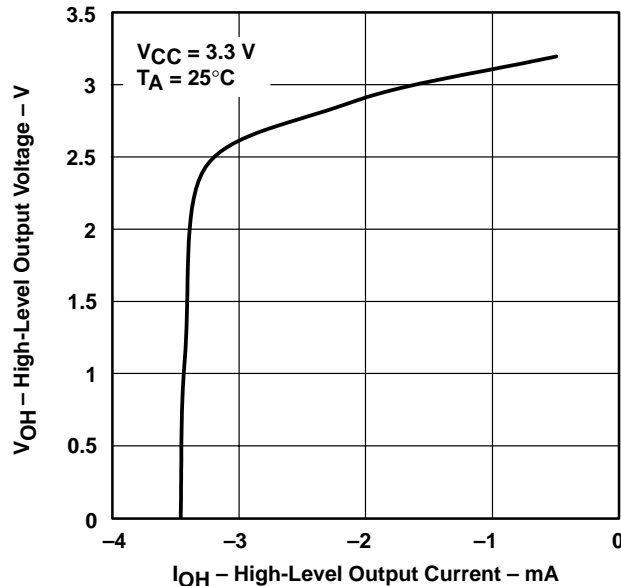
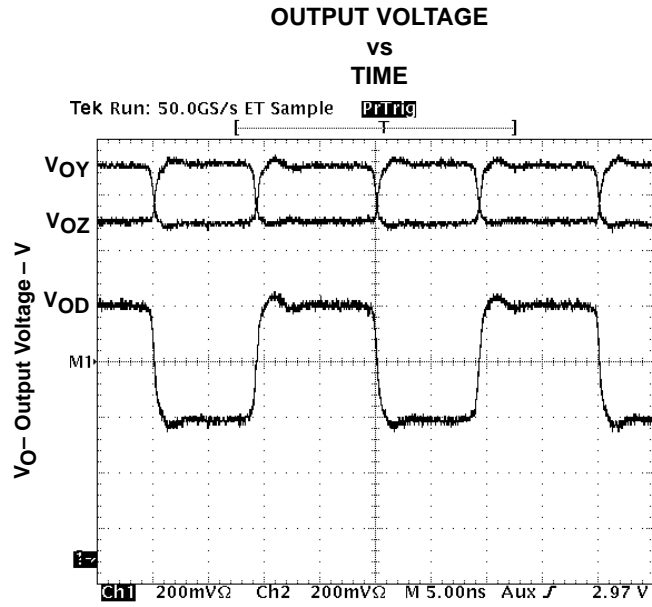


Figure 12

TYPICAL CHARACTERISTICS



t – Time – ns

Figure 13

**SN65LVDS387, SN75LVDS387, SN65LVDS389
SN75LVDS389, SN65LVDS391, SN75LVDS391
HIGH-SPEED DIFFERENTIAL LINE DRIVERS**

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APPLICATION INFORMATION

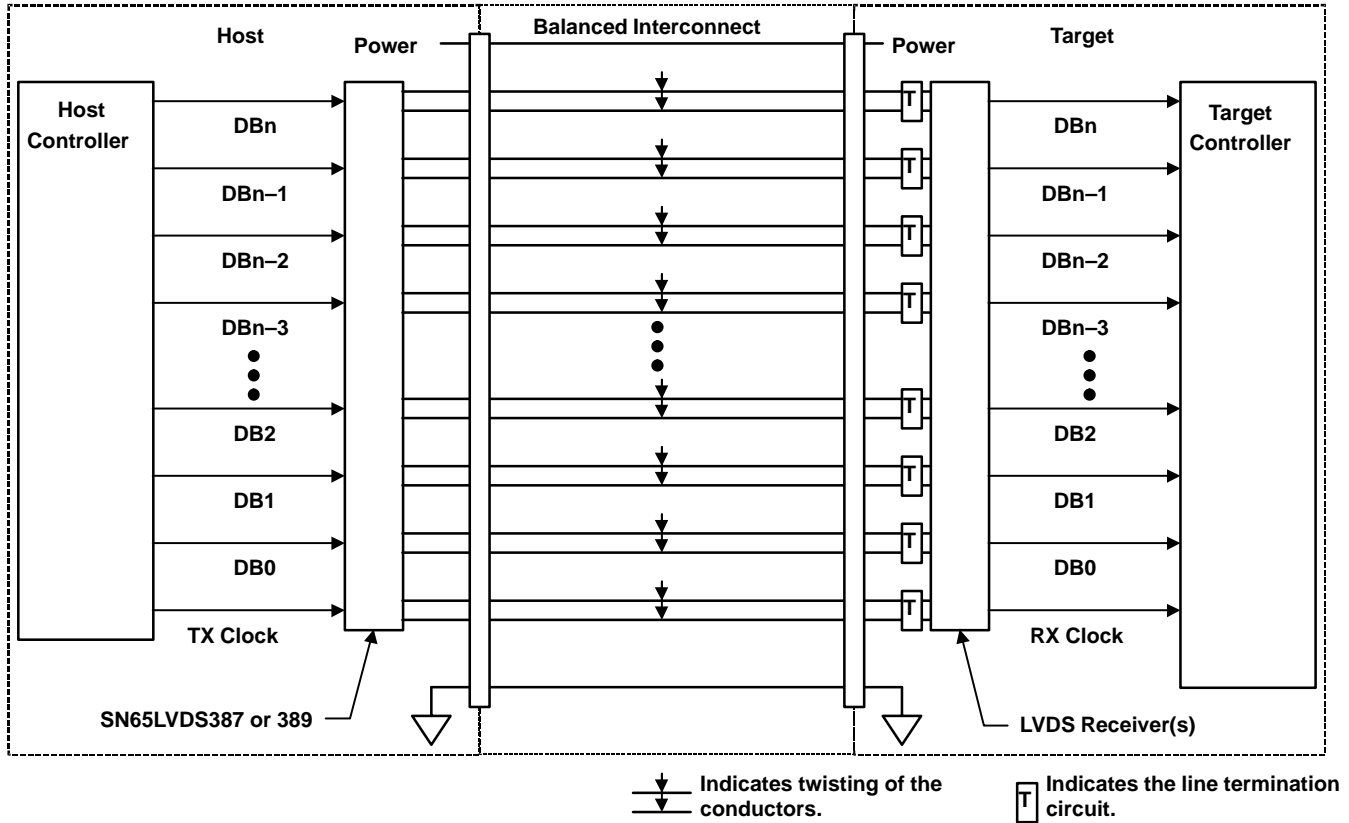


Figure 14. Typical Application Schematic

Signaling Rate vs Distance

The ultimate data transfer rate over a given cable or trace length involves many variables. Starting with the capabilities of this LVDS driver to reproduce a data pulse as short as 1.6 ns (a 630 Mbps signaling rate) with less than 500 ps of pulse distortion, any degradation of this pulse by the transmission media will necessarily reduce the timing margin at the receiving end of the data link.

The timing uncertainty induced by the transmission media is commonly referred to as jitter and comes from numerous sources. The characteristics of a particular transmission media can be quantified by using an eyepattern measurement such as shown in Figure 12, which shows about 340 ps of jitter or 20% of the data pulse width.

APPLICATION INFORMATION

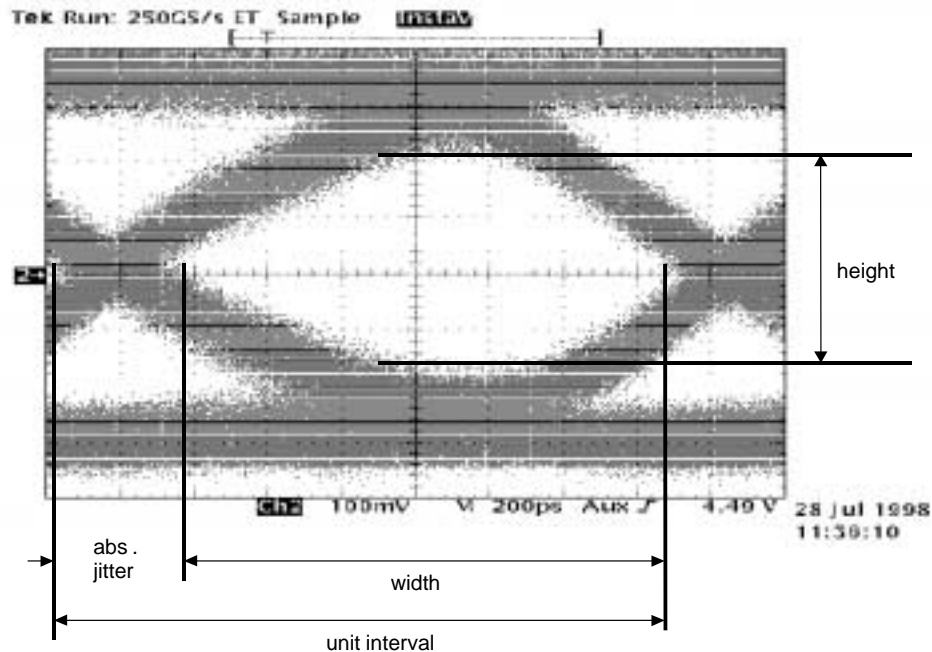


Figure 15. Typical LVDS Eyepattern

A generally accepted range of jitter at the receiver inputs that allows data recovery is 5% to 20% of the unit interval (data pulse width). Table 1 shows the signaling rate achieved on various cables and lengths at a 5% eyepattern jitter with a typical LVDS driver.

Table 1. Signaling Rates for Various Cables for 5% Eyepattern Jitter

LENGTH (m)	CABLE†					
	A (Mbps)	B (Mbps)	C (Mbps)	D (Mbps)	E (Mbps)	F (Mbps)
1	240	200	240	270	180	230
5	205	210	230	250	215	230
10	180	150	195	200	145	180

† Cable A: CAT 3, specified up to 16 MHz, no shield, outside conductor diameter (Ø) 0.52 mm

Cable B: CAT 5, specified up to 100 MHz, no shield, Ø 0.52 mm

Cable C: CAT 5, specified up to 100 MHz, taped over all shield, Ø 0.52 mm

Cable D: CAT 5 (exceeding CAT 5), specified up to 300 MHz, braided over all shield plus taped individual shield for any pair, Ø 0.64 mm (AWG22)

Cable E: CAT 5 (exceeding CAT 5), specified up to 350 MHz, Ø 0.64 mm (AWG22), no shield

Cable F: CAT 5 (exceeding CAT 5), specified up to 350 MHz, "self-shielded", Ø 0.64 mm (AWG22)

During synchronous parallel transfers, skew between the data and clock lines will also reduce the timing margin. This must be accounted for in the system timing budget. Fortunately, the low output skew of this LVDS driver will generally be a small portion of this budget.

other LVDS products

For other products and applications notes in the LVDS and LVDM product families visit our Web site at <http://www.ti.com/sc/datatran>.

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HIGH-SPEED DIFFERENTIAL LINE DRIVERS**

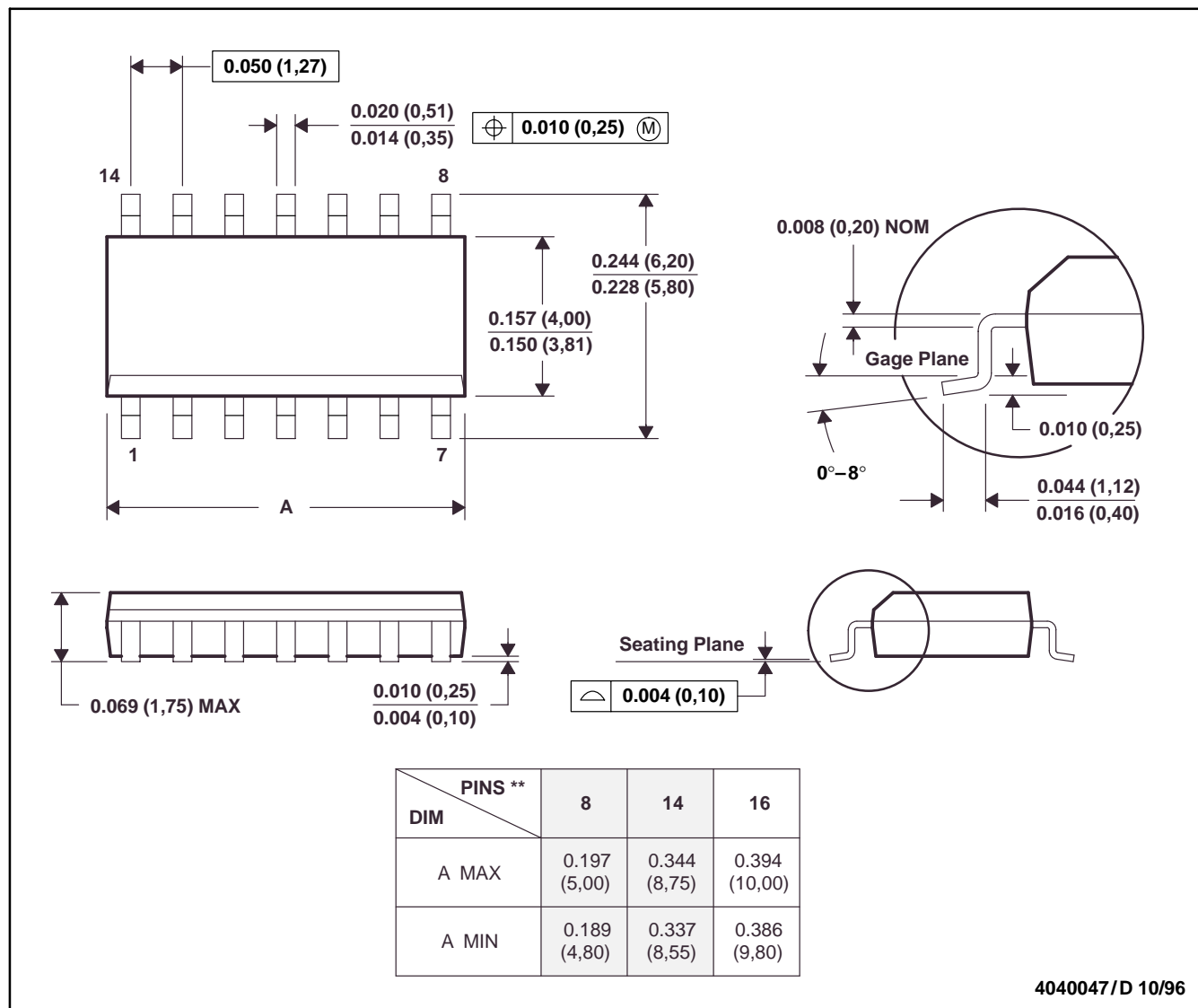
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MECHANICAL DATA

D (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

SN65LVDS387, SN75LVDS387, SN65LVDS389
 SN75LVDS389, SN65LVDS391, SN75LVDS391
 HIGH-SPEED DIFFERENTIAL LINE DRIVERS

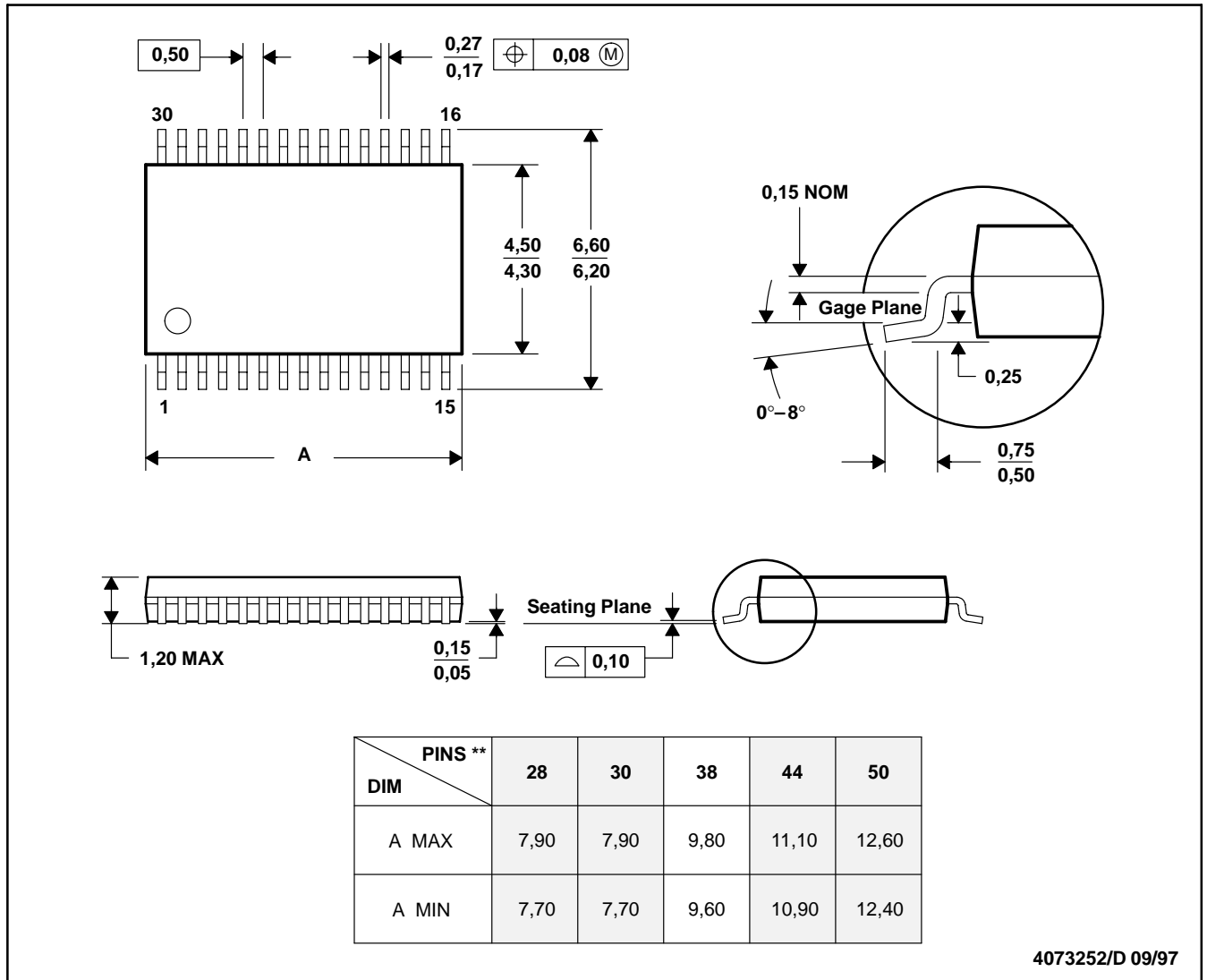
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MECHANICAL DATA

DBT (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

30 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-153

**SN65LVDS387, SN75LVDS387, SN65LVDS389
 SN75LVDS389, SN65LVDS391, SN75LVDS391
 HIGH-SPEED DIFFERENTIAL LINE DRIVERS**

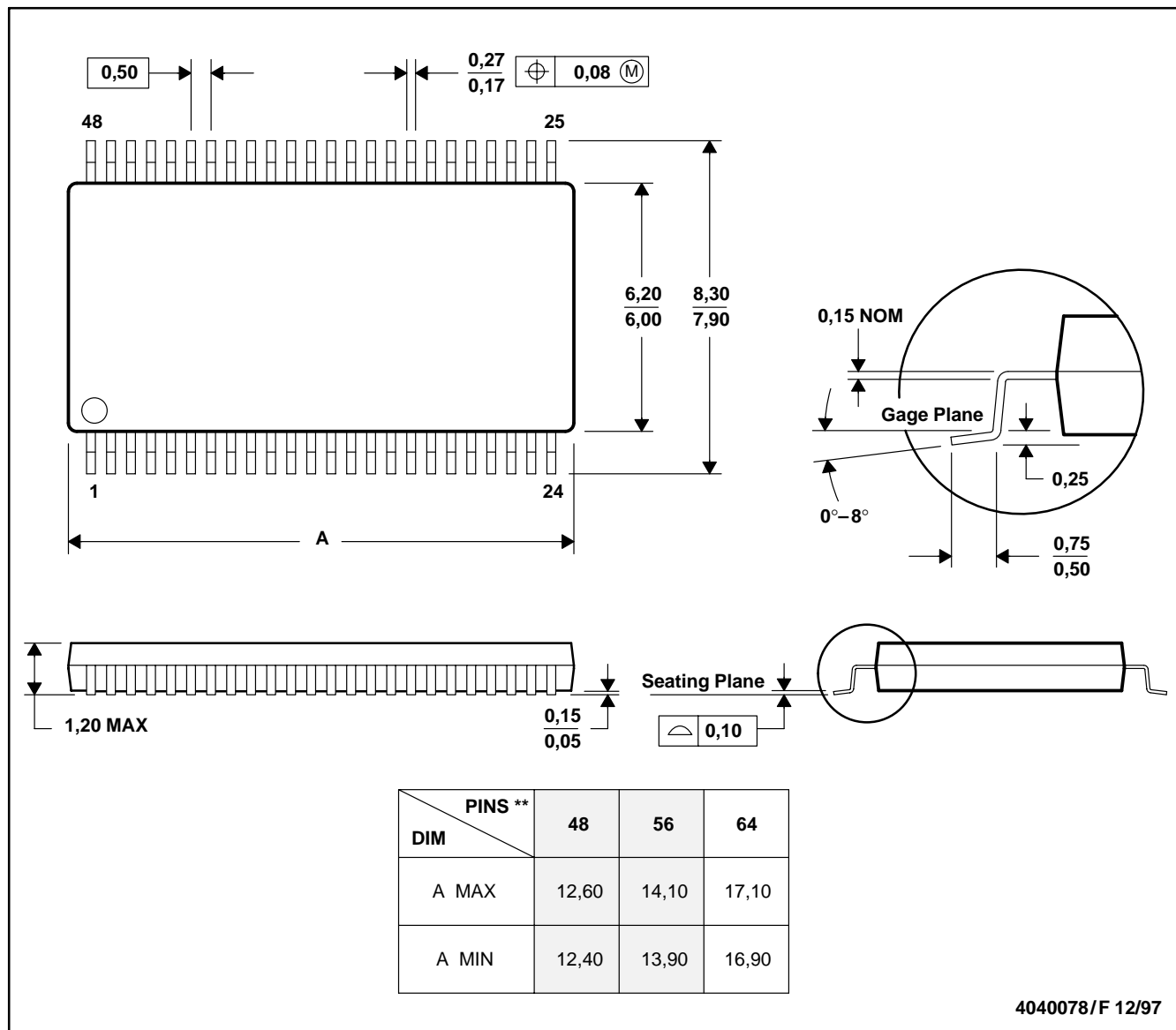
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MECHANICAL DATA

DGG (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



4040078/F 12/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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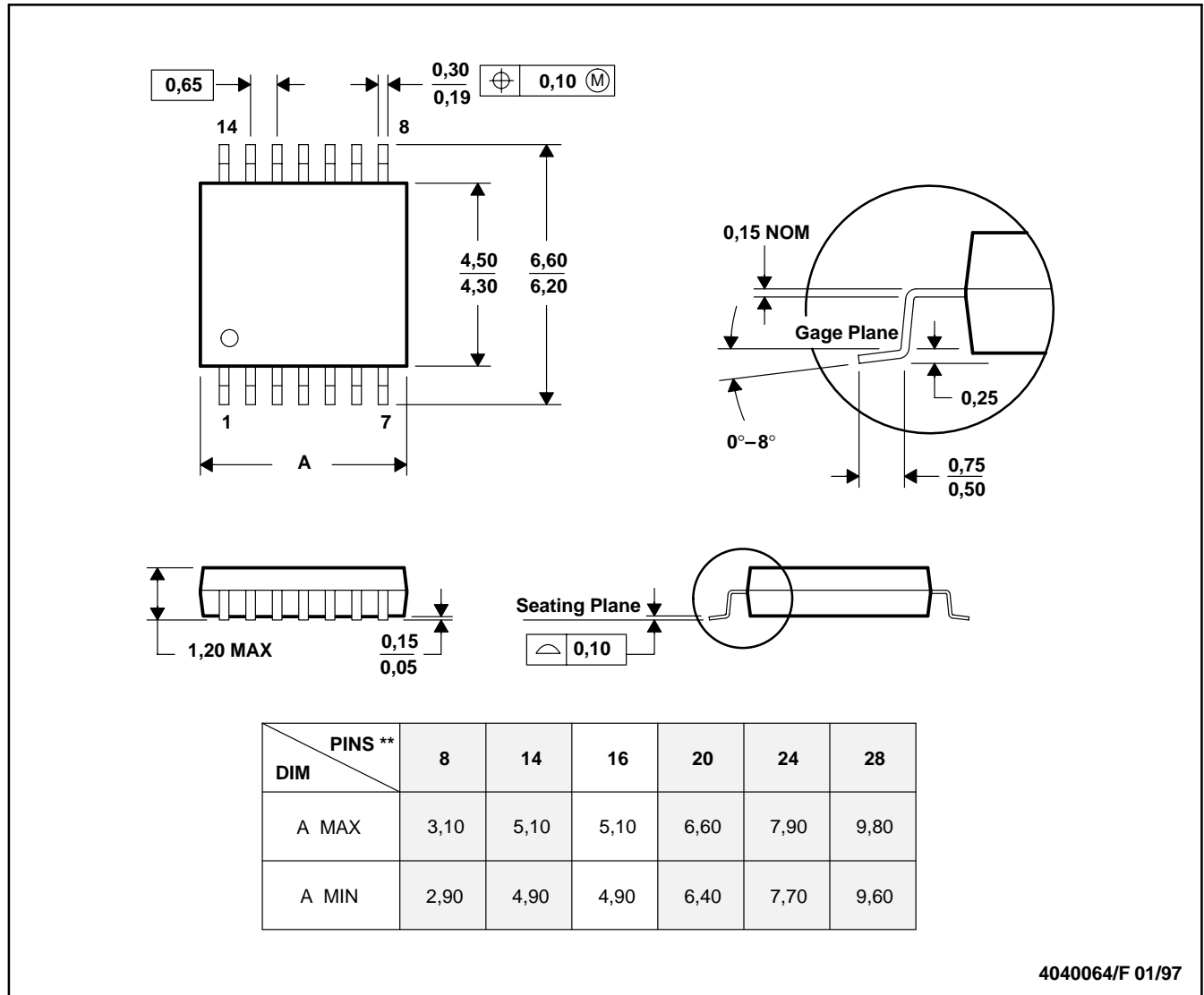
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MECHANICAL DATA

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65LVDS387DGG	ACTIVE	TSSOP	DGG	64	25	None	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS387DGGR	ACTIVE	TSSOP	DGG	64	2000	None	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS389DBT	ACTIVE	SM8	DBT	38	50	None	CU NIPDAU	Level-2-220C-1 YEAR
SN65LVDS389DBTG4	PREVIEW	SM8	DBT	38	50	None	Call TI	Call TI
SN65LVDS389DBTR	ACTIVE	SM8	DBT	38	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
SN65LVDS389DBTRG4	PREVIEW	SM8	DBT	38	2000	None	Call TI	Call TI
SN65LVDS391D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS391DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS391PW	ACTIVE	TSSOP	PW	16	90	None	CU NIPDAU	Level-1-220C-UNLIM
SN65LVDS391PWR	ACTIVE	TSSOP	PW	16	2000	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDS387DGG	ACTIVE	TSSOP	DGG	64	25	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDS387DGGR	ACTIVE	TSSOP	DGG	64	2000	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDS389DBT	ACTIVE	SM8	DBT	38	50	None	CU NIPDAU	Level-2-220C-1 YEAR
SN75LVDS389DBTR	ACTIVE	SM8	DBT	38	2000	None	CU NIPDAU	Level-2-220C-1 YEAR
SN75LVDS389DBTRG4	ACTIVE	SM8	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS391D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN75LVDS391DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN75LVDS391PW	ACTIVE	TSSOP	PW	16	90	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDS391PWR	ACTIVE	TSSOP	PW	16	2000	None	CU NIPDAU	Level-1-220C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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