

SN65LVDS386/388A/390, SN65LVDT386/388A/390 SN75LVDS386/388A/390, SN75LVDT386/388A/390 HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

SLLS394E – SEPTEMBER 1999 – REVISED SEPTEMBER 2002

- Four ('390), Eight ('388A), or Sixteen ('386) Line Receivers Meet or Exceed the Requirements of ANSI TIA/EIA-644 Standard
- Integrated 110-Ω Line Termination Resistors on LVDT Products
- Designed for Signaling Rates[†] Up To 630 Mbps
- SN65 Version's Bus-Terminal ESD Exceeds 15 kV
- Operates From a Single 3.3-V Supply
- Typical Propagation Delay Time of 2.6 ns
- Output Skew 100 ps (Typ)
Part-To-Part Skew Is Less Than 1 ns
- LVTTTL Levels Are 5-V Tolerant
- Open-Circuit Fail Safe
- Flow-Through Pin Out
- Packaged in Thin Shrink Small-Outline Package With 20-mil Terminal Pitch

description

This family of four, eight, or sixteen differential line receivers (with optional integrated termination) implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3-V supply rail. Any of the eight or sixteen differential receivers will provide a valid logical output state with a ± 100 mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes. Additionally, the high-speed switching of LVDS signals almost always requires the use of a line impedance matching resistor at the receiving end of the cable or transmission media. The LVDT products eliminate this external resistor by integrating it with the receiver.

'LVDS388A, 'LVDT388A
DBT PACKAGE
(TOP VIEW)

A1A	1	38	GND
A1B	2	37	V _{CC}
A2A	3	36	ENA
A2B	4	35	A1Y
AGND	5	34	A2Y
B1A	6	33	ENB
B1B	7	32	B1Y
B2A	8	31	B2Y
B2B	9	30	DGND
AGND	10	29	DV _{CC}
C1A	11	28	DGND
C1B	12	27	C1Y
C2A	13	26	C2Y
C2B	14	25	ENC
AGND	15	24	D1Y
D1A	16	23	D2Y
D1B	17	22	END
D2A	18	21	V _{CC}
D2B	19	20	GND

See application section for V_{CC} and GND description.

'LVDS390, 'LVDT390
D OR PW PACKAGE
(TOP VIEW)

1A	1	16	EN1,2
1B	2	15	1Y
2A	3	14	2Y
2B	4	13	V _{CC}
3A	5	12	GND
3B	6	11	3Y
4A	7	10	4Y
4B	8	9	EN3,4

'LVDS386, 'LVDT386
DGG PACKAGE
(TOP VIEW)

A1A	1	64	GND
A1B	2	63	V _{CC}
A2A	3	62	V _{CC}
A2B	4	61	GND
A3A	5	60	ENA
A3B	6	59	A1Y
A4A	7	58	A2Y
A4B	8	57	A3Y
B1A	9	56	A4Y
B1B	10	55	ENB
B2A	11	54	B1Y
B2B	12	53	B2Y
B3A	13	52	B3Y
B3B	14	51	B4Y
B4A	15	50	GND
B4B	16	49	V _{CC}
C1A	17	48	V _{CC}
C1B	18	47	GND
C2A	19	46	C1Y
C2B	20	45	C2Y
C3A	21	44	C3Y
C3B	22	43	C4Y
C4A	23	42	ENC
C4B	24	41	D1Y
D1A	25	40	D2Y
D1B	26	39	D3Y
D2A	27	38	D4Y
D2B	28	37	END
D3A	29	36	GND
D3B	30	35	V _{CC}
D4A	31	34	V _{CC}
D4B	32	33	GND



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†] Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN65LVDS386/388A/390, SN65LVDT386/388A/390 SN75LVDS386/388A/390, SN75LVDT386/388A/390 HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

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description (continued)

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω . The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of receivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with its companion, 8- or 16-channel driver, the SN65LVDS389 or SN65LVDS387, over 300 million data transfers per second in single-edge clocked systems are possible with very little power. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

AVAILABLE OPTIONS

PART NUMBER	TEMPERATURE RANGE	NUMBER OF RECEIVERS	BUS-PIN ESD	SYMBOLIZATION
SN65LVDS386DGG	–40°C to 85°C	16	15 kV	LVDS386
SN65LVDT386DGG	–40°C to 85°C	16	15 kV	LVDT386
SN75LVDS386DGG	0°C to 70°C	16	4 kV	75LVDS386
SN75LVDT386DGG	0°C to 70°C	16	4 kV	75LVDT386
SN65LVDS388ADBT	–40°C to 85°C	8	15 kV	LVDS388A
SN65LVDT388ADBT	–40°C to 85°C	8	15 kV	LVDT388A
SN75LVDS388ADBT	0°C to 70°C	8	4 kV	75LVDS388A
SN75LVDT388ADBT	0°C to 70°C	8	4 kV	75LVDT388A
SN65LVDS390D	–40°C to 85°C	4	15 kV	LVDS390
SN65LVDS390PW	–40°C to 85°C	4	15 kV	LVDS390
SN65LVDT390D	–40°C to 85°C	4	15 kV	LVDT390
SN65LVDT390PW	–40°C to 85°C	4	15 kV	LVDT390
SN75LVDS390D	0°C to 70°C	4	4 kV	75LVDS390
SN75LVDS390PW	0°C to 70°C	4	4 kV	DS390
SN75LVDT390D	0°C to 70°C	4	4 kV	75LVDT390
SN75LVDT390PW	0°C to 70°C	4	4 kV	DG390

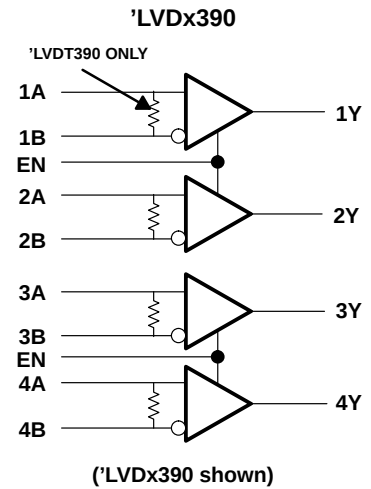
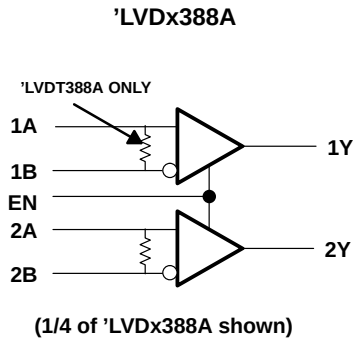
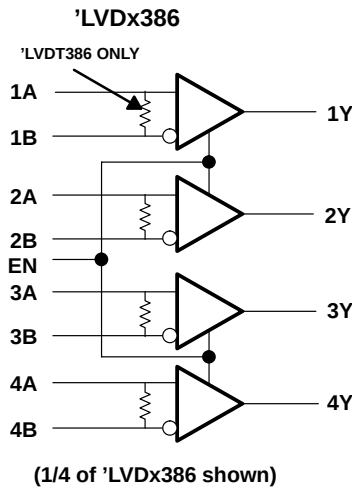


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logic diagram (positive logic)



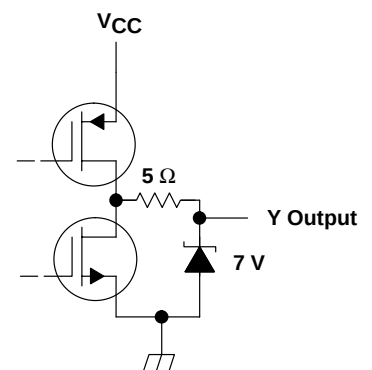
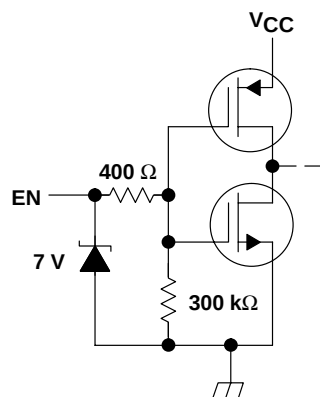
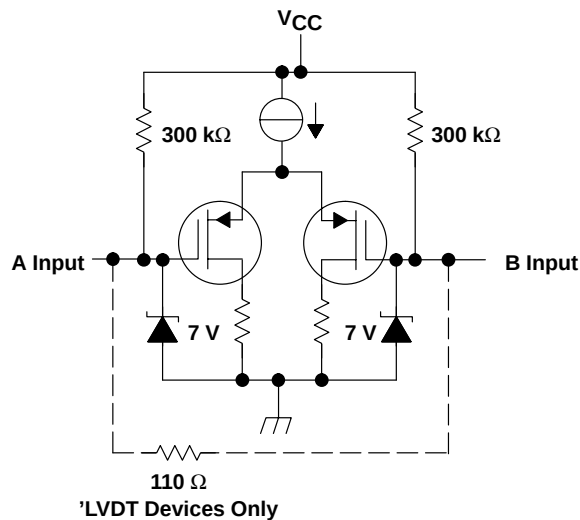
Function Table

SNx5LVDS386/388A/390 and SNx5LVDT386/388A/390

DIFFERENTIAL INPUT	ENABLES	OUTPUT
A-B	EN	Y
$V_{ID} \geq 100 \text{ mV}$	H	H
$-100 \text{ mV} < V_{ID} \leq 100 \text{ mV}$	H	?
$V_{ID} \leq -100 \text{ mV}$	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

equivalent input and output schematic diagrams



SN65LVDS386/388A/390, SN65LVDT386/388A/390 SN75LVDS386/388A/390, SN75LVDT386/388A/390 HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 4 V
Voltage range: Enables or Y	–0.5 V to 6 V
A or B	–0.5 V to 4 V
Electrostatic discharge: (see Note 2)	
SN65' (A, B, and GND)	Class 3, A:15 kV, B: 700 V
SN75' (A, B, and GND)	Class 2, A:4 kV, B: 400 V
Continuous power dissipation	See Dissipation Rating Table
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR [‡] ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
DBT	1071 mW	8.5 mW/°C	688 mW	556 mW
DGG	2094 mW	16.7 mW/°C	1342 mW	1089 mW
PW	774 mW	6.2 mW/°C	496 mW	402 mW

[‡] This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Magnitude of differential input voltage, $ V_{ID} $		0.1		0.6	V
Common-mode input voltage, V_{IC} (see Figure 4)		$\frac{ V_{ID} }{2}$	2.4	$\frac{ V_{ID} }{2}$	V
			$V_{CC} - 0.8$		
Operating free-air temperature, T_A	SN75'	0		70	°C
	SN65'	–40		85	°C



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electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V _{IT+}	Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV
V _{IT−}	Negative-going differential input voltage threshold		−100			mV
V _{OH}	High-level output voltage	I _{OH} = −8 mA	2.4	3		V
V _{OL}	Low-level output voltage	I _{OL} = 8 mA		0.2	0.4	V
I _{CC}	Supply current	'LVDx386	Enabled, No load		50	mA
		'LVDx388A			22	
		'LVDx390			8	
		'LVDx386	Disabled		3	
		'LVDx388A			3	
		'LVDx390			1.5	
I _I	Input current (A or B inputs)	'LVDS	V _I = 0 V	−13	−20	μA
			V _I = 2.4 V	−1.2	−3	
		'LVDT	V _I = 0 V, other input open		−40	
			V _I = 2.4 V, other input open	−2.4		
I _{ID}	Differential input current I _{IA} − I _{IB}	'LVDS	V _{IA} = 0 V, V _{IB} = 0.1 V, V _{IA} = 2.4 V, V _{IB} = 2.3 V		±2	μA
I _{ID}	Differential input current (I _{IA} − I _{IB})	'LVDT	V _{IA} = 0.2 V, V _{IB} = 0 V, V _{IA} = 2.4 V, V _{IB} = 2.2 V	1.5	2.2	mA
I _{I(OFF)}	Power-off Input current (A or B inputs)	'LVDS	V _{CC} = 0 V, V _I = 2.4 V	12	±20	μA
I _{I(OFF)}	Power-off Input current (A or B inputs)	'LVDT	V _{CC} = 0 V, V _I = 2.4 V		±40	μA
I _{IH}	High-level input current (enables)		V _{IH} = 2 V		10	μA
I _{IL}	Low-level input current (enables)		V _{IL} = 0.8 V		10	μA
I _{OZ}	High-impedance output current		V _O = 0 V		±1	μA
			V _O = 3.6 V		10	
C _{IN}	Input capacitance, A or B input to GND		V _{ID} = 0.4 sin 2.5E09 t V	5		pF
Z _(t)	Termination impedance		V _{ID} = 0.4 sin 2.5E09 t V	88	132	Ω

[†] All typical values are at 25°C and with a 3.3-V supply.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	See Figure 2	1	2.6	4	ns
t _{PHL}	Propagation delay time, high-to-low-level output		1	2.5	4	ns
t _r	Output signal rise time		500	800	1200	ps
t _f	Output signal fall time		500	800	1200	ps
t _{sk(p)}	Pulse skew (t _{PHL} − t _{PLH})			150	600	ps
t _{sk(o)}	Output skew [‡]			100	400	ps
t _{sk(pp)}	Part-to-part skew [§]				1	ns
t _{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 3		7	15	ns
t _{PZL}	Propagation delay time, high-impedance-to-low-level output			7	15	ns
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output			7	15	ns
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output			7	15	ns

[†] All typical values are at 25°C and with a 3.3-V supply.

[‡] t_{sk(o)} is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.

[§] t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of any two devices characterized in this data sheet when both devices operate with the same supply voltage, at the same temperature, and have the same test circuits.



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PARAMETER MEASUREMENT INFORMATION

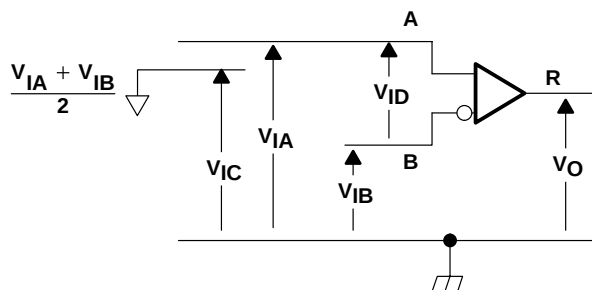
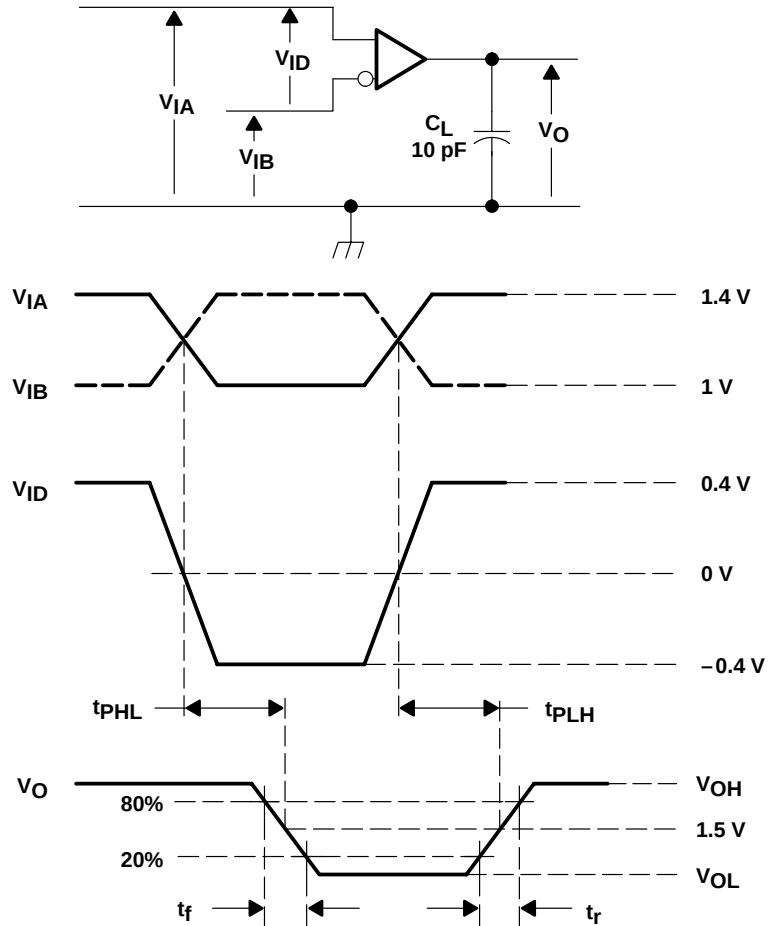


Figure 1. Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	-100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	-100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	-100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	-600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	-600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	-600 mV	0.3 V

PARAMETER MEASUREMENT INFORMATION



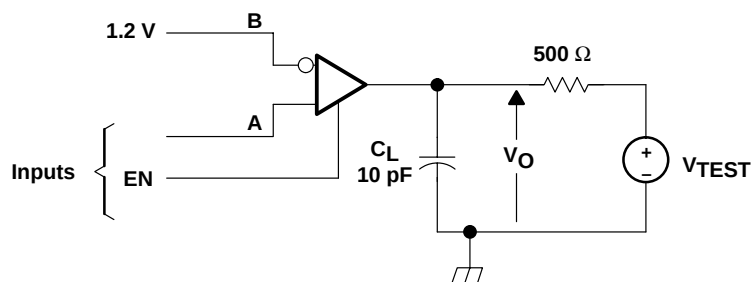
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1 \text{ ns}$, pulse repetition rate (PRR) = 50 Mpps, pulse width = $10 \pm 0.2 \text{ ns}$. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T.

Figure 2. Timing Test Circuit and Wave Forms

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PARAMETER MEASUREMENT INFORMATION



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

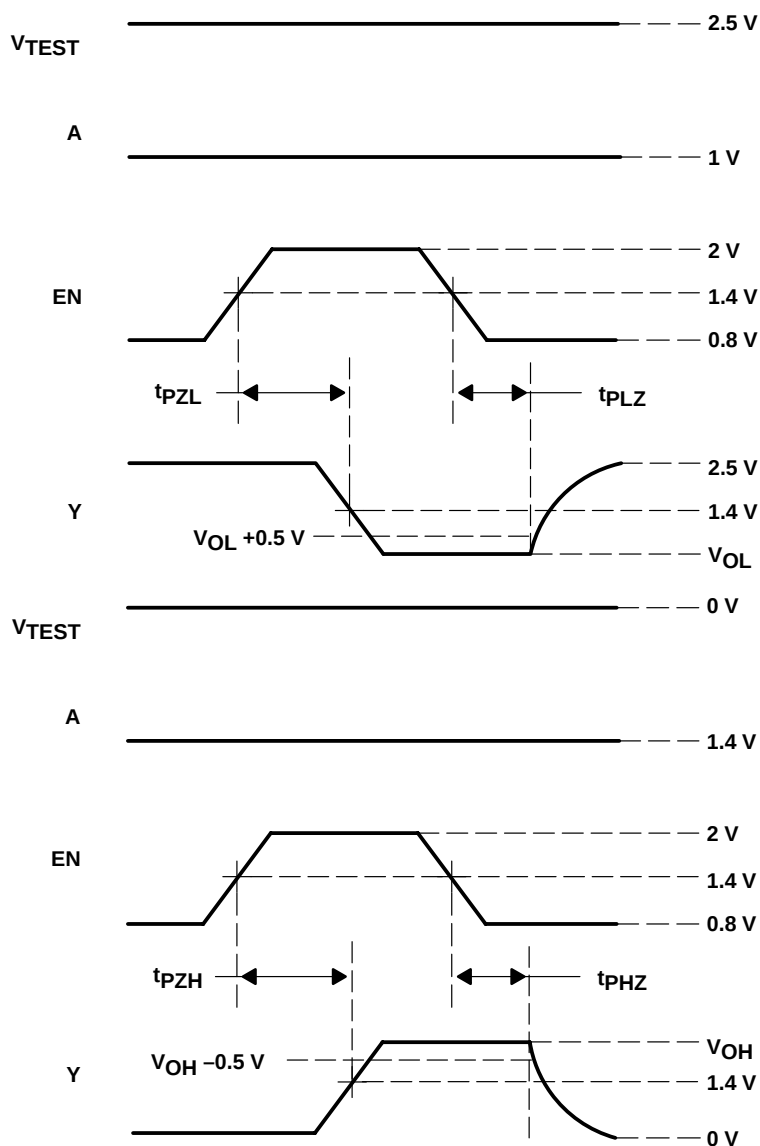


Figure 3. Enable/Disable Time Test Circuit and Wave Forms

TYPICAL CHARACTERISTICS

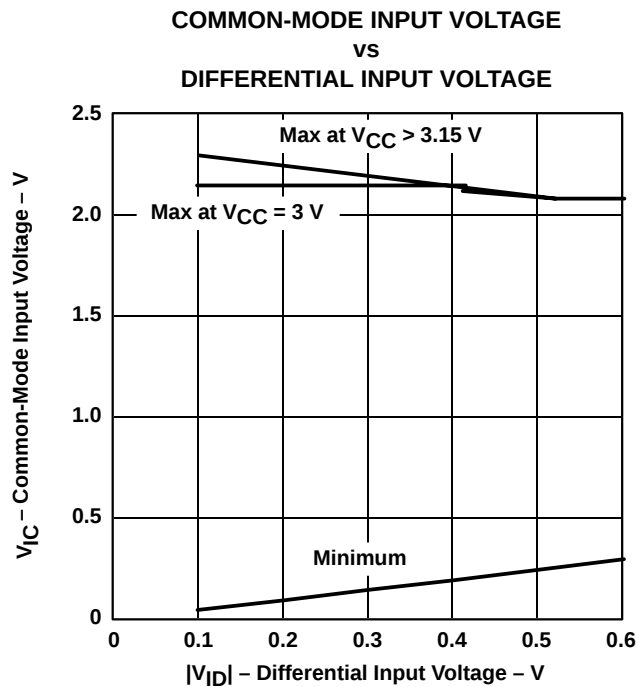


Figure 4

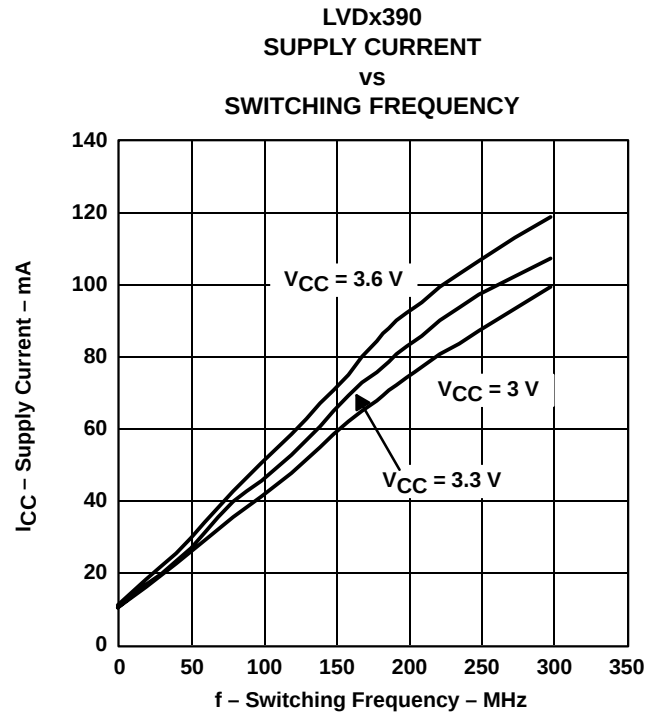


Figure 5

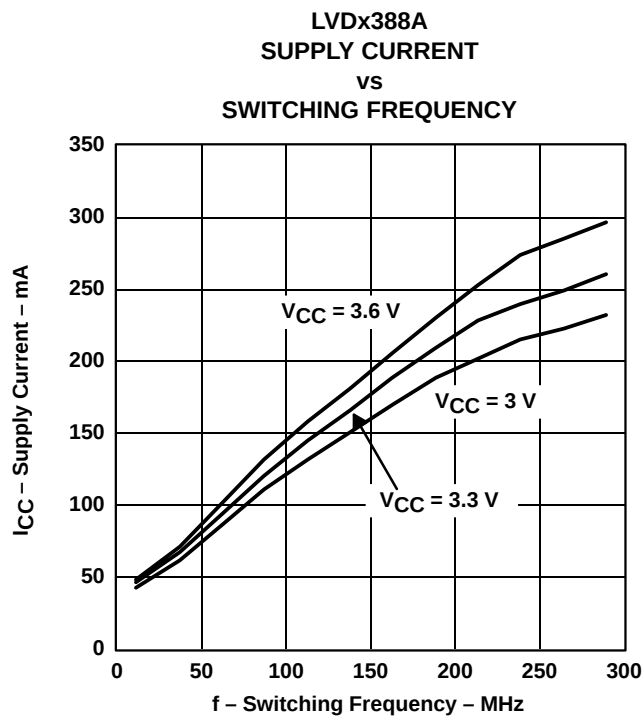


Figure 6

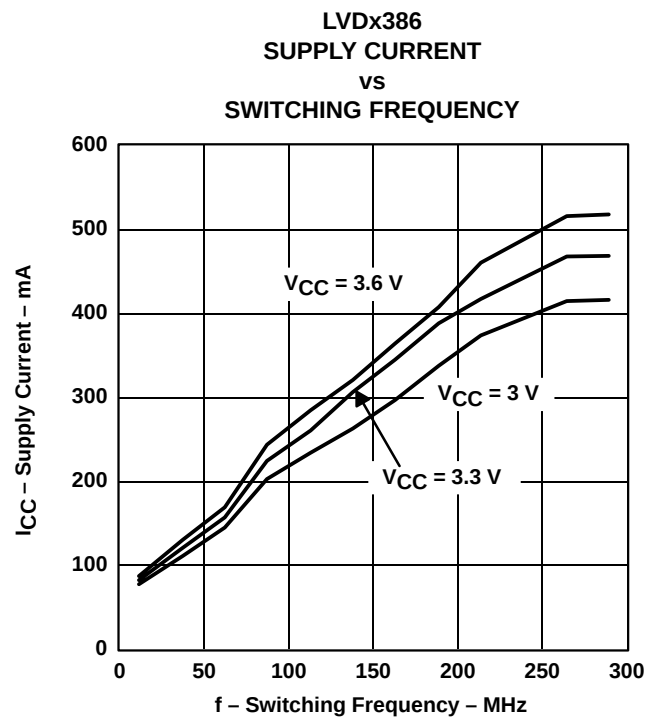


Figure 7

**SN65LVDS386/388A/390, SN65LVDT386/388A/390
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TYPICAL CHARACTERISTICS

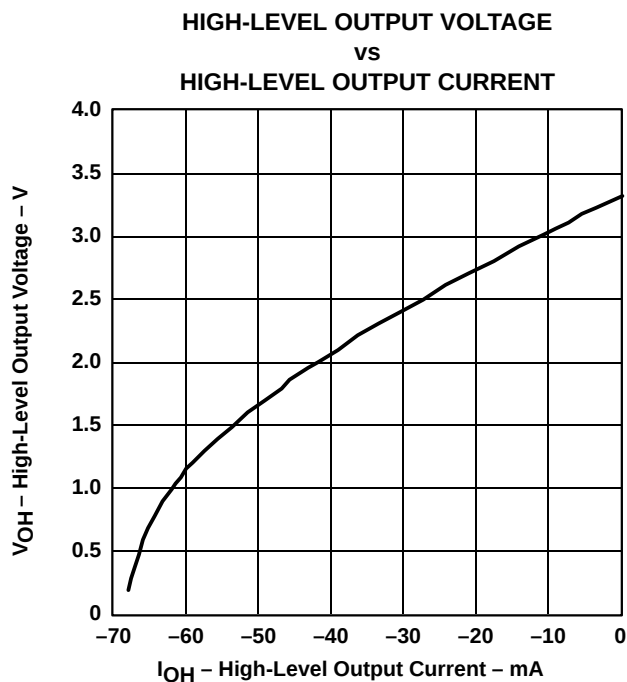


Figure 8

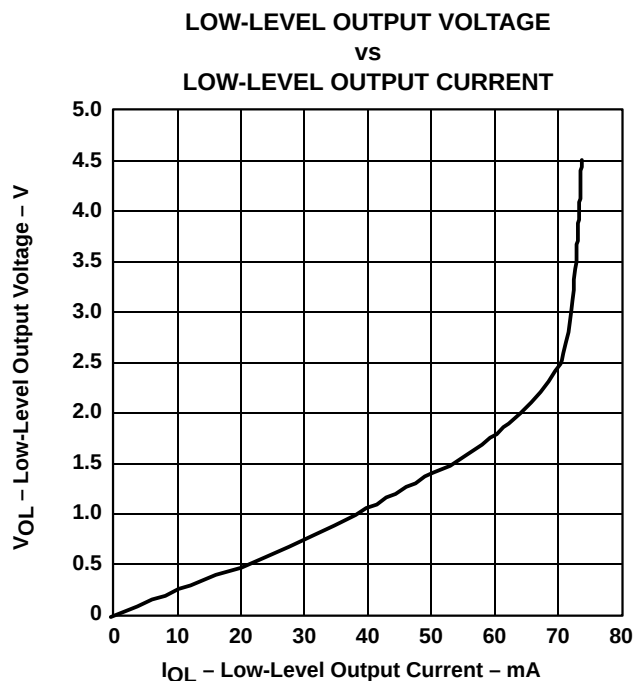


Figure 9

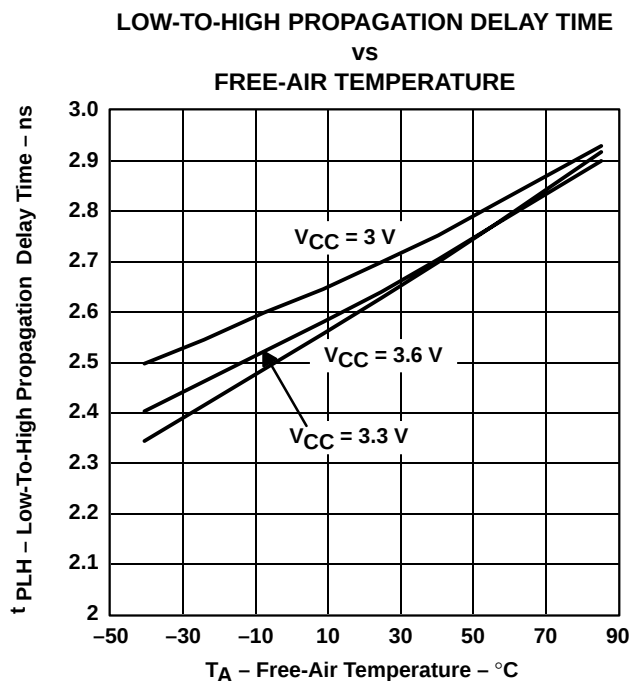


Figure 10

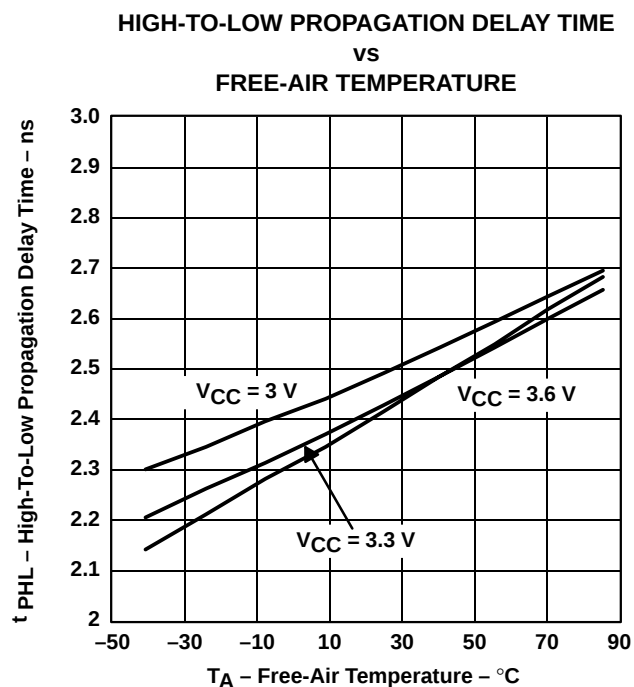


Figure 11

APPLICATION INFORMATION

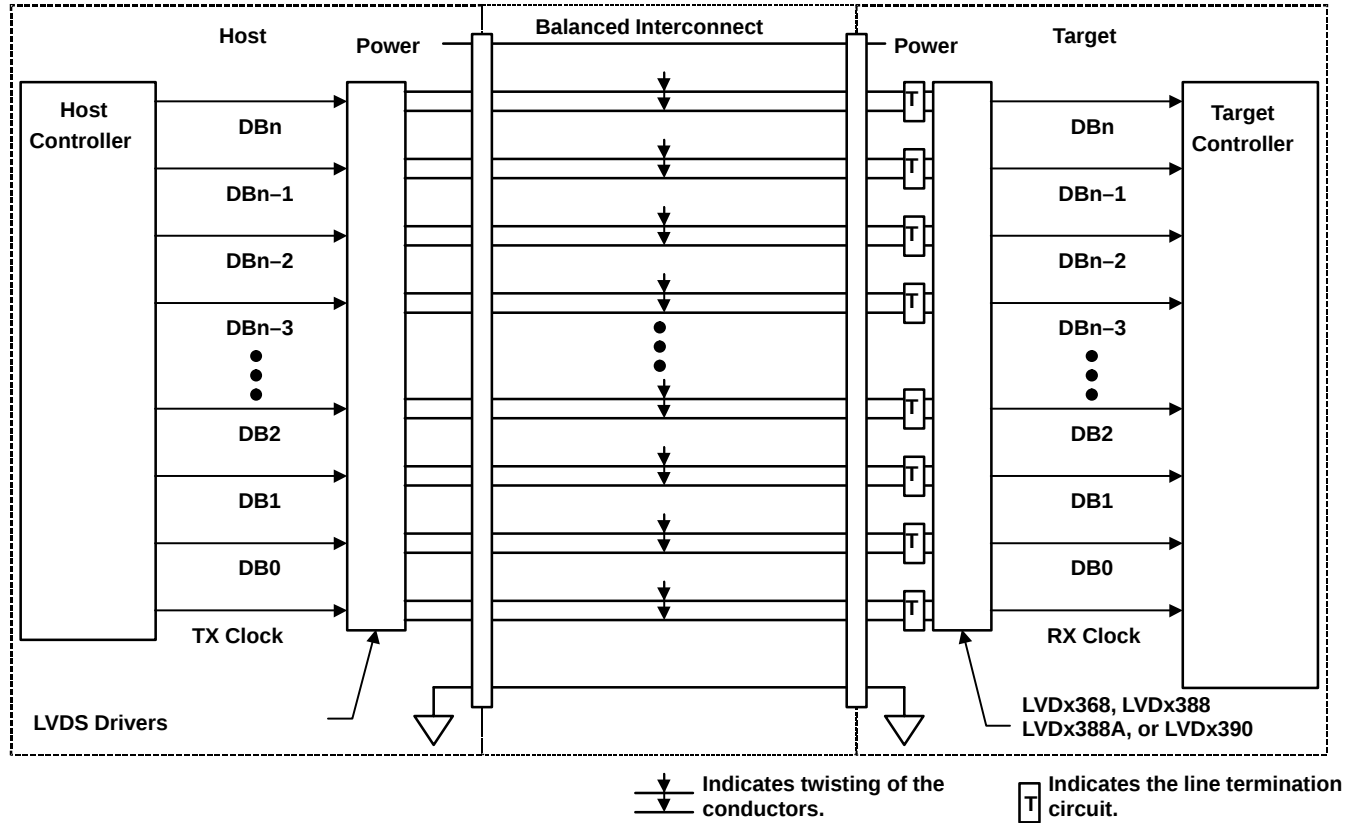


Figure 12. Typical Application Schematic

APPLICATION INFORMATION

analog and digital grounds/power supplies

Although it is not necessary to separate out the analog/digital supplies and grounds on the SN65LVDS/T388A and SN75LVDS/T388A, the pinout provides the user that option. To help minimize or perhaps eliminate switching noise being coupled between the two supplies, the user could lay out separate supply and ground planes for the designated pinout.

Most applications will probably have all grounds connected together and all power supplies connected together. This configuration was used while characterizing and setting the data sheet parameters.

fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between -100 mV and 100 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through $300\text{-k}\Omega$ resistors as shown in Figure 13. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

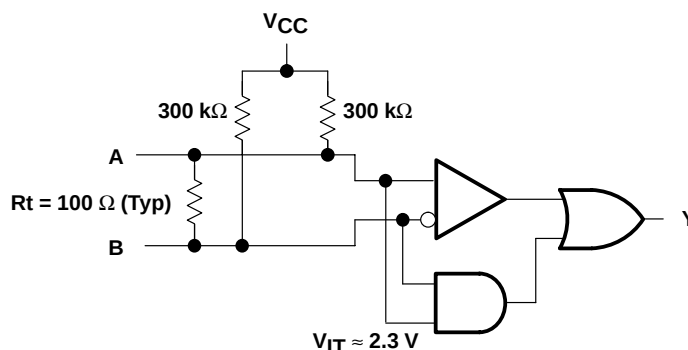


Figure 13. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, R_t , does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

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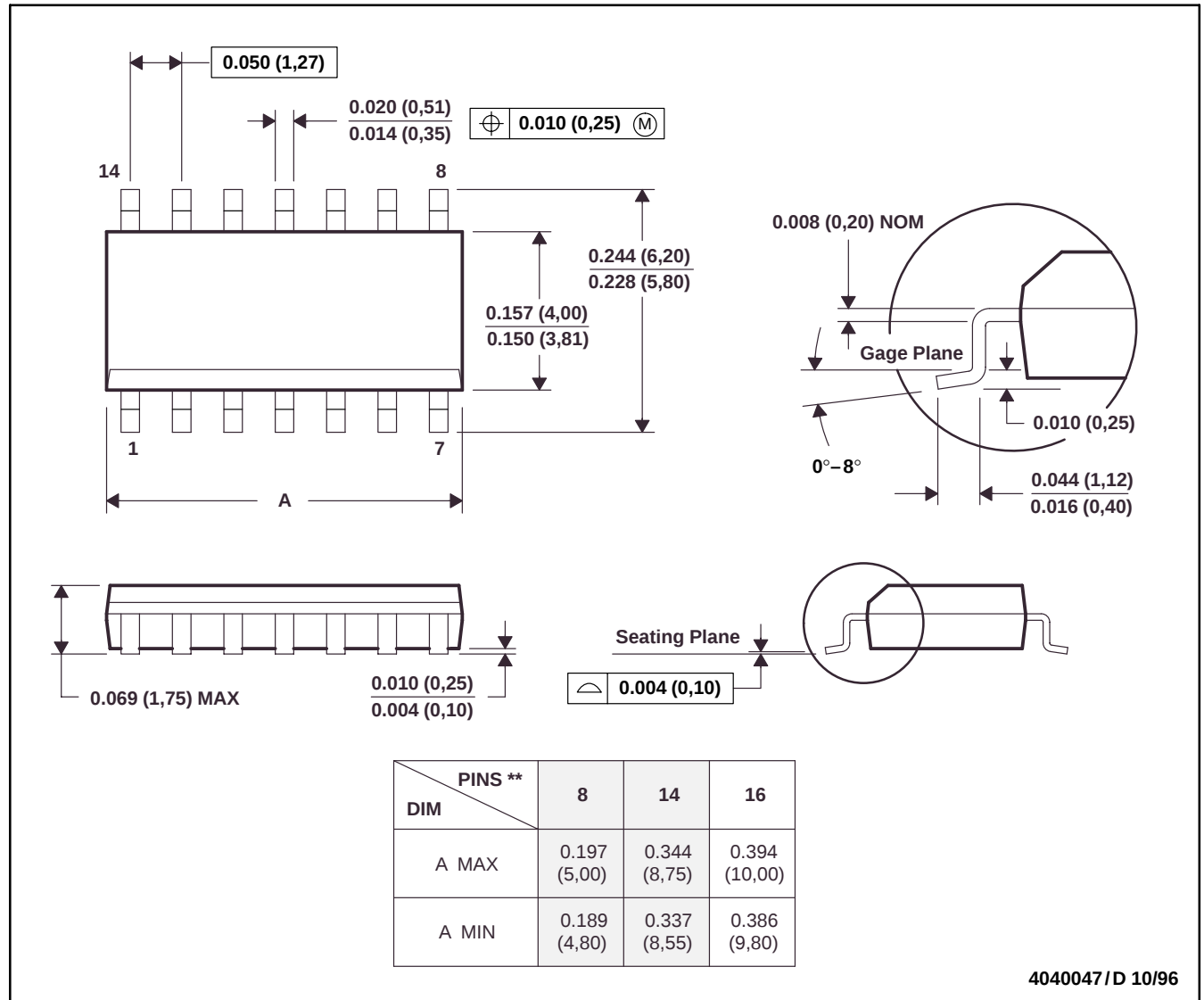
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MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

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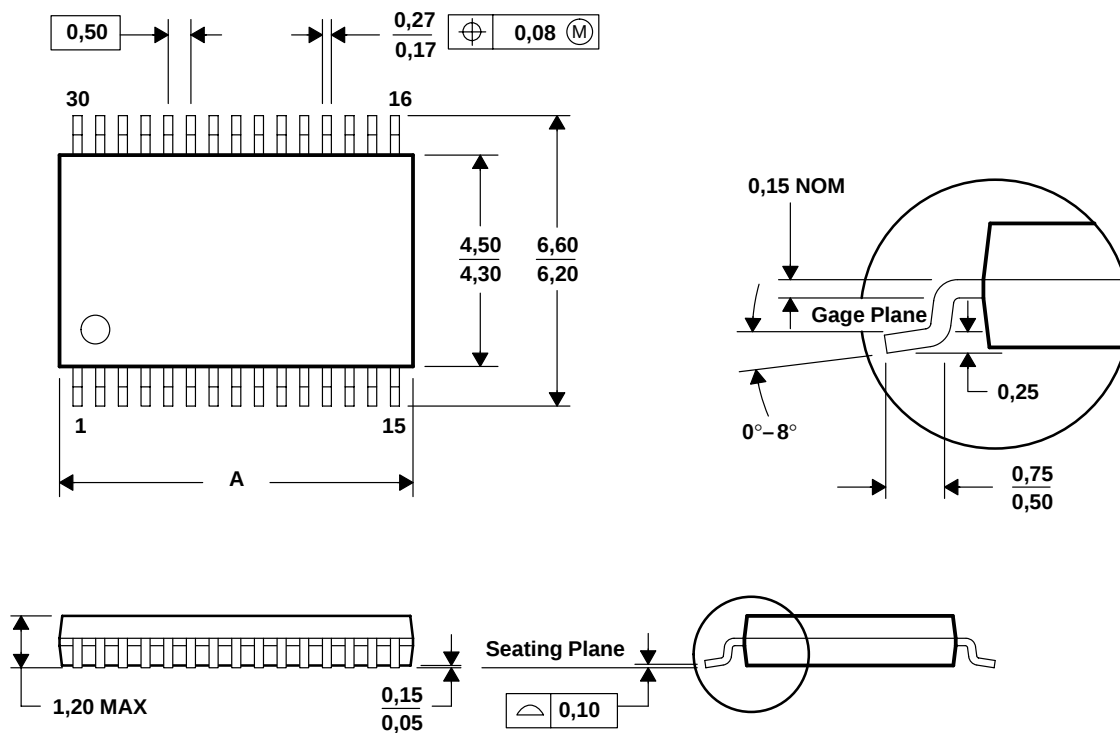
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MECHANICAL DATA

DBT (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

30 PINS SHOWN



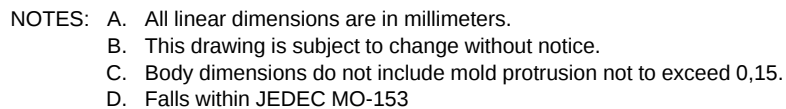
PINS **	28	30	38	44	50
DIM					
A MAX	7,90	7,90	9,80	11,10	12,60
A MIN	7,70	7,70	9,60	10,90	12,40

4073252/D 09/97

- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

SLLS394E – SEPTEMBER 1999 – REVISED SEPTEMBER 2002

48 PINS SHOWN



**SN65LVDS386/388A/390, SN65LVDT386/388A/390
SN75LVDS386/388A/390, SN75LVDT386/388A/390
HIGH-SPEED DIFFERENTIAL LINE RECEIVERS**

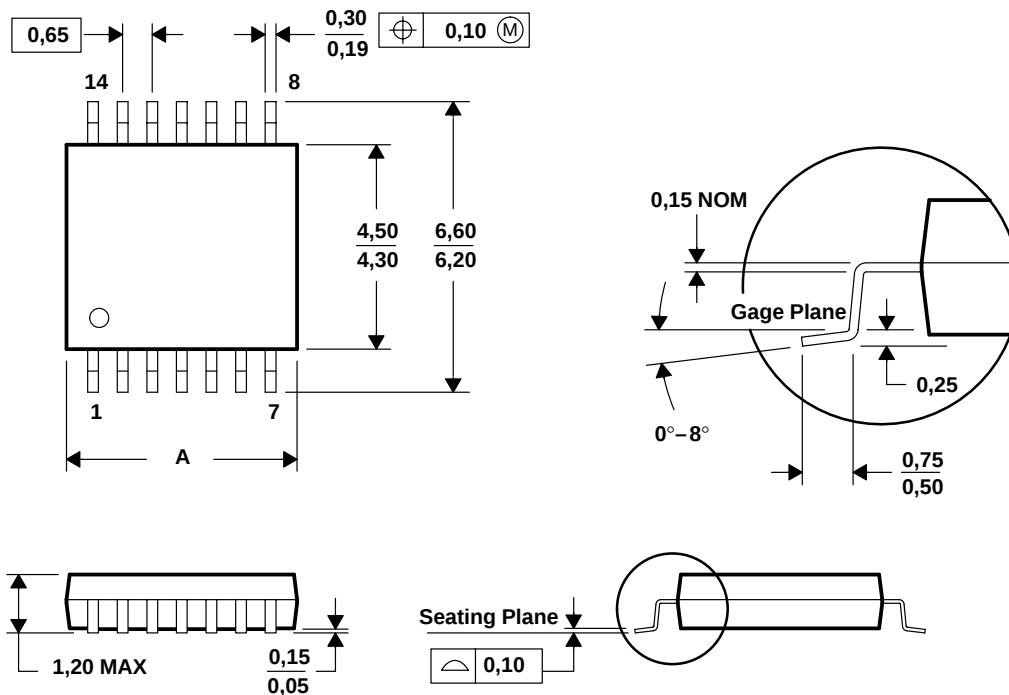
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MECHANICAL DATA

PW (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS **	8	14	16	20	24	28
DIM						
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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