

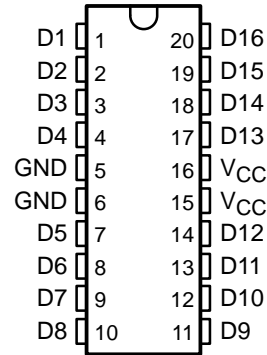
SN74ACT1073

16-BIT BUS-TERMINATION ARRAY WITH BUS-HOLD FUNCTION

SCAS193A – MARCH 1992 – REVISED NOVEMBER 2002

- Designed to Ensure Defined Voltage Levels on Floating Bus Lines in CMOS Systems
- 4.5-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Reduces Undershoot and Overshoot Caused By Line Reflections
- Repetitive Peak Forward Current . . . $I_{FRM} = 100$ mA
- Inputs Are TTL-Voltage Compatible
- Low Power Consumption (Like CMOS)
- Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

DW OR NS PACKAGE
(TOP VIEW)



description/ordering information

This device is designed to terminate bus lines in CMOS systems. The integrated low-impedance diodes clamp the voltage of undershoots and overshoots caused by line reflections and ensure signal integrity. The device also contains a bus-hold function that consists of a CMOS-buffer stage with a high-resistance feedback path between its output and its input. The SN74ACT1073 prevents bus lines from floating without using pullup or pulldown resistors.

The high-impedance inputs of these internal buffers are connected to the input terminals of the device. The feedback path on each internal buffer stage keeps a bus line tied to the bus holder at the last valid logic state generated by an active driver before the bus switches to the high-impedance state.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74ACT1073DW	ACT1073
		Tape and reel	SN74ACT1073DWR	
	SOP – NS	Tape and reel	SN74ACT1073NSR	ACT1073

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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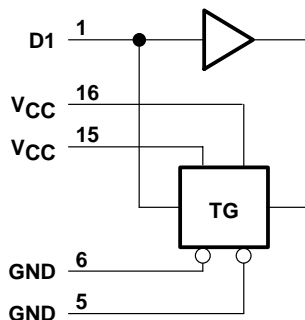
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logic diagram, one of sixteen channels (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Continuous input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Positive-peak input clamp current, I_{IK} ($V_I > V_{CC}$) ($t_w < 1 \mu s$, duty cycle $< 20\%$)	100 mA
Negative-peak input clamp current, I_{IK} ($V_I < 0$) ($t_w < 1 \mu s$, duty cycle $< 20\%$)	-100 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	58°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTE 1: The input negative-voltage rating may be exceeded if the input clamp-current rating is observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.5	5.5	V
V_{IH} High-level input voltage	2.5		V
V_{IL} Low-level input voltage		0.8	V
V_I Input voltage	0	V_{CC}	V
T_A Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SCAS193A – MARCH 1992 – REVISED NOVEMBER 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			MIN	MAX	UNIT
		MIN	TYP†	MAX			
I _{IL}	V _{CC} = 4.5 to 5.5 V, V _I = 0.8 V	0.15	0.3	0.9	0.1	1	mA
I _{IH}	V _{CC} = 4.5 to 5.5 V, V _I = 2.5 V	-0.2	-0.5	-1.4	-0.15	-1.5	mA
V _{IKL}	I _{IN} = -18 mA			-1.5	-1.5		V
V _{IKH}	I _{IN} = 18 mA			V _{CC} +2	V _{CC} +2		V
I _{CC} ‡	V _{CC} = 5.5 V, Inputs open			4	40		μA
ΔI _{CC} §	One input at 3.4 V, Other inputs at V _{CC} or GND			0.9	1		mA
C _i	V _I = V _{CC} or GND		3				pF

† All typical values are at V_{CC} = 5 V.

‡ Inputs may be set high or low prior to the I_{CC} measurement.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

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TYPICAL CHARACTERISTICS

**FORWARD CURRENT
 vs
 INPUT VOLTAGE
 (UPPER CLAMPING DIODE)**

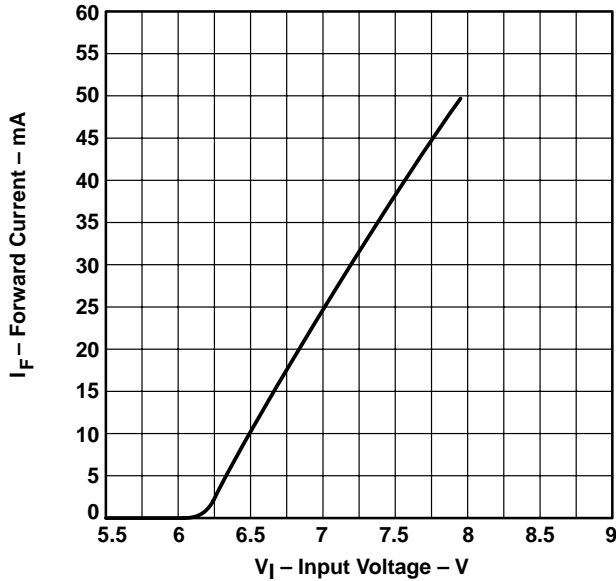


Figure 1

**FORWARD CURRENT
 vs
 INPUT VOLTAGE
 (LOWER CLAMPING DIODE)**

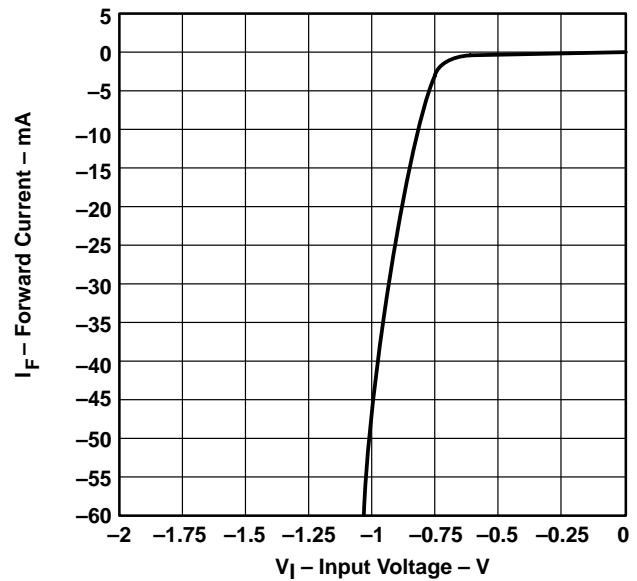


Figure 2

**INPUT CURRENT
 vs
 INPUT VOLTAGE**

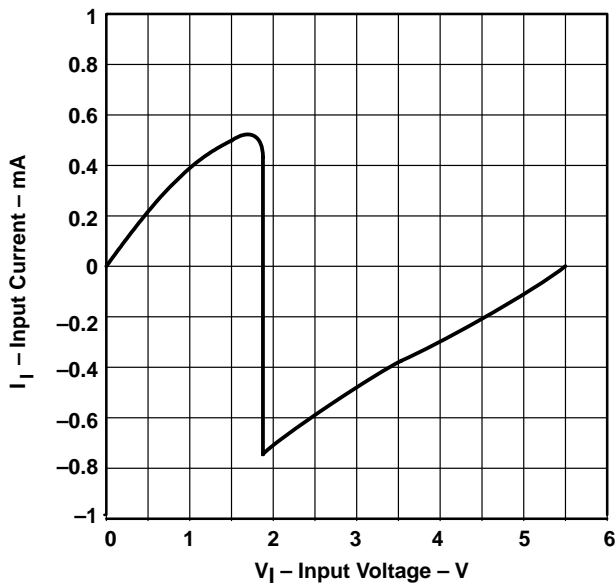


Figure 3

**SUPPLY CURRENT
 vs
 INPUT VOLTAGE**

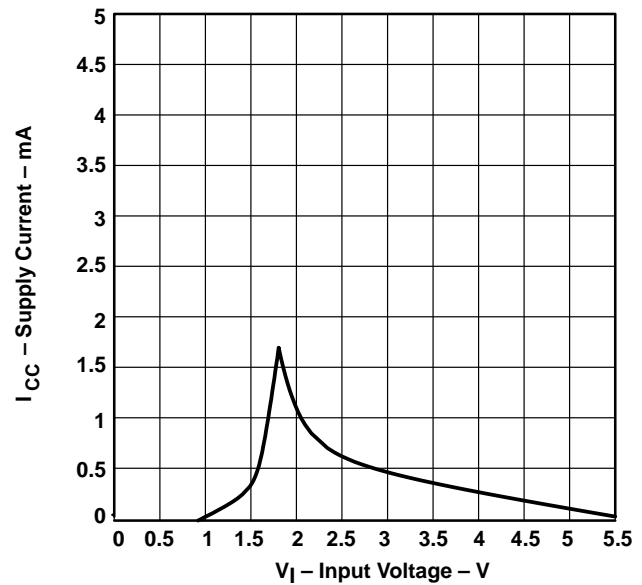


Figure 4



APPLICATION INFORMATION

The SN74ACT1073 terminates the output of a driving device and holds the input of the driven device at the logic level of the driver output prior to establishment of the high-impedance state on that output (see Figure 5).

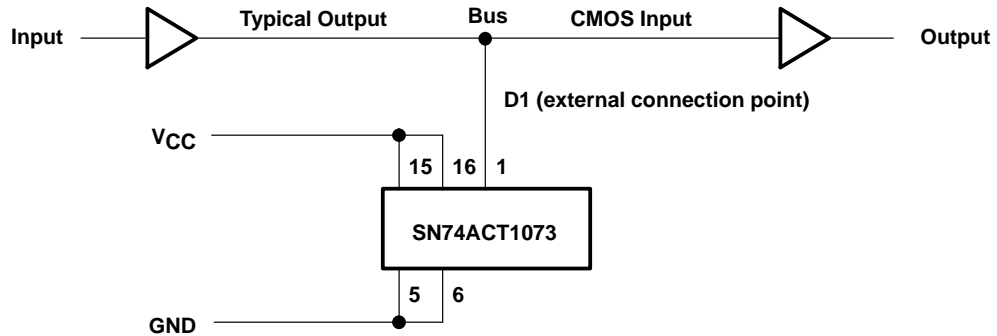


Figure 5. Bus-Hold Application

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ACT1073DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ACT1073DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ACT1073NSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

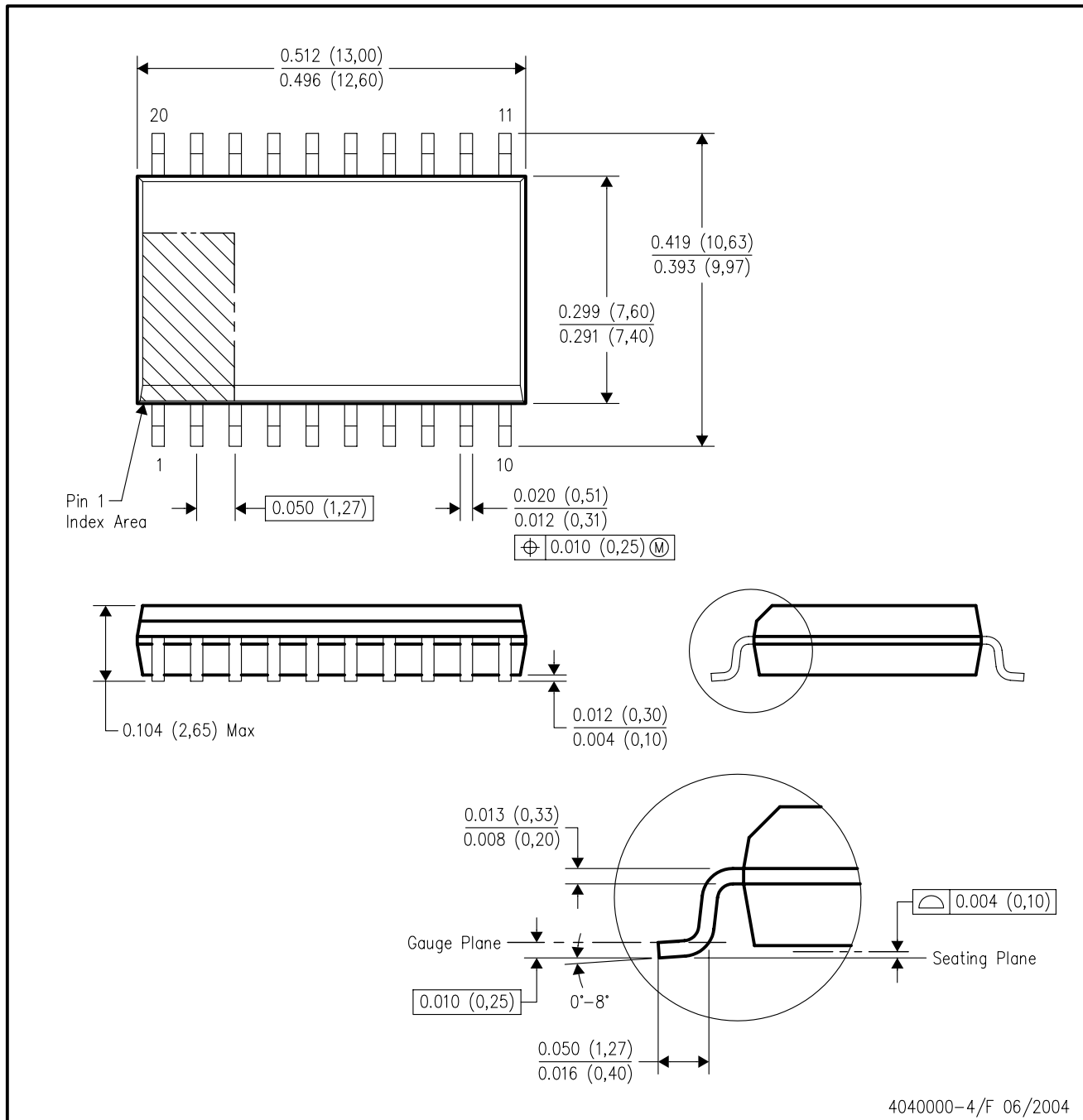
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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