

SN54ACT1284, SN74ACT1284 7-BIT BUS INTERFACES WITH 3-STATE OUTPUTS

SCAS459D – NOVEMBER 1994 – REVISED OCTOBER 2003

- 4.5-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 20 ns at 5 V
- 3-State Outputs Directly Drive Bus Lines
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
- Designed for the IEEE 1284-I (Level-1 Type) and IEEE 1284-II (Level-2 Type) Electrical Specifications

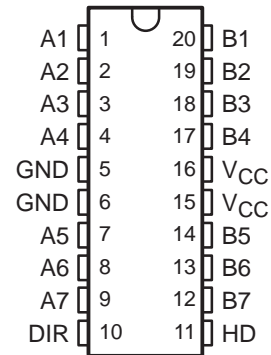
description/ordering information

The 'ACT1284 devices are designed for asynchronous two-way communication between data buses. The control function minimizes external timing requirements.

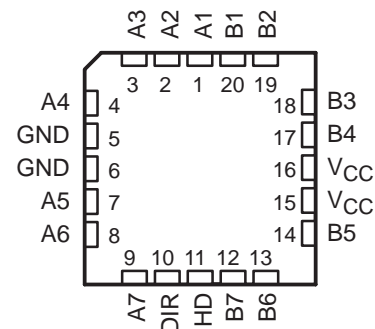
The devices allow data transmission in either the A-to-B or the B-to-A direction for bits 1, 2, 3, and 4, depending on the logic level at the direction-control (DIR) input. Bits 5, 6, and 7, however, always transmit in the A-to-B direction.

The output drive for each mode is determined by the high-drive (HD) control pin. When HD is high, the high drive is delivered by the totem-pole configuration, and when HD is low, the outputs are open drain. This meets the drive requirements as specified in the IEEE 1284-I (level-1 type) and the IEEE 1284-II (level-2 type) parallel peripheral-interface specification.

SN54ACT1284 . . . J OR W PACKAGE
SN74ACT1284 . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54ACT1284 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| 0°C to 70°C | SOIC – DW | Tube | SN74ACT1284DW | ACT1284 |
| | | Tape and reel | SN74ACT1284DWR | |
| | SOP – NS | Tape and reel | SN74ACT1284NSR | ACT1284 |
| | SSOP – DB | Tape and reel | SN74ACT1284DBR | AU284 |
| –55°C to 125°C | TSSOP – PW | Tube | SN74ACT1284PW | AU284 |
| | | Tape and reel | SN74ACT1284PWR | |
| | CDIP – J | Tube | SNJ54ACT1284J | SNJ54ACT1284J |
| | CFP – W | Tube | SNJ54ACT1284W | SNJ54ACT1284W |
| | LCCC – FK | Tube | SNJ54ACT1284FK | SNJ54ACT1284FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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SN54ACT1284, SN74ACT1284

7-BIT BUS INTERFACES

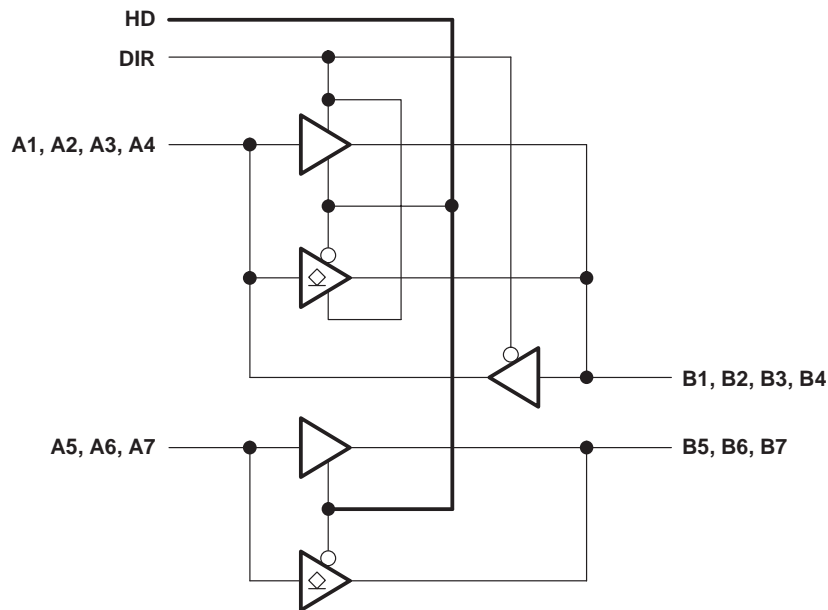
WITH 3-STATE OUTPUTS

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FUNCTION TABLE

| INPUTS | | OUTPUT | MODE |
|--------|----|------------|--|
| DIR | HD | | |
| L | L | Open drain | A to B: Bits 5, 6, 7 |
| | | Totem pole | B to A: Bits 1, 2, 3, 4 |
| L | H | Totem pole | B to A: Bits 1, 2, 3, 4 and A to B: Bits 5, 6, 7 |
| H | L | Open drain | A to B: Bits 1, 2, 3, 4, 5, 6, 7 |
| H | H | Totem pole | A to B: Bits 1, 2, 3, 4, 5, 6, 7 |

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| B-port input and output voltage range, V_I and V_O (see Notes 1 and 2) | –2 V to 7 V |
| A-port input and output voltage range, V_I and V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±50 mA |
| Continuous current through V_{CC} or GND | ±200 mA |
| Package thermal impedance, θ_{JA} (see Note 3): DB package | 70°C/W |
| DW package | 58°C/W |
| NS package | 60°C/W |
| PW package | 83°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The ac input voltage pulse duration is limited to 20 ns if the input voltage goes more negative than –0.5 V.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

| | | | SN54ACT1284 | | SN74ACT1284 | | UNIT |
|----------|---------------------------|-----------------|-------------|----------|-------------|----------|------|
| | | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | | 4.7 | 5.5 | 4.7 | 5.5 | V |
| V_{IH} | High-level input voltage | | 2 | | 2 | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | | 0.8 | V |
| V_I | Input voltage | | 0 | V_{CC} | 0 | V_{CC} | V |
| V_O | Open-drain output voltage | HD low | 0 | 5.5 | 0 | 5.5 | V |
| | | B port, HD high | | –14 | | –14 | mA |
| I_{OH} | High-level output current | A port | | –4 | | –4 | |
| | | B port | | 14 | | 14 | mA |
| I_{OL} | Low-level output current | A port | | 4 | | 4 | |
| | | | | –55 | 125 | 0 | 70 |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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7-BIT BUS INTERFACES

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} † | SN54ACT1284 | | | SN74ACT1284 | | | UNIT |
|------------------|------------------|---|-------------------|----------------------|-----|-----|----------------------|-----|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{hys} | Input hysteresis | V _{IT+} – V _{IT-} for all inputs | 5 V | 0.4 | | | 0.4 | | | V |
| | | | 4.7 V | 0.2 | | | 0.2 | | | |
| V _{OH} | B port | I _{OH} = –14 mA | 4.7 V | 2.4 | | | 2.4 | | | V |
| | A port | I _{OH} = –50 μA | MIN to MAX | V _{CC} –0.2 | | | V _{CC} –0.2 | | | |
| | | I _{OH} = –4 mA | 4.7 V | 3.7 | | | 3.7 | | | |
| V _{OL} | B port | I _{OL} = 14 mA | 4.7 V | | | | 0.4 | | | V |
| | A port | I _{OL} = 50 μA | 4.7 V | | | | 0.2 | | | |
| | | I _{OL} = 4 mA | | | | | 0.4 | | | |
| I _I | | V _I = V _{CC} or GND | 5.5 V | | | | ±1 | | | μA |
| I _{OZ} | A or B ports‡ | V _O = V _{CC} or GND | 5.5 V | | | | ±20 | | | μA |
| I _{off} | B port | V _I or V _O ≤ 7 V | 0 V | | | | ±100 | | | μA |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | | 1.5 | | | mA |
| C _i | Control inputs | V _I = V _{CC} or GND | 5 V | 4 | | | 4 | | | pF |
| C _{io} | A or B ports | V _O = V _{CC} or GND | 5 V | 12 | | | 12 | | | pF |
| Z _O | B port | I _{OH} = –20 mA, I _{OH} = –50 mA | 5 V | 8 | 30 | | 8 | 30 | | Ω |

† For I/O ports, the parameter I_{OZ} includes the input leakage current I_I.

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

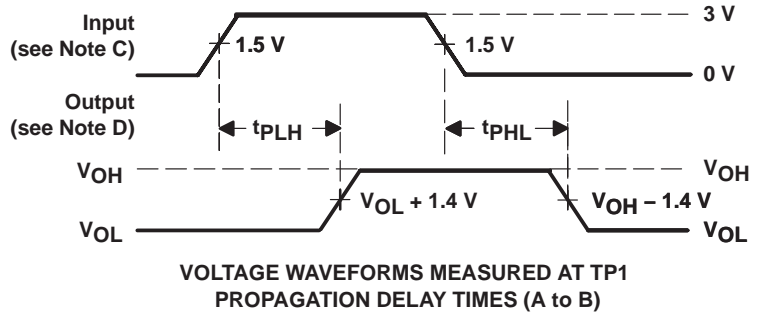
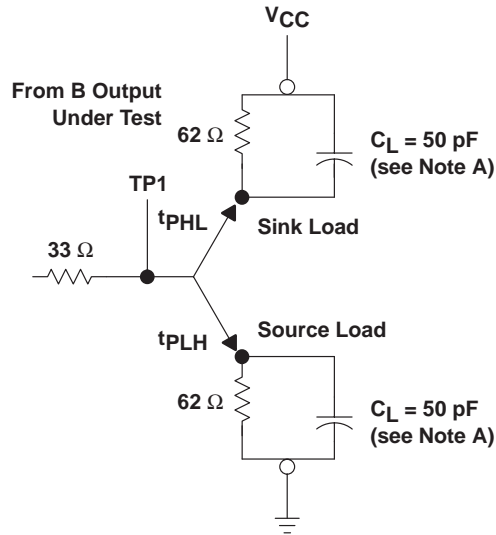
| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | SN54ACT1284 | | SN74ACT1284 | | UNIT |
|---------------------------------|------------|--------------|-------------|-------------|-----|-------------|-----|------|
| | | | | MIN | MAX | MIN | MAX | |
| t _{PLH} | Totem pole | A or B | B or A | 1 | 20 | 1 | 20 | ns |
| t _{PHL} | | | | 1 | 20 | 1 | 20 | |
| SR | Totem pole | B output | | 0.05 | 0.4 | 0.05 | 0.4 | V/ns |
| t _{pd(EN)} | Totem pole | HD | B | 1 | 20 | 1 | 20 | ns |
| t _{pd(DIS)} | | | | 1 | 20 | 1 | 20 | |
| t _r , t _f | Open drain | A | B | 120 | | 120 | | ns |

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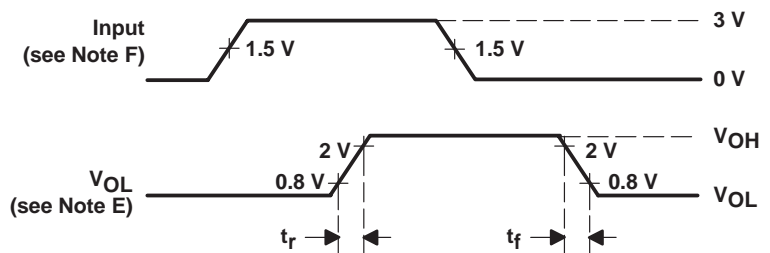
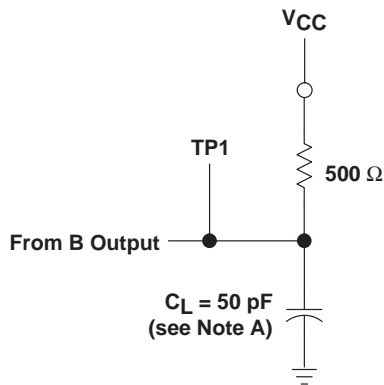


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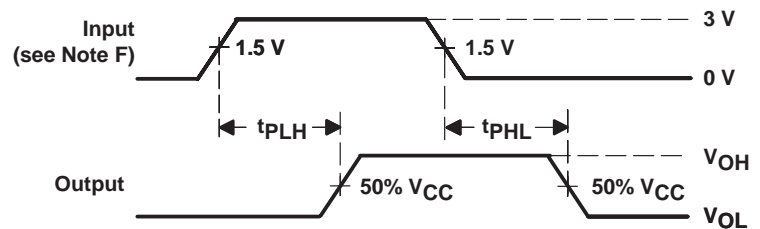
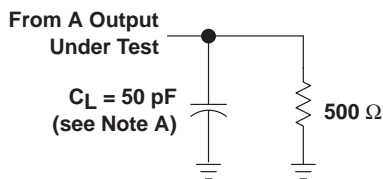
PARAMETER MEASUREMENT INFORMATION



A-TO-B LOAD (totem pole)



A-TO-B LOAD (open drain)



B-TO-A LOAD (totem pole)

- NOTES: A. C_L includes probe and jig capacitance.
 B. The outputs are measured one at a time with one transition per measurement.
 C. Input rise and fall times are 3 ns, $150 \text{ ns} < \text{pulse duration} < 10 \text{ } \mu\text{s}$ for both low-to-high and high-to-low transitions.
 D. Slew rate is defined as 10% and 90% of the transition times.
 E. Rise and fall times, open drain, are $< 120 \text{ ns}$.
 F. Input rise and fall times are 3 ns.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--|
| SN74ACT1284DBLE | OBSOLETE | SSOP | DB | 20 | | None | Call TI | Call TI |
| SN74ACT1284DBR | ACTIVE | SSOP | DB | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74ACT1284DW | ACTIVE | SOIC | DW | 20 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74ACT1284DWR | ACTIVE | SOIC | DW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74ACT1284NSR | ACTIVE | SO | NS | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74ACT1284PW | ACTIVE | TSSOP | PW | 20 | 70 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74ACT1284PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
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 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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