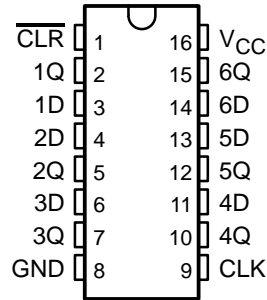


SN54AHC174, SN74AHC174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

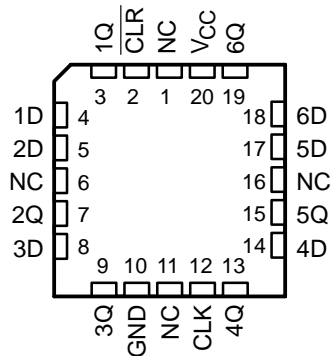
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- Operating Range 2-V to 5.5-V V_{CC}
- Contain Six Flip-Flops With Single-Rail Outputs
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54AHC174 . . . J OR W PACKAGE
SN74AHC174 . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC174 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHC174 devices are positive-edge-triggered D-type flip-flops with a direct clear (CLR) input and are designed for 2-V to 5.5-V V_{CC} operation.

Information at the data (D) inputs that meets the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHC174N	SN74AHC174N
	SOIC – D	Tube	SN74AHC174D	AHC174
		Tape and reel	SN74AHC174DR	
	SOP – NS	Tube	SN74AHC174NSR	AHC174
	SSOP – DB	Tape and reel	SN74AHC174DBR	HA174
	TSSOP – PW	Tape and reel	SN74AHC174PWR	HA174
	TVSOP – DGV	Tape and reel	SN74AHC174DGVR	HA174
–55°C to 125°C	CDIP – J	Tube	SNJ54AHC174J	SNJ54AHC174J
	CFP – W	Tube	SNJ54AHC174W	SNJ54AHC174W
	LCCC – FK	Tube	SNJ54AHC174FK	SNJ54AHC174FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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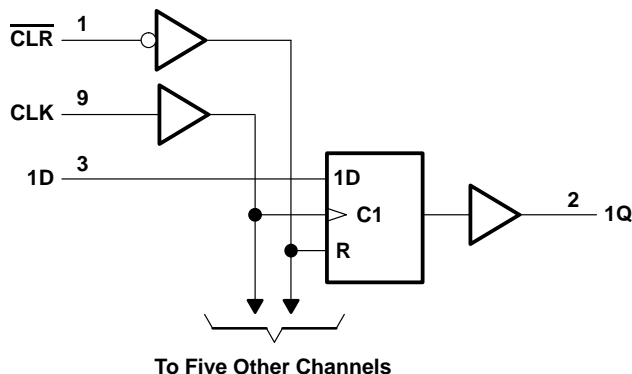
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FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	73°C/W
DB package	82°C/W
DGV package	120°C/W
N package	67°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54AHC174, SN74AHC174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

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recommended operating conditions (see Note 3)

		SN54AHC174		SN74AHC174		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5		V
		V _{CC} = 3 V		2.1		
		V _{CC} = 5.5 V		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		V
		V _{CC} = 3 V		0.9		
		V _{CC} = 5.5 V		1.65		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50		μA
		V _{CC} = 3.3 V ± 0.3 V		-4		
		V _{CC} = 5 V ± 0.5 V		-8		
I _{OL}	Low-level output current	V _{CC} = 2 V		50		μA
		V _{CC} = 3.3 V ± 0.3 V		4		
		V _{CC} = 5 V ± 0.5 V		8		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100		ns/V
		V _{CC} = 5 V ± 0.5 V		20		
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC174		SN74AHC174		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V				0.1		0.1	V	
		3 V				0.1		0.1		
		4.5 V				0.1		0.1		
	I _{OL} = 4 mA	3 V				0.36		0.5		0.44
	I _{OL} = 8 mA	4.5 V				0.36		0.5		0.44
I _I	V _I = 5.5 V or GND	0 V to 5.5 V				± 0.1		± 1*	± 1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V				4		40	40	μA
C _i	V _I = V _{CC} or GND	5 V		1.7	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

		$T_A = 25^\circ\text{C}$		SN54AHC174		SN74AHC174		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$ low	5	5	5	5	ns	
		CLK high or low	5	5	5			
t_{su}	Setup time before CLK \uparrow	Data	5	6	6	ns		
		$\overline{\text{CLR}}$ inactive	3	3	3			
t_h	Hold time, data after CLK \uparrow	0	0	0	0	ns		

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

		$T_A = 25^\circ\text{C}$		SN54AHC174		SN74AHC174		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$ low	5	5	5	5	ns	
		CLK high or low	5	5	5			
t_{su}	Setup time before CLK \uparrow	Data	4.5	4.5	4.5	ns		
		$\overline{\text{CLR}}$ inactive	2.5	2.5	2.5			
t_h	Hold time, data after CLK \uparrow	0.5	0.5	0.5	0.5	ns		

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC174		SN74AHC174		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	95*	170*		80*		80	MHz	
			$C_L = 50\text{ pF}$	55	130		50		50		
t_{PHL}	$\overline{\text{CLR}}$	Any Q	$C_L = 15\text{ pF}$	4.5*	11.4*		1*	13.5*	1	13.5	ns
t_{PLH}	CLK	Any Q	$C_L = 15\text{ pF}$	5.8*	11*		1*	13*	1	13	ns
t_{PHL}				5.8*	11*		1*	13*	1	13	
t_{PHL}	$\overline{\text{CLR}}$	Any Q	$C_L = 50\text{ pF}$	6	14.9		1	17	1	17	ns
t_{PLH}	CLK	Any Q	$C_L = 50\text{ pF}$	7.5	14.5		1	16.5	1	16.5	ns
t_{PHL}				7.5	14.5		1	16.5	1	16.5	
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1.5**				1.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC174		SN74AHC174		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF	130*	240*		110*		110		MHz
			C _L = 50 pF	90	180		80		80		
t _{PHL}	$\overline{\text{CLR}}$	Any Q	C _L = 15 pF		3*	7.6*	1*	9*	1	9	ns
t _{PLH}	CLK	Any Q	C _L = 15 pF		4.1*	7.2*	1*	8.5*	1	8.5	ns
t _{PHL}					4.1*	7.2*	1*	8.5*	1	8.5	
t _{PHL}	$\overline{\text{CLR}}$	Any Q	C _L = 50 pF		4.2	9.6	1	11	1	11	ns
t _{PLH}	CLK	Any Q	C _L = 50 pF		5.5	9.2	1	10.5	1	10.5	ns
t _{PHL}					5.5	9.2	1	10.5	1	10.5	
t _{sk(o)}			C _L = 50 pF			1**				1	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

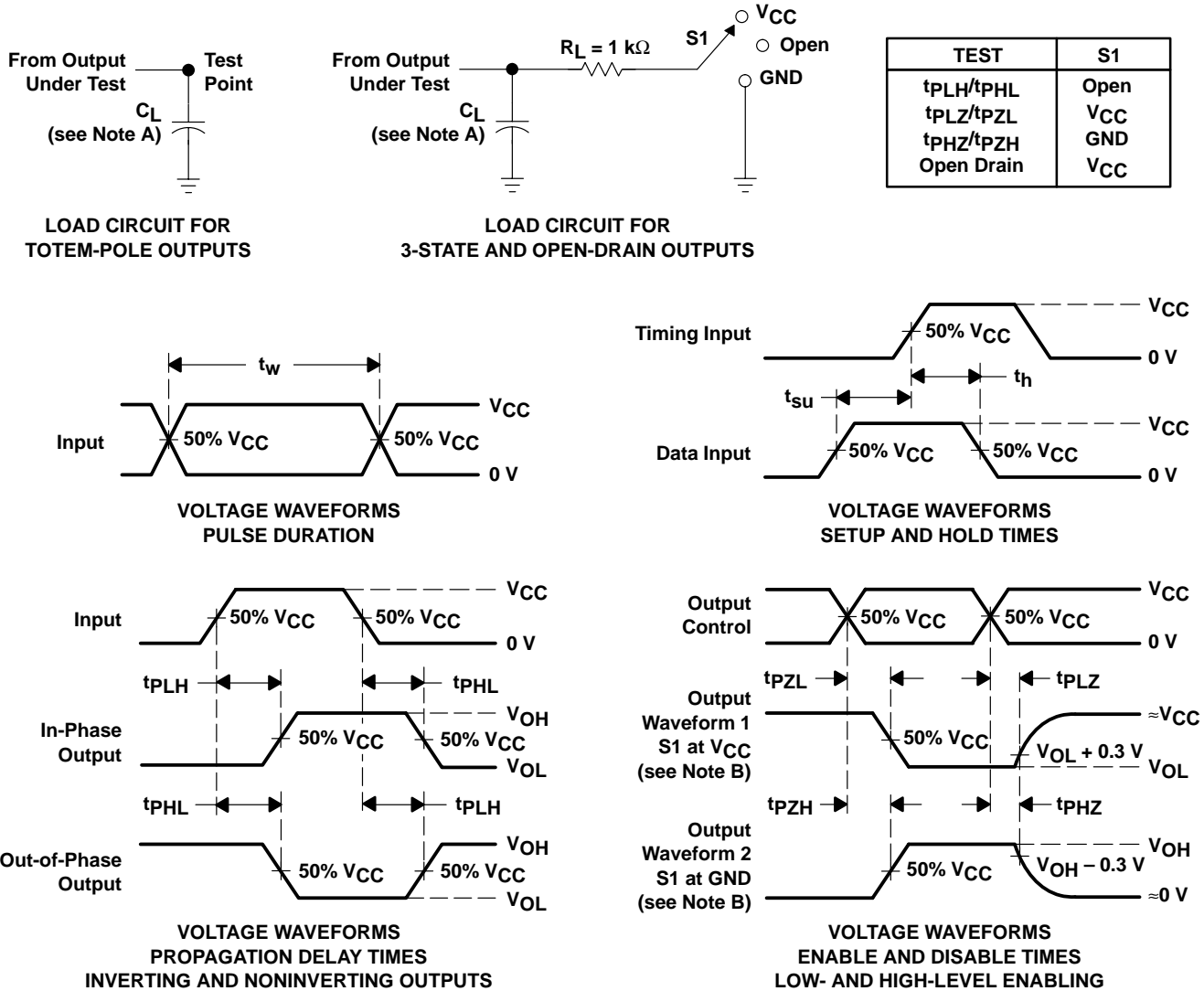
operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load, f = 1 MHz	15.2	pF

SN54AHC174, SN74AHC174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AHC174D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC174DBR	ACTIVE	SSOP	DB	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC174DGVR	ACTIVE	TVSOP	DGV	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHC174DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC174N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74AHC174NSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC174PWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

4040065 /E 12/01

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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