

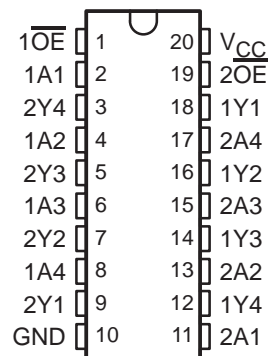
SN74AHCT240-Q1 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCLS582A – APRIL 2004 – REVISED JUNE 2004

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

† Contact factory for details. Q100 qualification data available on request.

PW PACKAGE
(TOP VIEW)



description/ordering information

This octal buffer/driver is designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74AHCT240 device is organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – PW	Tape and reel	SN74AHCT240IPWRQ1	AHCT240I

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 4-bit buffer/driver)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	L
L	L	H
H	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

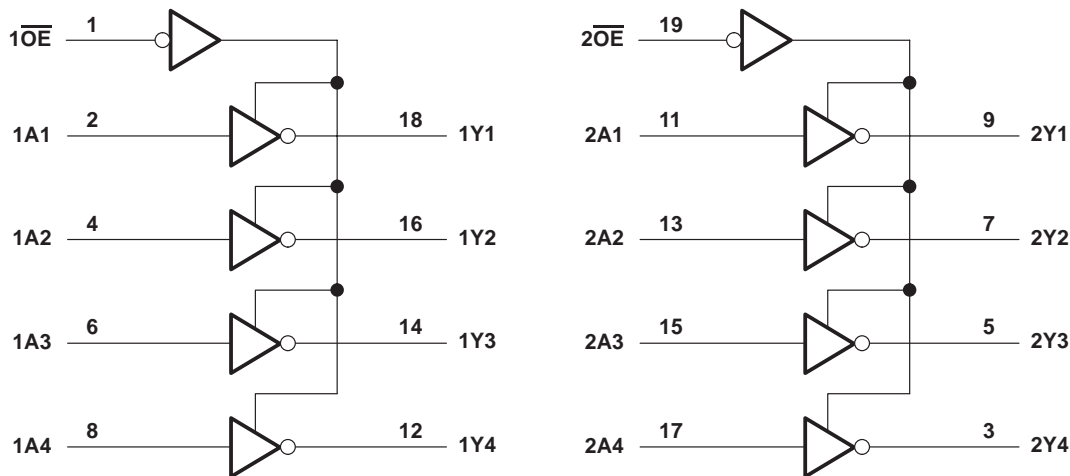
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SCLS582A – APRIL 2004 – REVISED JUNE 2004

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±75 mA
Package thermal impedance, θ_{JA} (see Note 2)	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4	V	
	I _{OH} = -8 mA		3.94			3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1	0.1	V	
	I _{OL} = 8 mA				0.36	0.44		
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25	±2.5	μA	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1	±1	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4	40	μA	
ΔI _{CC} [†]	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35	1.5	mA	
C _i	V _I = V _{CC} or GND	5 V		2.5	10	10	pF	
C _o	V _O = V _{CC} or GND	5 V		3			pF	

[†] This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{PLH}	A	Y	C _L = 15 pF	5.4	7.4		1	8.5	ns
t _{PHL}				5.4	7.4		1	8.5	
t _{PZH}	\overline{OE}	Y	C _L = 15 pF	7.7	10.4		1	12	ns
t _{PZL}				7.7	10.4		1	12	
t _{PHZ}	\overline{OE}	Y	C _L = 15 pF	8.3	10.4		1	12	ns
t _{PLZ}				8.3	10.4		1	12	
t _{PLH}	A	Y	C _L = 50 pF	5.9	8.4		1	9.5	ns
t _{PHL}				5.9	8.4		1	9.5	
t _{PZH}	\overline{OE}	Y	C _L = 50 pF	8.2	11.4		1	13	ns
t _{PZL}				8.2	11.4		1	13	
t _{PHZ}	\overline{OE}	Y	C _L = 50 pF	8.8	11.4		1	13	ns
t _{PLZ}				8.8	11.4		1	13	
t _{sk(o)}			C _L = 50 pF			1	1	ns	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER	MIN	TYP	MAX	UNIT
V _{OH(V)} Quiet output, minimum dynamic V _{OH}		4.1		V
V _{IH(D)} High-level dynamic input voltage	2			V
V _{IL(D)} Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

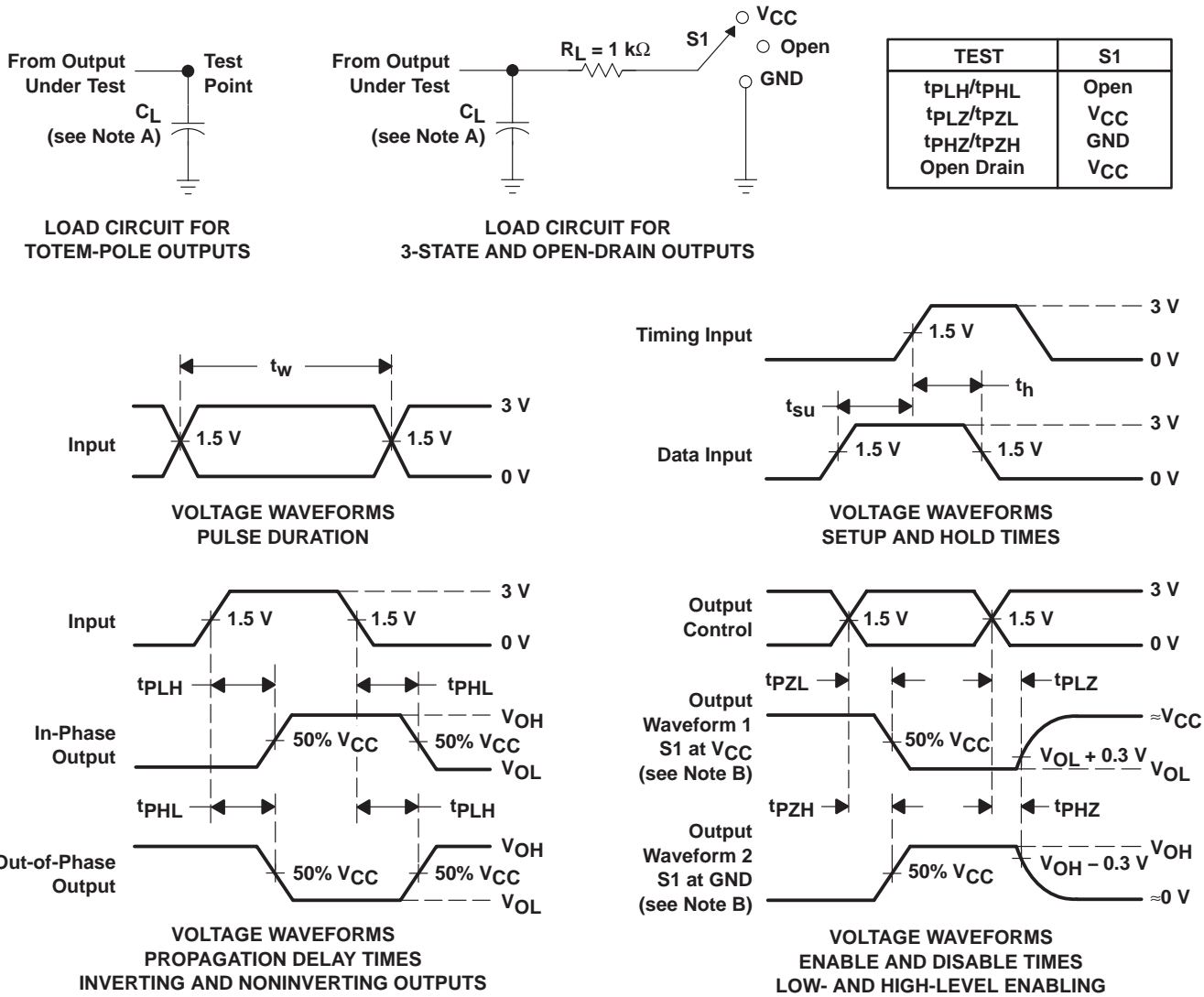
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load, f = 1 MHz	10	pF

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SCLS582A – APRIL 2004 – REVISED JUNE 2004

PARAMETER MEASUREMENT INFORMATION



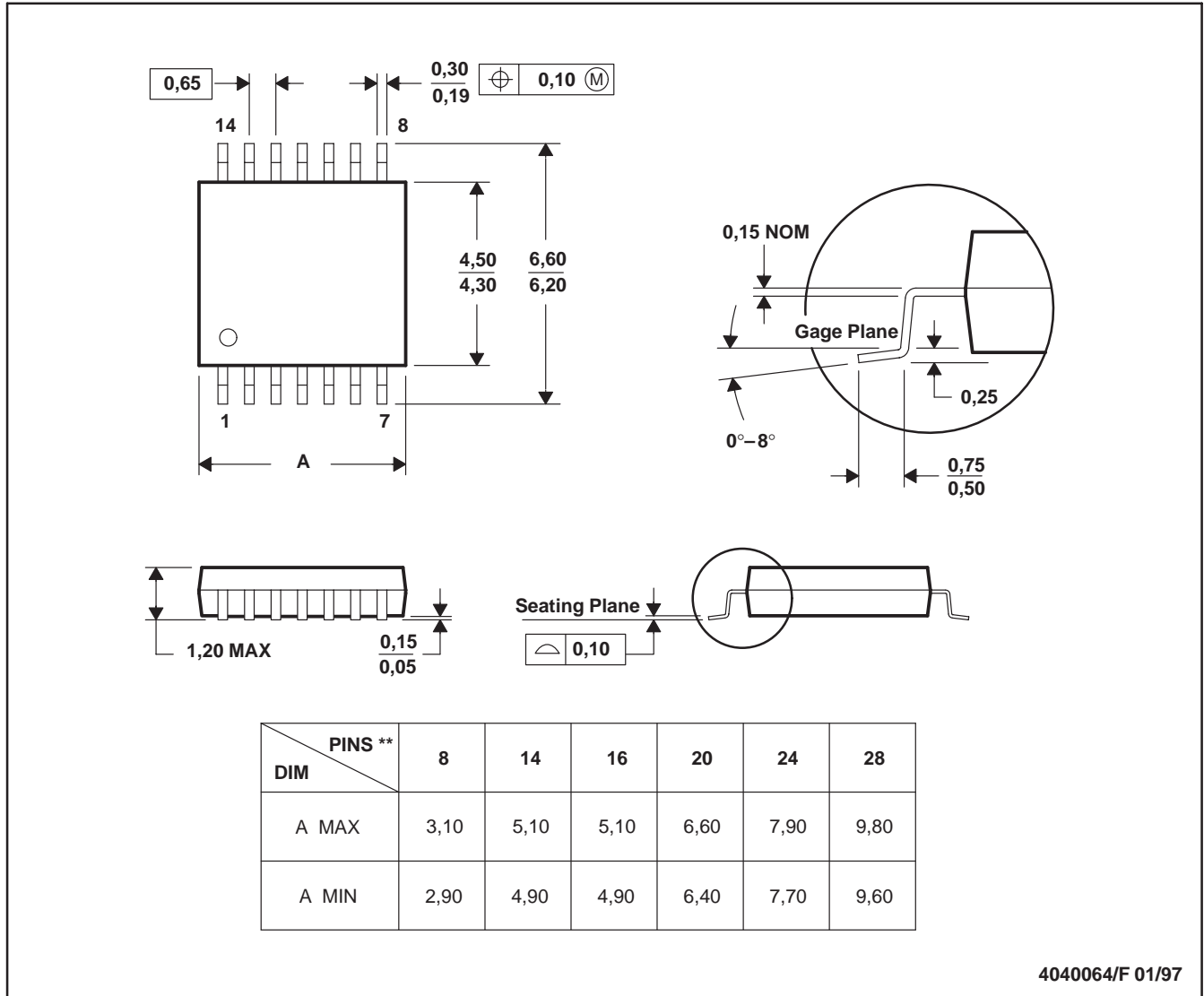
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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