

# SN74ALVCH32501 36-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES144C – OCTOBER 1998 – REVISED MAY 2000

- Member of the Texas Instruments *Widebus*™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Packaged in Plastic Fine-Pitch Ball Grid Array Package

## description

This 36-bit universal bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

This device can be used as two 18-bit transceivers or one 36-bit transceiver. Data flow in each direction is controlled by output-enable (OEAB and  $\overline{OEBA}$ ), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses  $\overline{OEBA}$ , LEBA, and CLKBA. The output enables are complementary (OEAB is active high and  $\overline{OEBA}$  is active low).

To ensure the high-impedance state during power up or power down,  $\overline{OEBA}$  should be tied to  $V_{CC}$  through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH32501 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE†

INPUTS				A	OUTPUT B
OEAB	LEAB	CLKAB			
L	X	X	X		Z
H	H	X	L		L
H	H	X	H		H
H	L	↑	L		L
H	L	↑	H		H
H	L	H	X		$B_0^{\ddagger}$
H	L	L	X		$B_0^{\S}$

† A-to-B data flow is shown; B-to-A flow is similar but uses  $\overline{OEBA}$ , LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established



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# SN74ALVCH32501

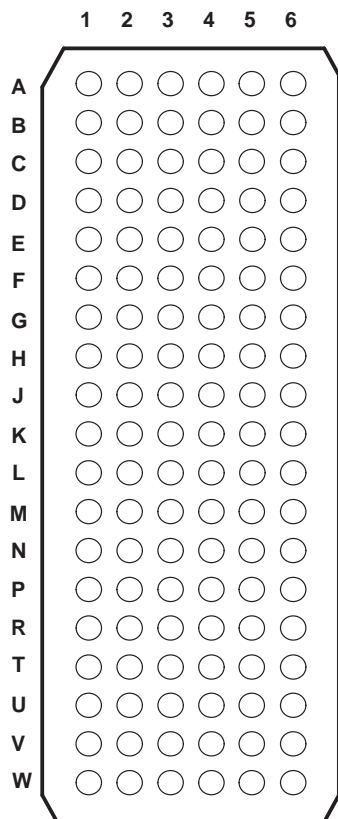
## 36-BIT UNIVERSAL BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

SCES144C – OCTOBER 1998 – REVISED MAY 2000

#### terminal assignments

GKF PACKAGE  
(TOP VIEW)



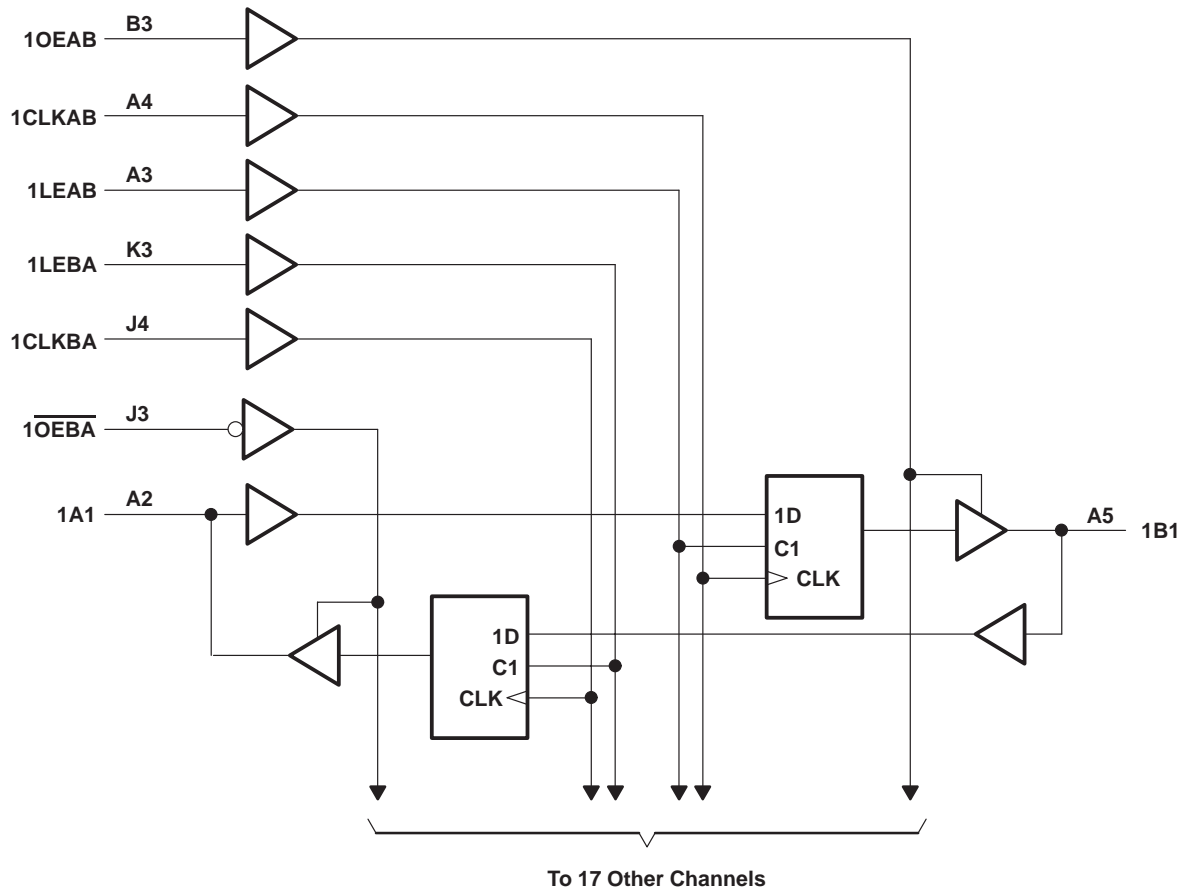
	1	2	3	4	5	6
A	1A2	1A1	1LEAB	1CLKAB	1B1	1B2
B	1A4	1A3	1OEAB	GND	1B3	1B4
C	1A6	1A5	GND	GND	1B5	1B6
D	1A8	1A7	V <sub>CC</sub>	V <sub>CC</sub>	1B7	1B8
E	1A10	1A9	GND	GND	1B9	1B10
F	1A12	1A11	GND	GND	1B11	1B12
G	1A14	1A13	V <sub>CC</sub>	V <sub>CC</sub>	1B13	1B14
H	1A15	1A16	GND	GND	1B16	1B15
J	1A17	1A18	1OEBA	1CLKBA	1B18	1B17
K	NC	2LEAB	1LEBA	GND	2CLKAB	NC
L	2A2	2A1	2OEAB	GND	2B1	2B2
M	2A4	2A3	GND	GND	2B3	2B4
N	2A6	2A5	V <sub>CC</sub>	V <sub>CC</sub>	2B5	2B6
P	2A8	2A7	GND	GND	2B7	2B8
R	2A10	2A9	GND	GND	2B9	2B10
T	2A12	2A11	V <sub>CC</sub>	V <sub>CC</sub>	2B11	2B12
U	2A14	2A13	GND	GND	2B13	2B14
V	2A15	2A16	2OEBA	2CLKBA	2B16	2B15
W	2A17	2A18	2LEBA	GND	2B18	2B17

NC – No internal connection

SN74ALVCH32501  
 36-BIT UNIVERSAL BUS TRANSCEIVER  
 WITH 3-STATE OUTPUTS

SCES144C – OCTOBER 1998 – REVISED MAY 2000

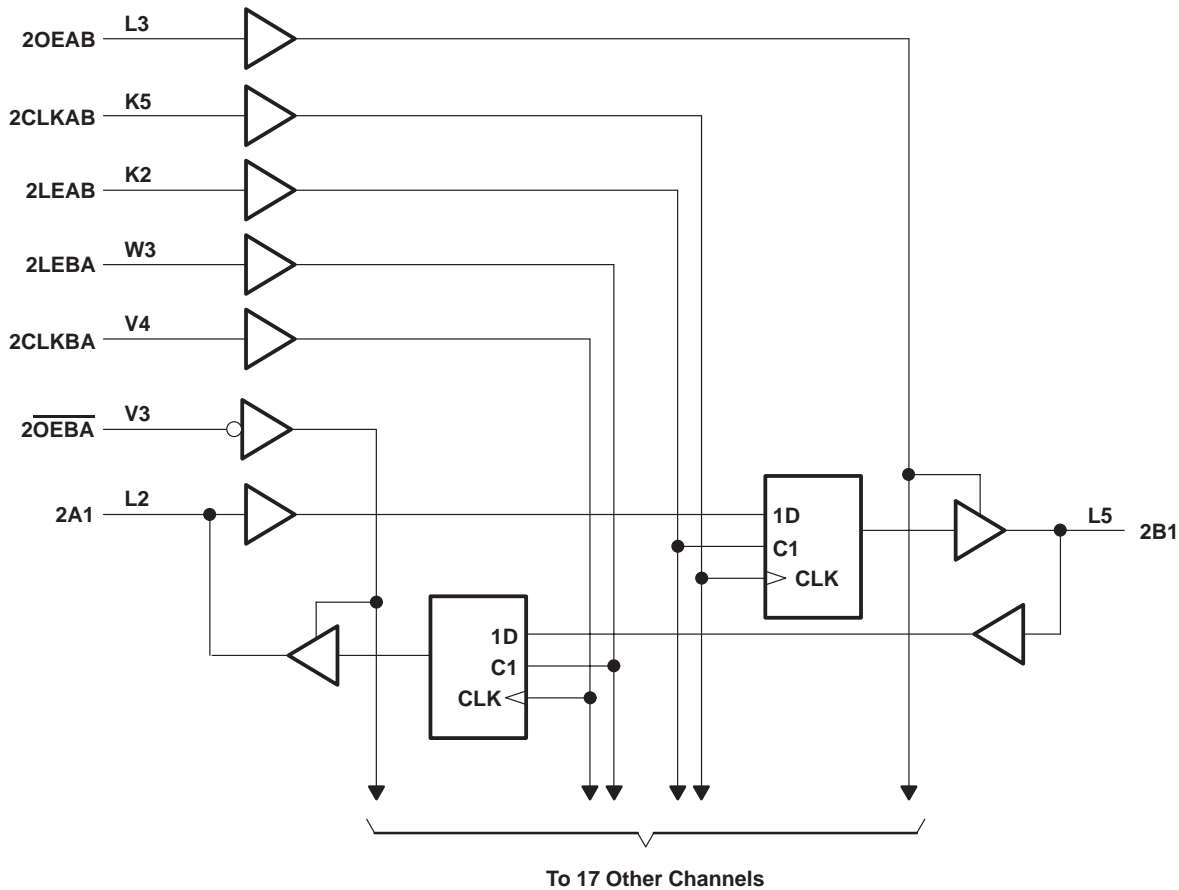
logic diagram (positive logic)



**SN74ALVCH32501**  
**36-BIT UNIVERSAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCES144C – OCTOBER 1998 – REVISED MAY 2000

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ : Except I/O ports (see Note 1) .....	-0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 50$ mA
Continuous current through each $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) .....	39°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output-current ratings are observed.  
 2. This value is limited to 4.6 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51.



**SN74ALVCH32501**  
**36-BIT UNIVERSAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCES144C – OCTOBER 1998 – REVISED MAY 2000

**recommended operating conditions (see Note 4)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	-4	mA
		V <sub>CC</sub> = 2.3 V	-12	
		V <sub>CC</sub> = 2.7 V	-12	
		V <sub>CC</sub> = 3 V	-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	4	mA
		V <sub>CC</sub> = 2.3 V	12	
		V <sub>CC</sub> = 2.7 V	12	
		V <sub>CC</sub> = 3 V	24	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**SN74ALVCH32501**  
**36-BIT UNIVERSAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCES144C – OCTOBER 1998 – REVISED MAY 2000

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> -0.2			V
	I <sub>OH</sub> = -4 mA	1.65 V	1.2			
	I <sub>OH</sub> = -6 mA	2.3 V	2			
	I <sub>OH</sub> = -12 mA	2.3 V	1.7			
		2.7 V	2.2			
		3 V	2.4			
I <sub>OH</sub> = -24 mA	3 V	2				
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
	I <sub>OL</sub> = 6 mA	2.3 V			0.4	
	I <sub>OL</sub> = 12 mA	2.3 V			0.7	
		2.7 V			0.4	
	I <sub>OL</sub> = 24 mA	3 V			0.55	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±5	μA
I <sub>I</sub> (hold)	V <sub>I</sub> = 0.58 V	1.65 V	25			μA
	V <sub>I</sub> = 1.07 V		-25			
	V <sub>I</sub> = 0.7 V	2.3 V	45			
	V <sub>I</sub> = 1.7 V		-45			
	V <sub>I</sub> = 0.8 V	3 V	75			
	V <sub>I</sub> = 2 V		-75			
	V <sub>I</sub> = 0 to 3.6 V‡		±500			
I <sub>OZ</sub> §	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			20	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	4		pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	8		pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.



**SN74ALVCH32501**  
**36-BIT UNIVERSAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCES144C – OCTOBER 1998 – REVISED MAY 2000

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)**

			V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f <sub>clock</sub>	Clock frequency		†		150		150		150		MHz	
t <sub>w</sub>	Pulse duration	LE high	†		3.3		3.3		3.3		ns	
		CLK high or low	†		3.3		3.3		3.3			
t <sub>su</sub>	Setup time	Data before CLK↑	†		2.2		2.1		1.7		ns	
		Data before LE↓	CLK high	†		1.9		1.6		1.5		
			CLK low	†		1.3		1.1		1		
t <sub>h</sub>	Hold time	Data after CLK↑	†		0.6		0.6		0.7		ns	
		Data after LE↓	CLK high or low	†		1.4		1.7		1.4		

† This information was not available at the time of publication.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			†		150		150		150		MHz
t <sub>pd</sub>	A or B	B or A	†		1	4.8	4.5		1	3.9	ns
	LE	A or B	†		1.1	5.7	5.3		1.3	4.6	
	CLK		†		1.2	6.1	5.6		1.4	4.9	
t <sub>en</sub>	OEAB	B	†		1	5.8	5.3		1	4.6	ns
t <sub>dis</sub>	OEAB	B	†		1.5	6.2	5.7		1.4	5	ns
t <sub>en</sub>	$\overline{\text{OEBA}}$	A	†		1.3	6.3	6		1.1	5	ns
t <sub>dis</sub>	$\overline{\text{OEBA}}$	A	†		1.3	5.3	4.6		1.3	4.2	ns

† This information was not available at the time of publication.

**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
				TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	C <sub>L</sub> = 0, f = 10 MHz	†	44	54	pF
		Outputs disabled		†	6	6	

† This information was not available at the time of publication.

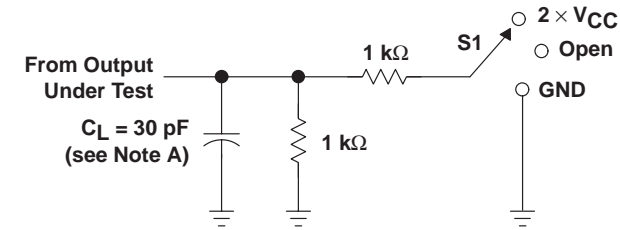


**SN74ALVCH32501**  
**36-BIT UNIVERSAL BUS TRANSCEIVER**  
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SCES144C – OCTOBER 1998 – REVISED MAY 2000

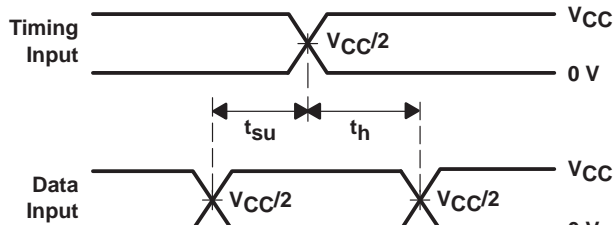
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 1.8\text{ V}$

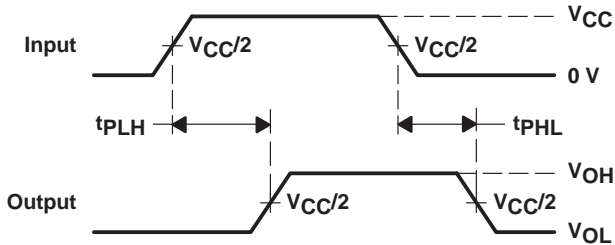


**LOAD CIRCUIT**

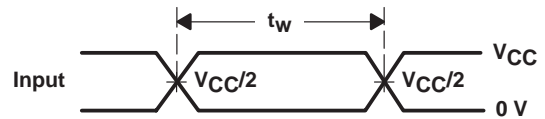
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



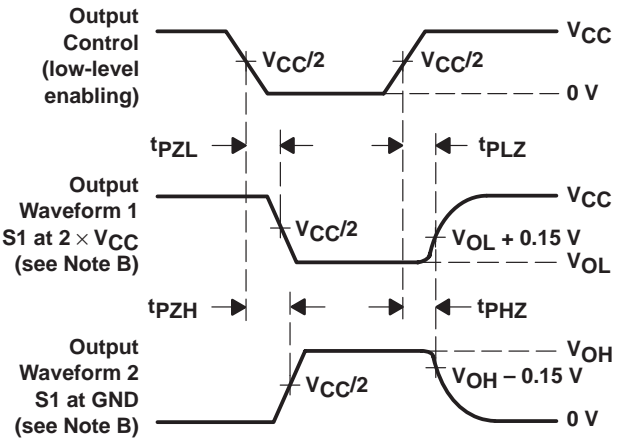
**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
 PULSE DURATION**



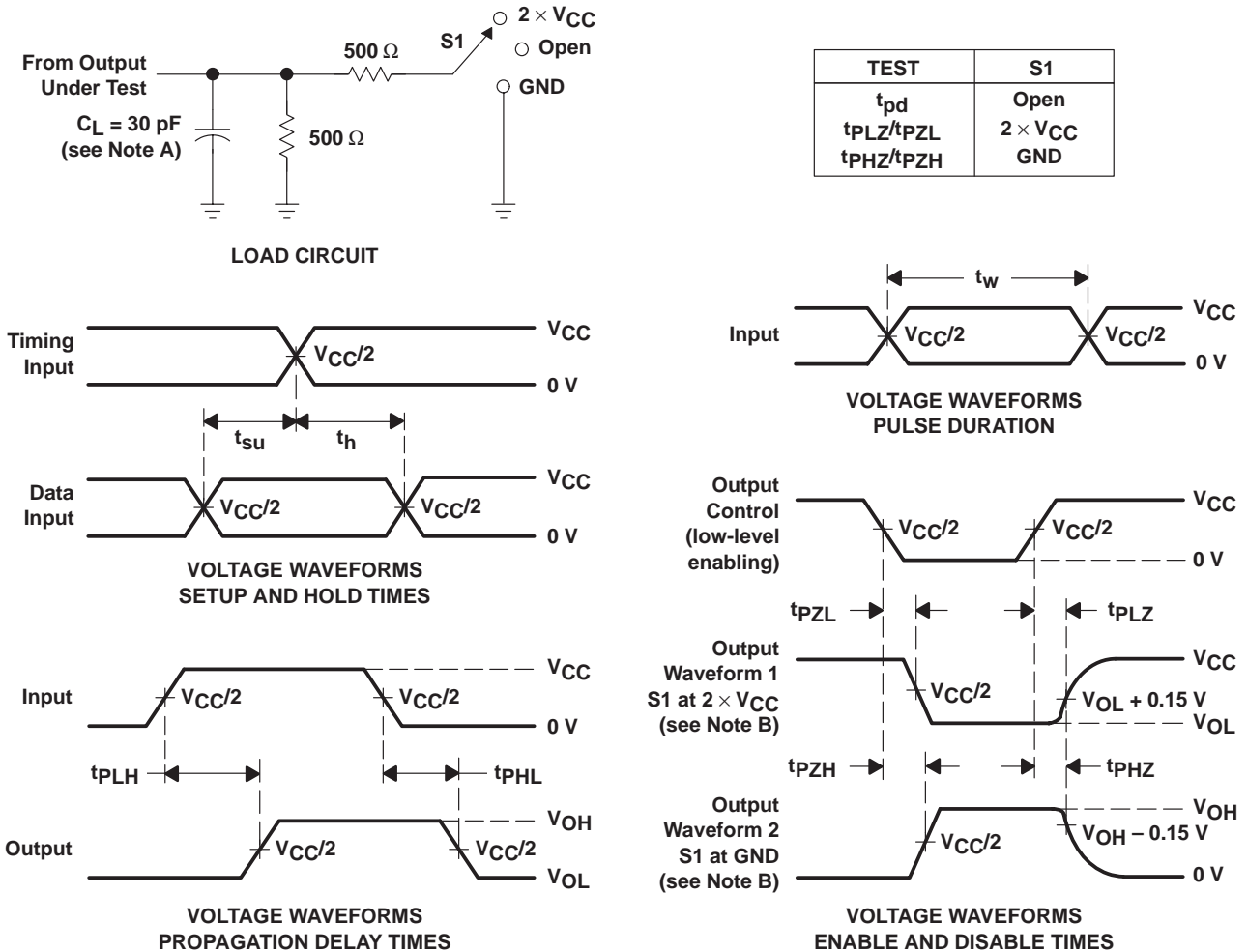
**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES**

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
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 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

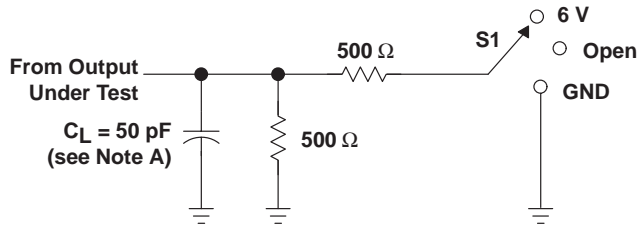
Figure 2. Load Circuit and Voltage Waveforms

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**36-BIT UNIVERSAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCES144C – OCTOBER 1998 – REVISED MAY 2000

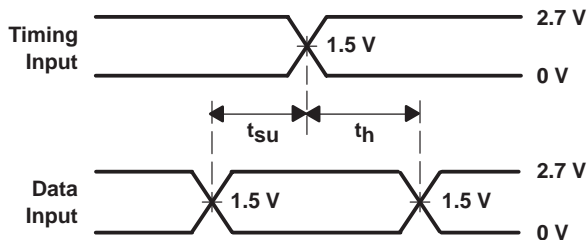
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

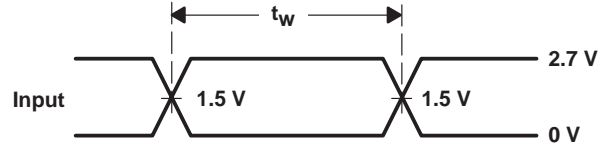


**LOAD CIRCUIT**

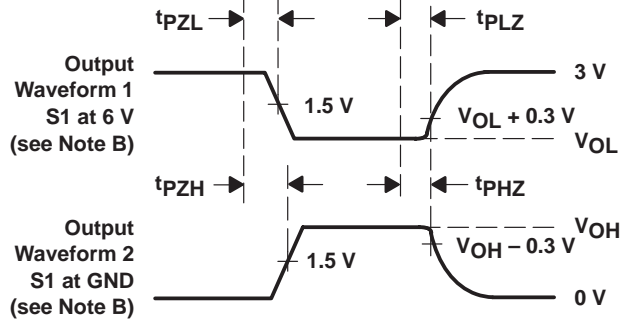
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



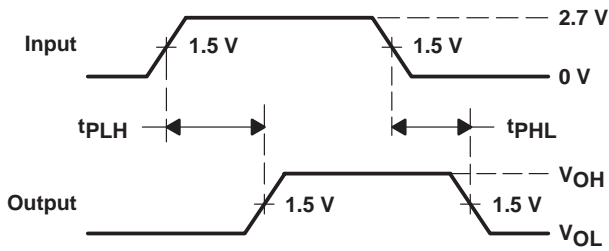
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**

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 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 3. Load Circuit and Voltage Waveforms**

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