

SN74ALVCHR16269A

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES050L – AUGUST 1995 – REVISED JUNE 1999

- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages**

NOTE: For order entry:
The DGG package is abbreviated to G,
the DGV package is abbreviated to V, and
the DL package is abbreviated to L.

For tape and reel:
The DGGR package is abbreviated to GR,
the DGVR package is abbreviated to VR, and
the DLR package is abbreviated to LR.

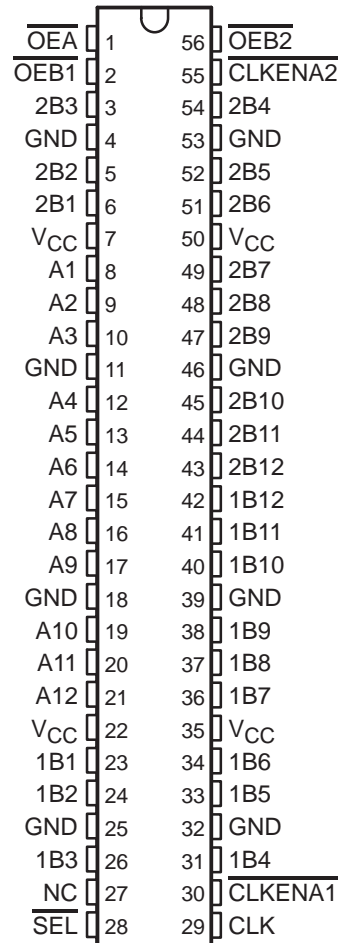
description

This 12-bit to 24-bit registered bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCHR16269A is used in applications in which two ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (CLKENA) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select (\overline{SEL}) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables (\overline{OEA} , $\overline{OEB1}$, and $\overline{OEB2}$).

**DGG, DGV, OR DL PACKAGE
(TOP VIEW)**



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated

SN74ALVCHR16269A

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER

WITH 3-STATE OUTPUTS

SCES050L – AUGUST 1995 – REVISED JUNE 1999

description (continued)

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible and \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to \overline{OE} being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

All outputs are designed to sink up to 12 mA, and include equivalent 26- Ω resistors to reduce overshoot and undershoot.

The SN74ALVCHR16269A is characterized for operation from -40°C to 85°C .

Function Tables

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	\overline{OEA}	\overline{OEB}	A	1B, 2B
\uparrow	H	H	Z	Z
\uparrow	H	L	Z	Active
\uparrow	L	H	Active	Z
\uparrow	L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB} = L$)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
L	H	\uparrow	L	L	$2B_0^{\dagger}$
L	H	\uparrow	H	H	$2B_0^{\dagger}$
L	L	\uparrow	L	L	L
L	L	\uparrow	H	H	H
H	L	\uparrow	L	$1B_0^{\dagger}$	L
H	L	\uparrow	H	$1B_0^{\dagger}$	H
H	H	X	X	$1B_0^{\dagger}$	$2B_0^{\dagger}$

\dagger Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEA} = L$)

INPUTS				OUTPUT
CLK	\overline{SEL}	1B	2B	A
X	H	X	X	A_0^{\dagger}
X	L	X	X	A_0^{\dagger}
\uparrow	H	L	X	L
\uparrow	H	H	X	H
\uparrow	L	X	L	L
\uparrow	L	X	H	H

\dagger Output level before the indicated steady-state input conditions were established

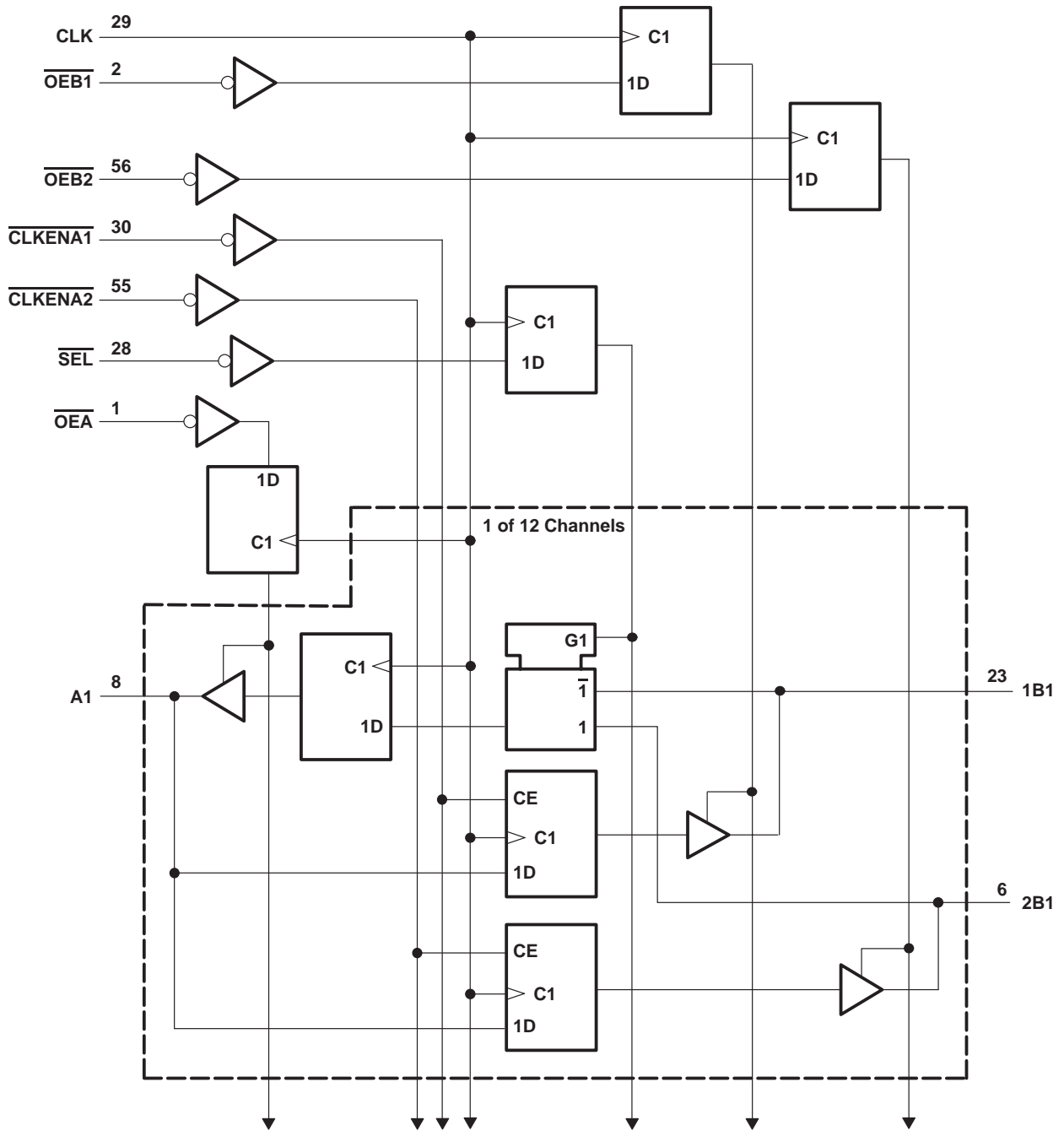


SN74ALVCHR16269A

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES050L – AUGUST 1995 – REVISED JUNE 1999

logic diagram (positive logic)



SN74ALVCHR16269A

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER

WITH 3-STATE OUTPUTS

SCES050L – AUGUST 1995 – REVISED JUNE 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DGV package	86°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.65	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	
		$V_{CC} = 2.7$ V to 3.6 V	2	
V_{IL}	Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	0.7	
		$V_{CC} = 2.7$ V to 3.6 V	0.8	
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65$ V	–2	mA
		$V_{CC} = 2.3$ V	–6	
		$V_{CC} = 2.7$ V	–8	
		$V_{CC} = 3$ V	–12	
I_{OL}	Low-level output current	$V_{CC} = 1.65$ V	2	mA
		$V_{CC} = 2.3$ V	6	
		$V_{CC} = 2.7$ V	8	
		$V_{CC} = 3$ V	12	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74ALVCHR16269A

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES050L – AUGUST 1995 – REVISED JUNE 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			V
	I _{OH} = -2 mA	1.65 V	1.2			
	I _{OH} = -4 mA	2.3 V	1.9			
	I _{OH} = -6 mA	2.3 V	1.7			
		3 V	2.4			
	I _{OH} = -8 mA	2.7 V	2			
I _{OH} = -12 mA	3 V	2				
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 2 mA	1.65 V			0.45	
	I _{OL} = 4 mA	2.3 V			0.4	
	I _{OL} = 6 mA	2.3 V			0.55	
		3 V			0.55	
	I _{OL} = 8 mA	2.7 V			0.6	
I _{OL} = 12 mA	3 V			0.8		
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA
I _I (hold)	V _I = 0.58 V	1.65 V	25			μA
	V _I = 1.07 V		-25			
	V _I = 0.7 V	2.3 V	45			
	V _I = 1.7 V		-45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V		-75			
	V _I = 0 to 3.6 V‡	3.6 V			±500	
I _{OZ} §	V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			40	μA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	5		pF
C _{iO}	A or B ports	V _O = V _{CC} or GND	3.3 V	8.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCHR16269A

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER

WITH 3-STATE OUTPUTS

SCES050L – AUGUST 1995 – REVISED JUNE 1999

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	†		95		115		135		MHz
t _w	Pulse duration, CLK high or low	†		5.2		4.3		3.3		ns
t _{su}	Setup time	A data before CLK↑		†		1.4		1		ns
		B data before CLK↑		†		1.6		1.1		
		$\overline{\text{SEL}}$ before CLK↑		†		0.8		1.1		
		CLKENA1 or CLKENA2 before CLK↑		†		0.8		1		
		$\overline{\text{OE}}$ before CLK↑		†		1.7		1.6		
t _h	Hold time	A data after CLK↑		†		0.9		1.2		ns
		B data after CLK↑		†		0.8		1		
		$\overline{\text{SEL}}$ after CLK↑		†		1.1		0.8		
		CLKENA1 or CLKENA2 after CLK↑		†		1.4		1		
		$\overline{\text{OE}}$ after CLK↑		†		0.9		0.8		

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		95		115		135		MHz
t _{pd}	CLK	B	†		2.3	7.7	6.9		2.2	5.8	ns
		A	†		1.9	6.4	5.8		2	5.2	
t _{en}	CLK	B	†		2.5	7.7	6.9		2.3	5.8	ns
		A	†		2.2	6.7	6		2.1	5.3	
t _{dis}	CLK	B	†		3.3	8.1	6.7		2.4	6	ns
		A	†		2.7	8	6.2		2.1	6	

† This information was not available at the time of publication.

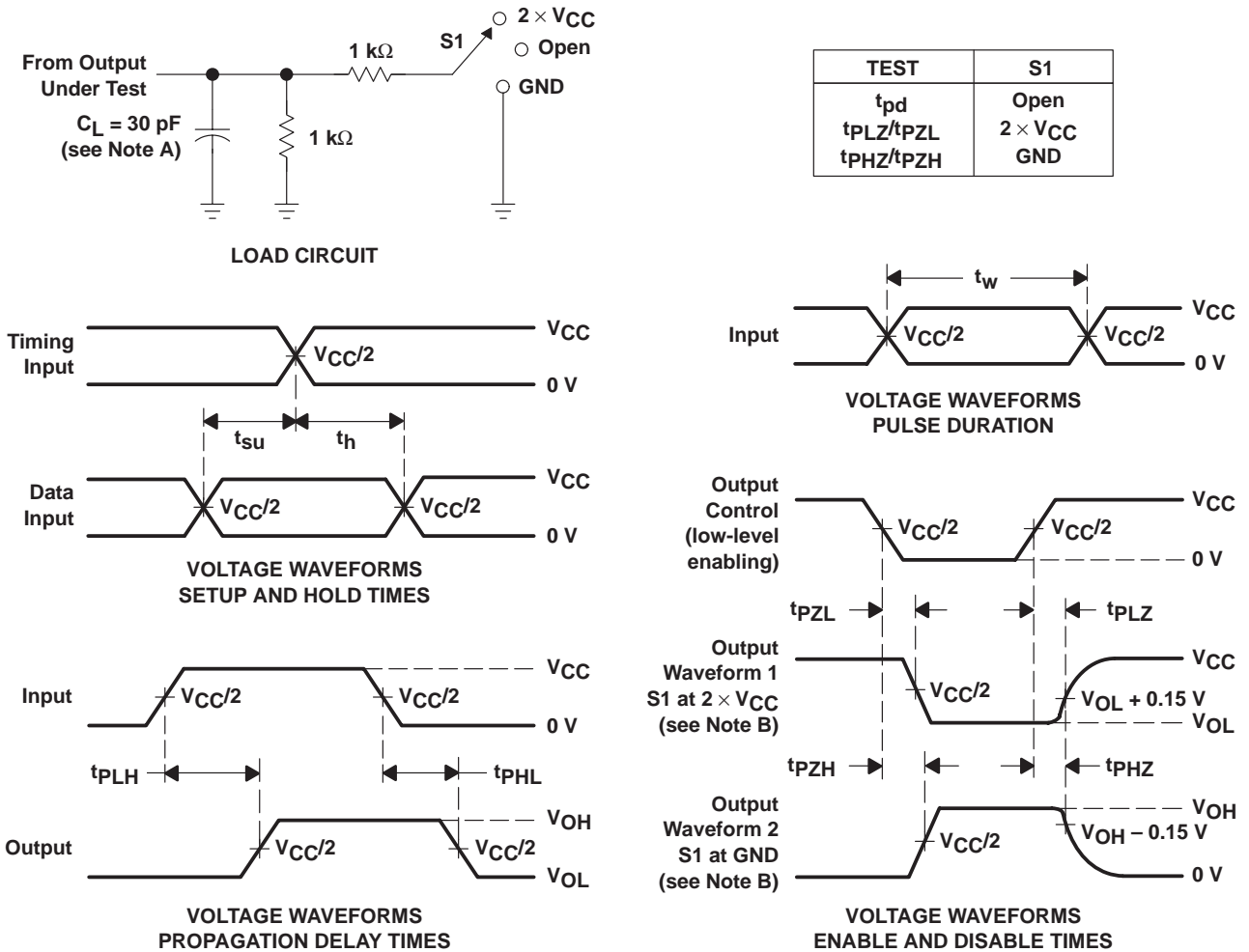
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	All outputs enabled	†	142	172	pF
		All outputs disabled	†	115	129	

† This information was not available at the time of publication.



PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8\text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

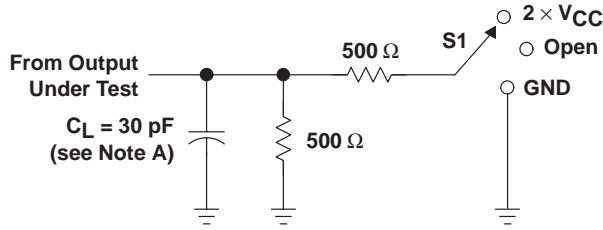
Figure 1. Load Circuit and Voltage Waveforms

SN74ALVCHR16269A
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

SCES050L – AUGUST 1995 – REVISED JUNE 1999

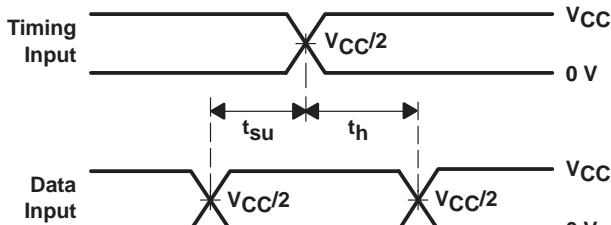
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

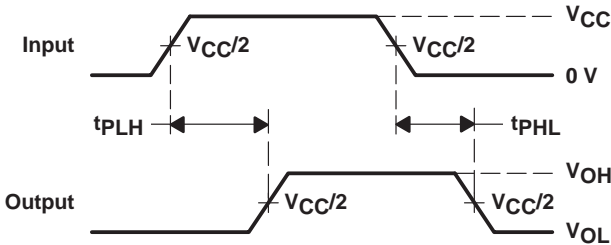


LOAD CIRCUIT

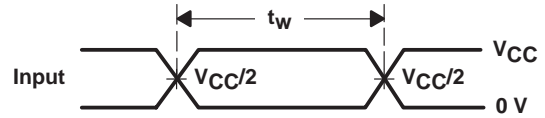
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



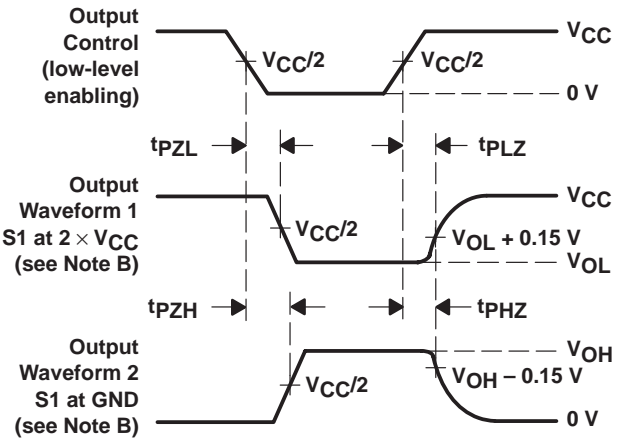
**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
 PULSE DURATION**

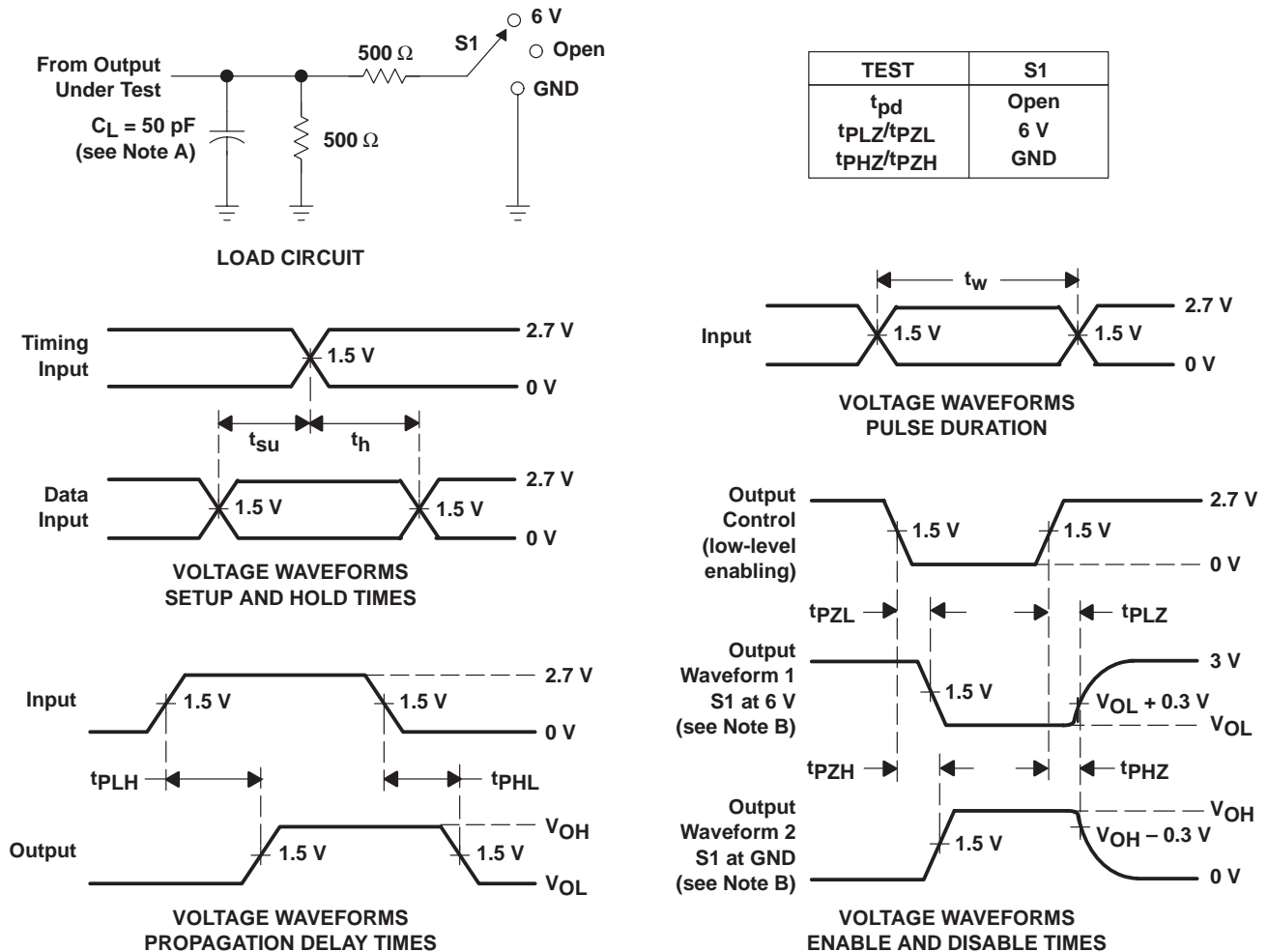


**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES**

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.