

# SN74CBT16233

## 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS010K – MAY 1995 – REVISED NOVEMBER 2001

- Member of the Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

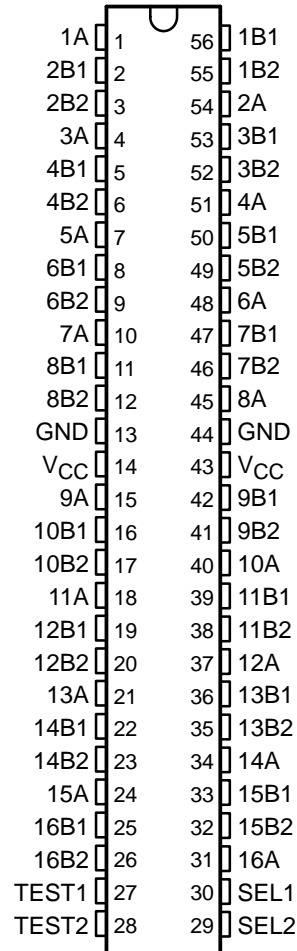
### description

The SN74CBT16233 is a 16-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, where two different banks of memory need to be addressed simultaneously. The device can be used as two 8-bit to 16-bit multiplexers or as one 16-bit to 32-bit multiplexer.

Two select (SEL1 and SEL2) inputs control the data flow. When the TEST inputs are asserted, the A port is connected to both the B1 and the B2 ports. SEL1, SEL2, and the TEST inputs can be driven with a 5-V CMOS, a 5-V TTL, or a low-voltage TTL driver.

This device is designed so it does not have through current when switching directions.

### DGG, DGV, OR DL PACKAGE (TOP VIEW)



### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBT16233DL	CBT16233
		Tape and reel	SN74CBT16233DLR	
	TSSOP – DGG	Tape and reel	SN74CBT16233DGGR	CBT16233
	TVSOP – DGV	Tape and reel	SN74CBT16233DGVR	CY233

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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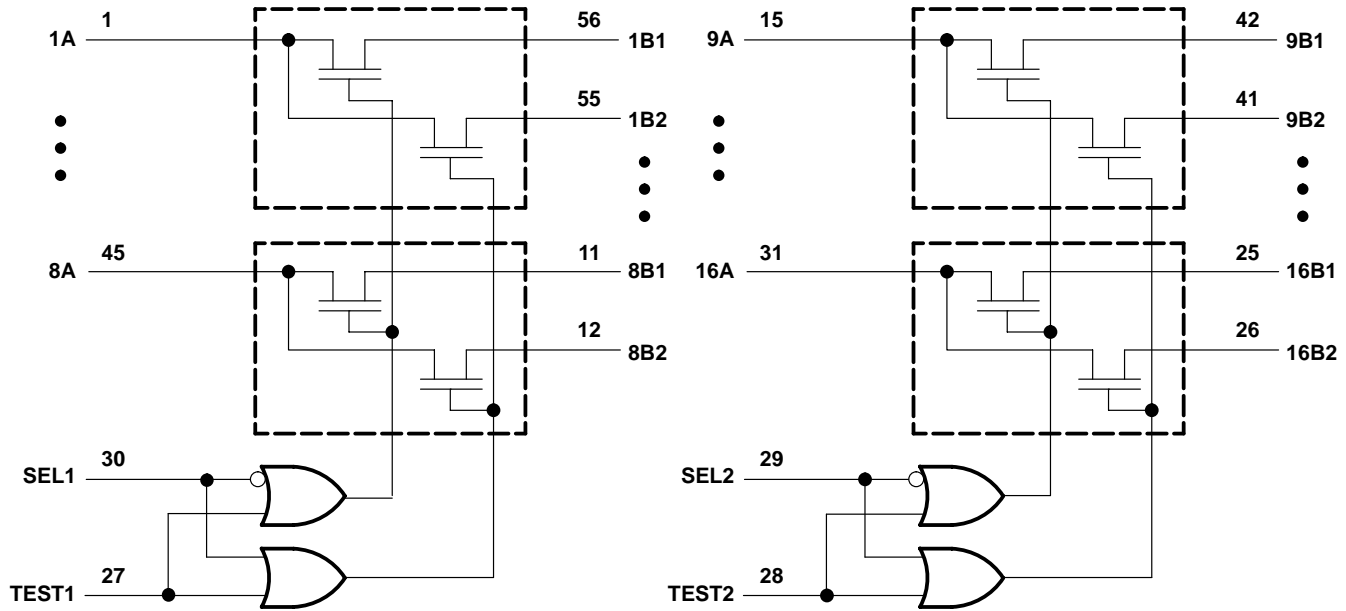
## 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

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**FUNCTION TABLE**  
(each multiplexer/demultiplexer)

INPUTS		FUNCTION
SEL	TEST	
L	L	A = B1
H	L	A = B2
X	H	A = B1 and A = B2

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DGG package	64°C/W
DGV package	48°C/W
DL package	56°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.75	5.25	V
V <sub>IH</sub>	High-level control input voltage	2		V
V <sub>IL</sub>	Low-level control input voltage		0.8	V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.75 V,	I <sub>I</sub> = -18 mA			-1.2	V
I <sub>I</sub>		V <sub>CC</sub> = 0,	V <sub>I</sub> = 5.25 V			10	μA
		V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 5.25 V or GND			±1	μA
I <sub>CC</sub>		V <sub>CC</sub> = 5.25 V,	I <sub>O</sub> = 0,			3	μA
			V <sub>I</sub> = V <sub>CC</sub> or GND				
ΔI <sub>CC</sub> ‡	Control inputs	V <sub>CC</sub> = 5.25 V,	One input at 3.4 V,			2.5	mA
			Other inputs at V <sub>CC</sub> or GND				
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3 V or 0				4.5	pF
C <sub>io(OFF)</sub>		V <sub>O</sub> = 3 V or 0				4	pF
r <sub>on</sub> §		V <sub>CC</sub> = 4.75 V	V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA	5	7	Ω
				I <sub>I</sub> = 30 mA	5	7	
			V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA	7	12	

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

§ Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

### switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>pd</sub> ¶	A or B	B or A		0.25	ns
t <sub>pd</sub>	SEL	A	1.6	5.3	ns
t <sub>en</sub>	TEST or SEL	B	1.3	5.2	ns
t <sub>dis</sub>	TEST or SEL	B	1	5.3	ns

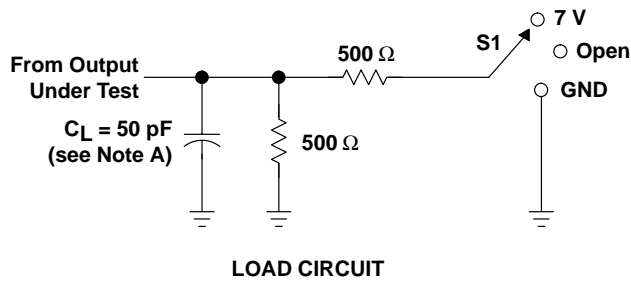
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



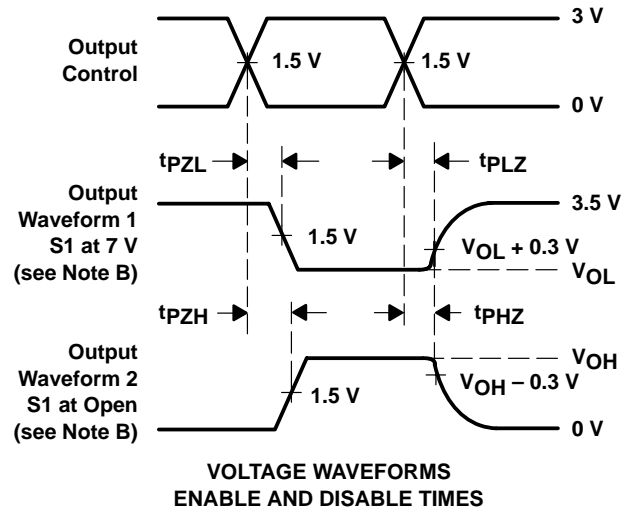
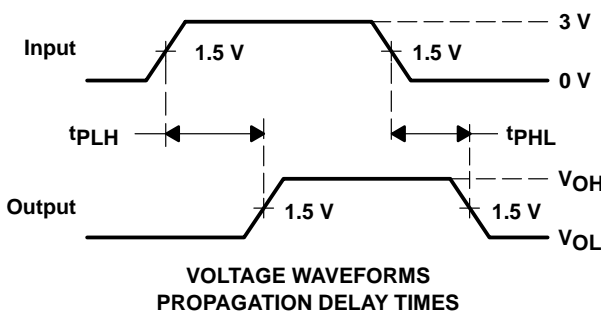
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## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74CBT16233DGGR	ACTIVE	TSSOP	DGG	56	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74CBT16233DGVR	ACTIVE	TVSOP	DGV	56	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74CBT16233DL	ACTIVE	SSOP	DL	56	20	None	CU NIPDAU	Level-1-235C-UNLIM
SN74CBT16233DLR	ACTIVE	SSOP	DL	56	1000	None	CU NIPDAU	Level-1-235C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

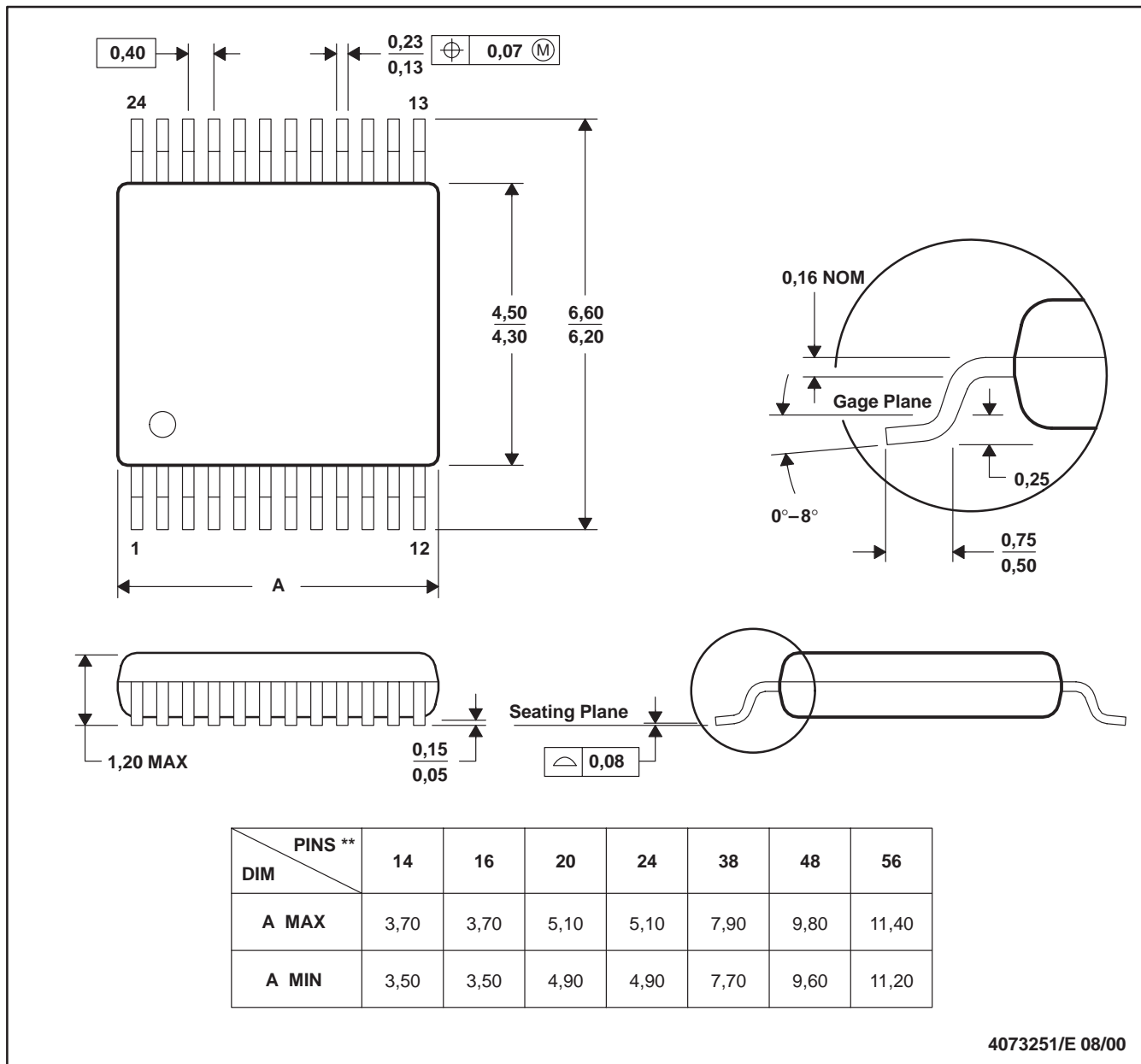
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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

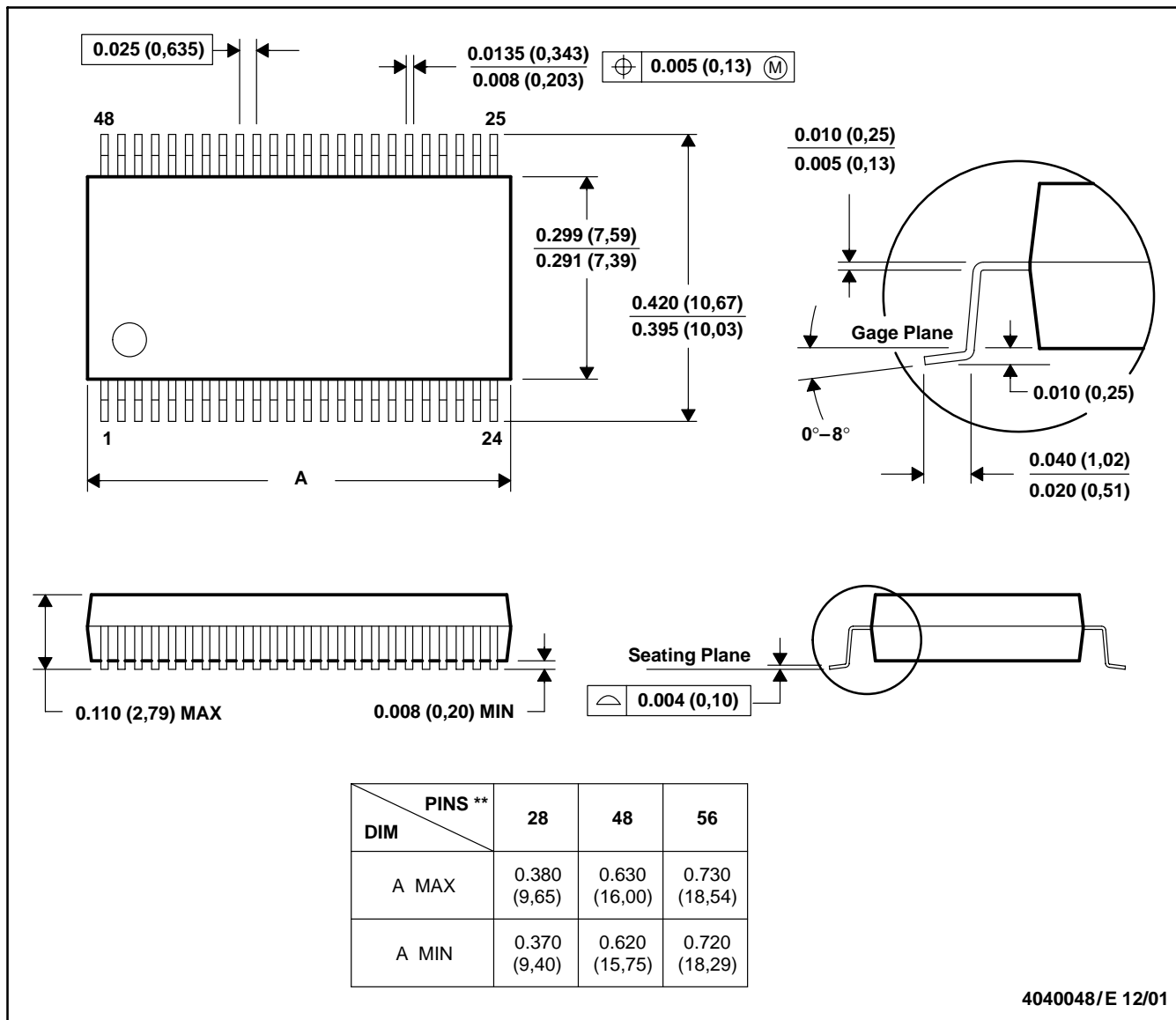


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

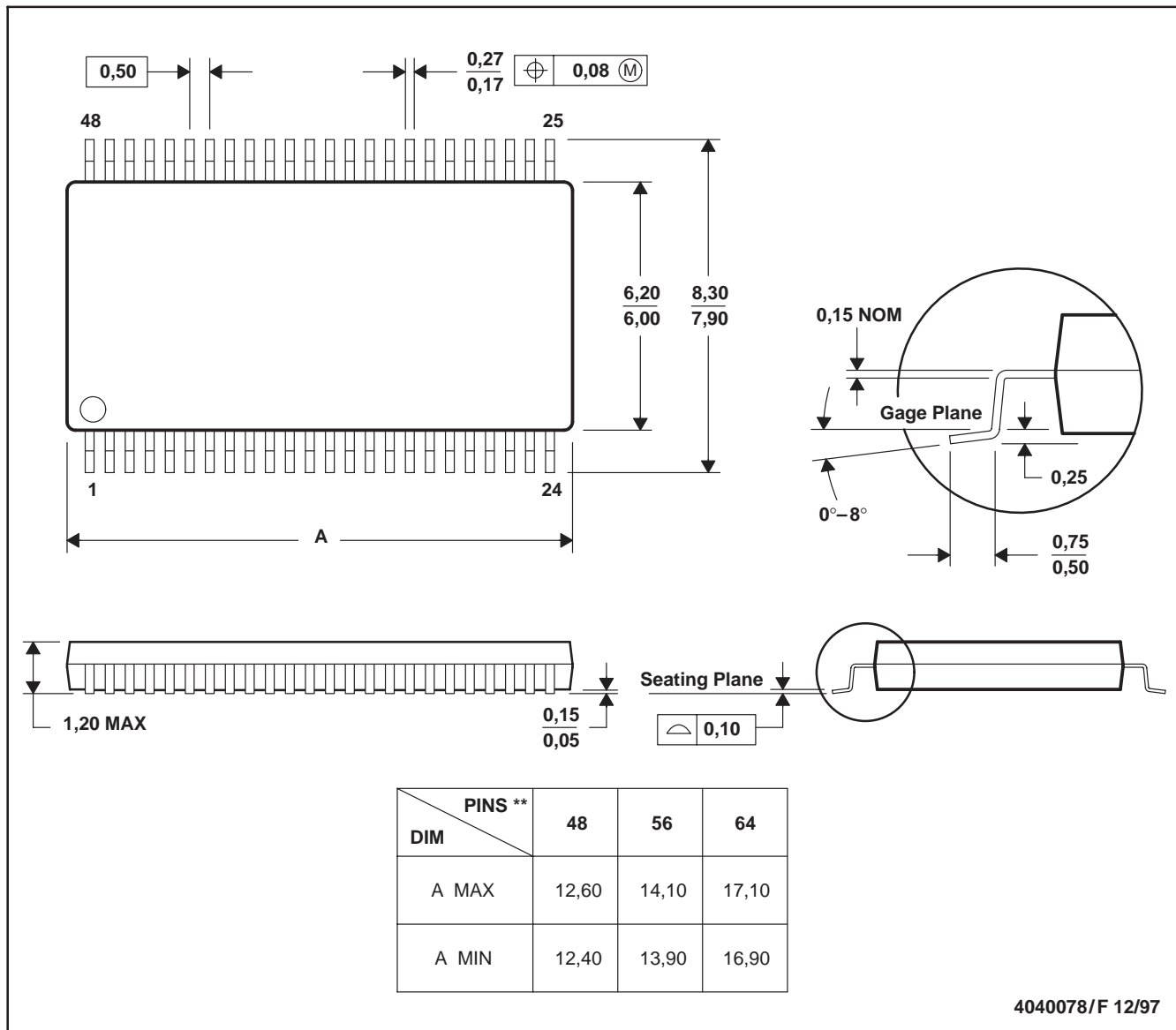


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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