

SN74CBT16233

16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS010H – MAY 1995 – REVISED OCTOBER 1998

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

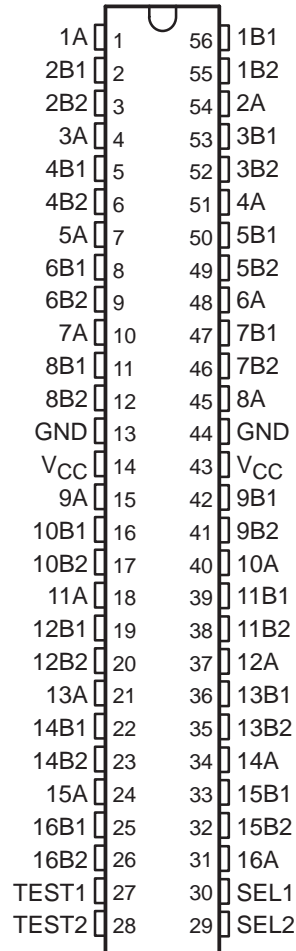
The SN74CBT16233 is a 16-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, where two different banks of memory need to be addressed simultaneously. The device can be used as two 8-bit to 16-bit multiplexers or as one 16-bit to 32-bit multiplexer.

Two select (SEL1 and SEL2) inputs control the data flow. When the TEST inputs are asserted, the A port is connected to both the B1 and the B2 ports. SEL1, SEL2, and the TEST inputs can be driven with a 5-V CMOS, a 5-V TTL, or a low-voltage TTL driver.

The device is specified by design not to have through current when switching directions.

The SN74CBT16233 is characterized for operation from 0°C to 70°C.

**DGG, DGV, OR DL PACKAGE
(TOP VIEW)**



**FUNCTION TABLE
(each multiplexer/demultiplexer)**

INPUTS		FUNCTION
SEL	TEST	
L	L	A = B1
H	L	A = B2
X	H	A = B1 and A = B2



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V_{IK}		$V_{CC} = 4.75\text{ V}$, $I_I = -18\text{ mA}$				-1.2	V	
I_I		$V_{CC} = 0$, $V_I = 5.25\text{ V}$				10	μA	
		$V_{CC} = 5.25\text{ V}$, $V_I = 5.25\text{ V or GND}$				± 1	μA	
I_{CC}		$V_{CC} = 5.25\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$				3	μA	
$\Delta I_{CC}‡$	Control inputs	$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at $V_{CC}\text{ or GND}$				2.5	mA	
C_i	Control inputs	$V_I = 3\text{ V or 0}$				4.5	pF	
$C_{iO(OFF)}$		$V_O = 3\text{ V or 0}$				4	pF	
$r_{on}§$		$V_{CC} = 4.75\text{ V}$	$V_I = 0$			5	7	Ω
						5	7	
			$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$	7	12		

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}¶$	A or B	B or A		0.25	ns
t_{pd}	SEL	A	1.6	5.3	ns
t_{en}	TEST or SEL	B	1.3	5.2	ns
t_{dis}	TEST or SEL	B	1	5.3	ns

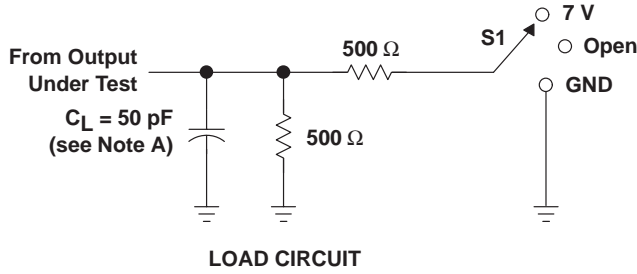
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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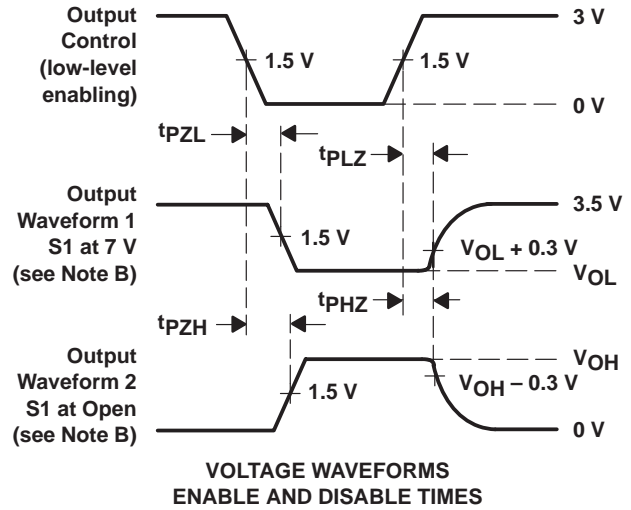
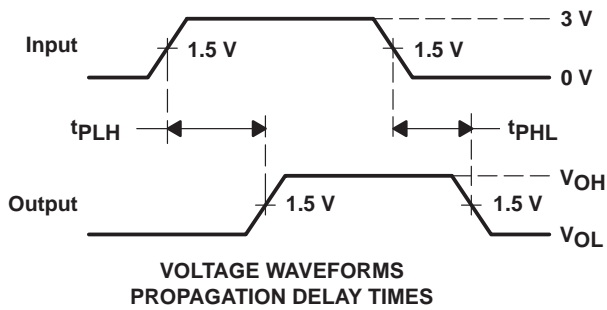
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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