

# SN74CBT16244C

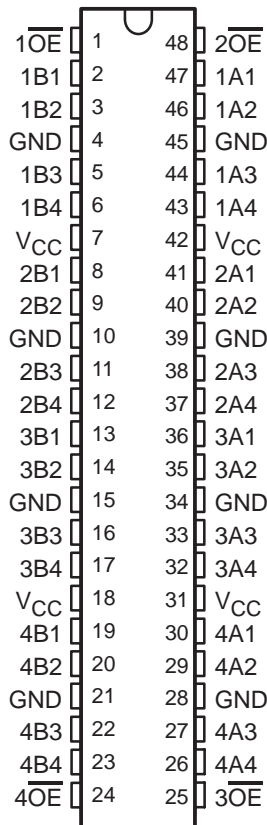
## 16-BIT FET BUS SWITCH

### 5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS134A – SEPTEMBER 2003 – REVISED OCTOBER 2003

- Member of the Texas Instruments Widebus™ Family
- Undershoot Protection for Off-Isolation on A and B Ports Up To -2 V
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{on}$ ) Characteristics ( $r_{on} = 3 \Omega$  Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{iO(OFF)} = 5.5 \text{ pF}$  Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 3 \mu\text{A}$  Max)
- $V_{CC}$  Operating Range From 4 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



#### description/ordering information

#### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBT16244CDL	CBT16244C
		Tape and reel	SN74CBT16244CDLR	
	TSSOP – DGG	Tube	SN74CBT16244CDGG	CBT16244C
		Tape and reel	SN74CBT16244CDGGR	
TVSOP – DGV	Tape and reel	SN74CBT16244CDGVR	CY244C	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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#### description/ordering information (continued)

The SN74CBT16244C is a high-speed TTL-compatible FET bus switch with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16244C provides protection for undershoot up to  $-2$  V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT16244C is organized as four 4-bit bus switches with separate output-enable ( $1\overline{OE}$ ,  $2\overline{OE}$ ,  $3\overline{OE}$ ,  $4\overline{OE}$ ) inputs. It can be used as four 4-bit bus switches, two 8-bit bus switches, or as one 16-bit bus switch. When  $\overline{OE}$  is low, the associated 4-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 4-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

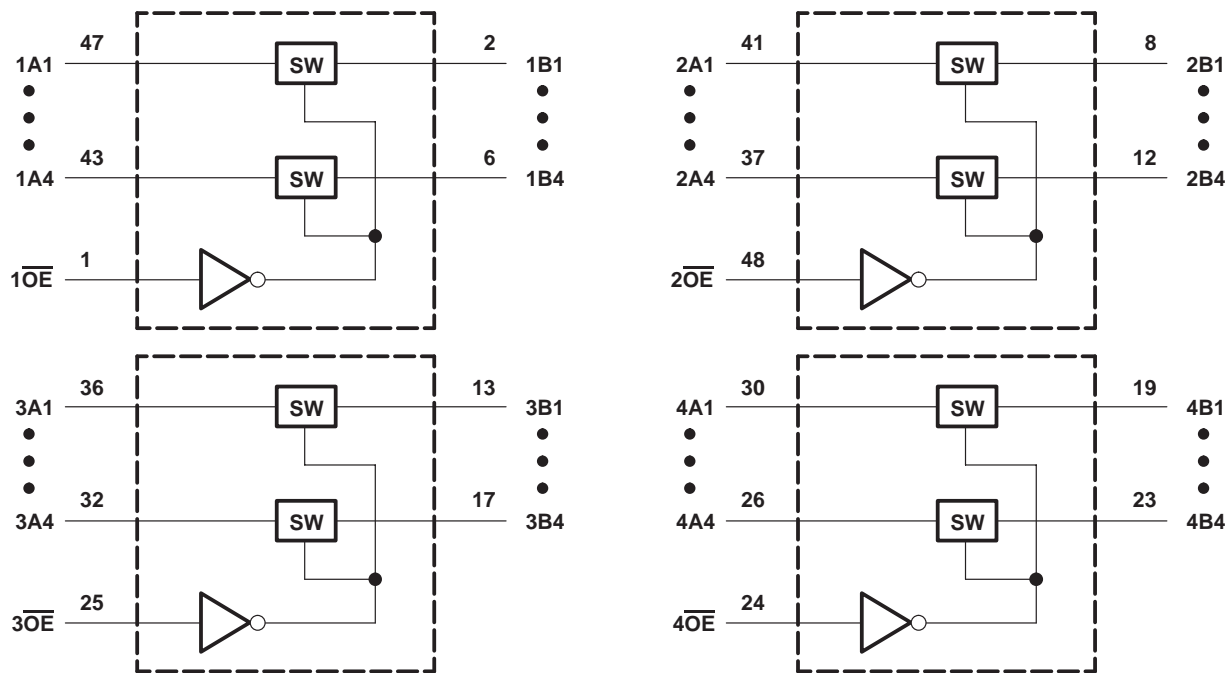
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE  
(each 4-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

#### logic diagram (positive logic)





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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	Control inputs	$V_{CC} = 4.5\text{ V}$ ,	$I_{IN} = -18\text{ mA}$			-1.8	V
$V_{IKU}$	Data inputs	$V_{CC} = 5\text{ V}$ ,	$0\text{ mA} > I_I \geq -50\text{ mA}$ , $V_{IN} = V_{CC}$ or GND, Switch OFF			-2	V
$I_{IN}$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_{IN} = V_{CC}$ or GND			$\pm 1$	$\mu\text{A}$
$I_{OZ}^\ddagger$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$ to $5.5\text{ V}$ , $V_I = 0$ , Switch OFF, $V_{IN} = V_{CC}$ or GND			$\pm 10$	$\mu\text{A}$
$I_{off}$		$V_{CC} = 0$ ,	$V_O = 0$ to $5.5\text{ V}$ , $V_I = 0$			10	$\mu\text{A}$
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ ,	$I_{I/O} = 0$ , $V_{IN} = V_{CC}$ or GND, Switch ON or OFF			3	$\mu\text{A}$
$\Delta I_{CC}^\S$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	One input at $3.4\text{ V}$ , Other inputs at $V_{CC}$ or GND			2.5	mA
$C_{in}$	Control inputs	$V_{IN} = 3\text{ V}$ or 0			3.5		pF
$C_{io(OFF)}$		$V_{I/O} = 3\text{ V}$ or 0, Switch OFF, $V_{IN} = V_{CC}$ or GND			5.5		pF
$C_{io(ON)}$		$V_{I/O} = 3\text{ V}$ or 0, Switch ON, $V_{IN} = V_{CC}$ or GND			14		pF
$r_{on}^\parallel$		$V_{CC} = 4\text{ V}$ , TYP at $V_{CC} = 4\text{ V}$	$V_I = 2.4\text{ V}$ , $I_O = -15\text{ mA}$	8	12	$\Omega$	
			$V_I = 0$ , $I_O = 64\text{ mA}$	3	6		
		$V_{CC} = 4.5\text{ V}$	$V_I = 0$ , $I_O = 30\text{ mA}$	3	6		
			$V_I = 2.4\text{ V}$ , $I_O = -15\text{ mA}$	5	10		

$V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.

† All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than  $V_{CC}$  or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^\#$	A or B	B or A	0.24		0.15		ns
$t_{en}$	$\overline{OE}$	A or B	5.1		1.5	4.7	ns
$t_{dis}$	$\overline{OE}$	A or B	5.2		1.5	5.4	ns

# The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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**16-BIT FET BUS SWITCH**  
**5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION**

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undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OUTU}$	$V_{CC} = 5.5\text{ V}$ , Switch OFF, $V_{IN} = V_{CC}$ or GND	2	$V_{OH} - 0.3$		V

† All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

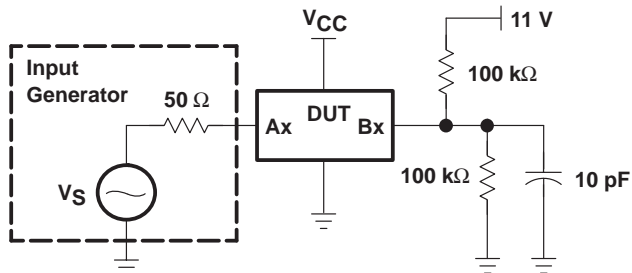


Figure 1. Device Test Setup

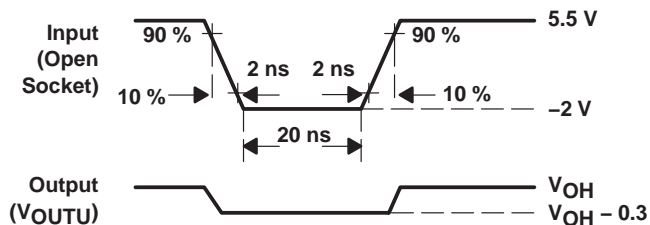
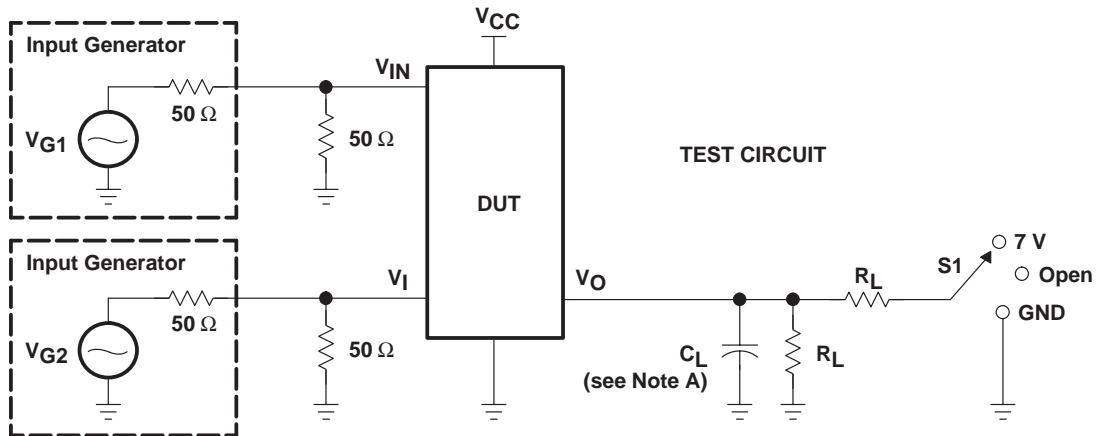


Figure 2. Transient Input Voltage ( $V_i$ ) and Output Voltage ( $V_{OUTU}$ ) Waveforms (Switch OFF)

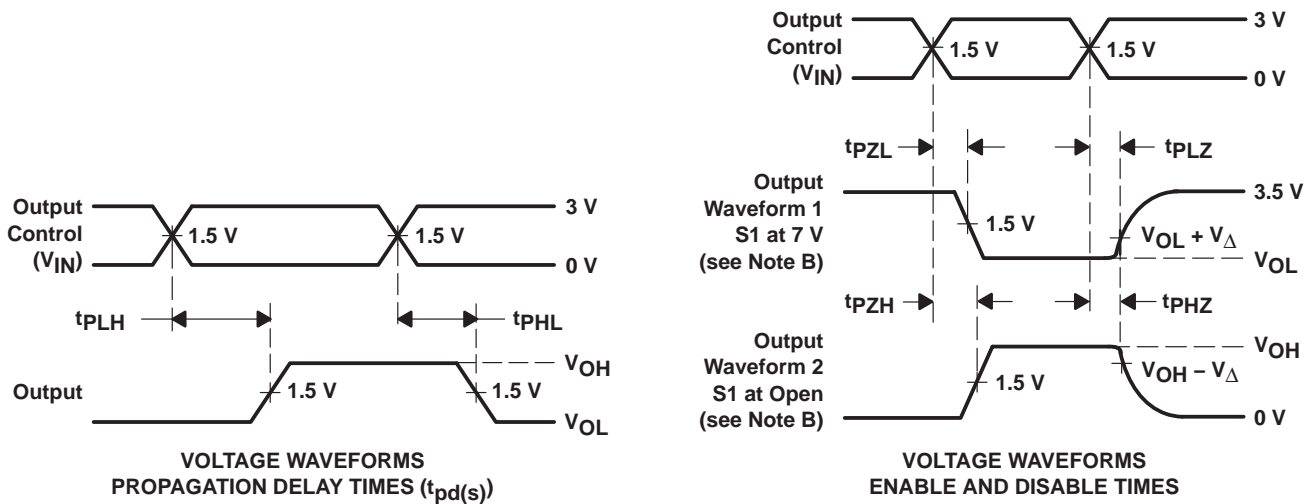
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**PARAMETER MEASUREMENT INFORMATION**



TEST	VCC	S1	RL	VI	CL	VΔ
t <sub>pd</sub> (s)	5 V ± 0.5 V	Open	500 Ω	VCC or GND	50 pF	
	4 V	Open	500 Ω	VCC or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	5 V ± 0.5 V	7 V	500 Ω	GND	50 pF	0.3 V
	4 V	7 V	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	5 V ± 0.5 V	Open	500 Ω	VCC	50 pF	0.3 V
	4 V	Open	500 Ω	VCC	50 pF	0.3 V



- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>(s). The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Test Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74CBT16244CDGGR	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74CBT16244CDGVR	ACTIVE	TVSOP	DGV	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74CBT16244CDL	ACTIVE	SSOP	DL	48	25	None	CU NIPDAU	Level-1-235C-UNLIM
SN74CBT16244CDLR	ACTIVE	SSOP	DL	48	1000	None	CU NIPDAU	Level-1-235C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

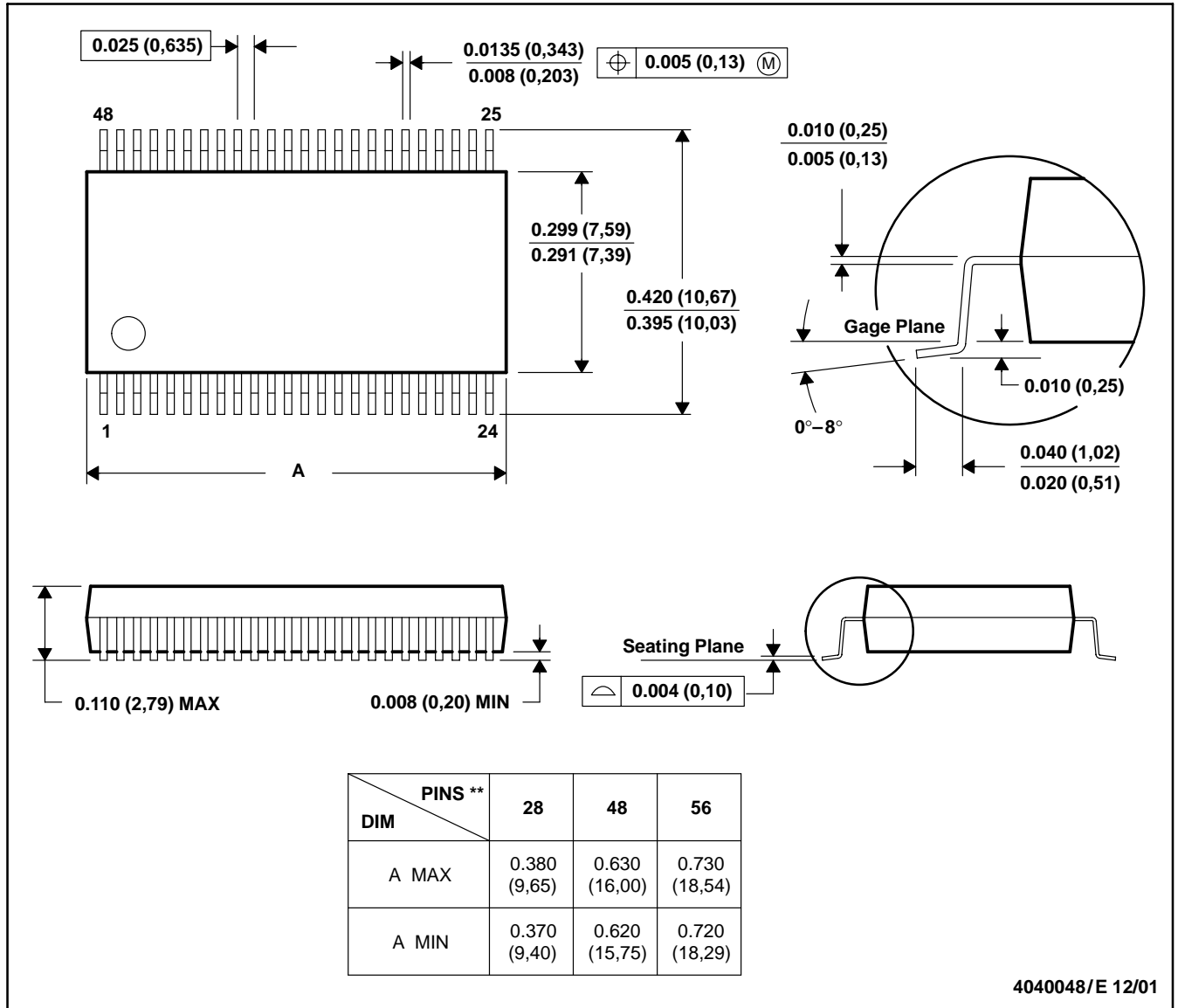


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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