

# SN74CBTD16210 20-BIT FET BUS SWITCH WITH LEVEL SHIFTING

SCDS049H – MARCH 1998 – REVISED JULY 2002

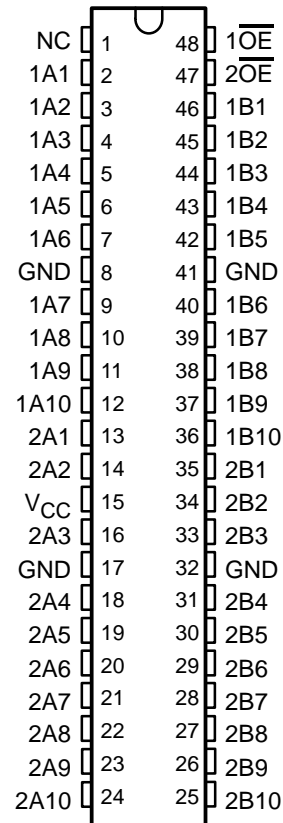
- Member of Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Designed to Be Used in Level-Shifting Applications

## description/ordering information

The SN74CBTD16210 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to  $V_{CC}$  is integrated in the circuit to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

The device is organized as a dual 10-bit bus switch with separate output-enable ( $\overline{OE}$ ) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When  $\overline{OE}$  is low, the associated 10-bit bus switch is on, and port A is connected to port B. When  $\overline{OE}$  is high, the switch is open, and the high-impedance state exists between the ports.

## DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

| $T_A$         | PACKAGE†    |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------|---------------|-----------------------|------------------|
| -40°C to 85°C | SSOP – DL   | Tube          | SN74CBTD16210DL       | CBTD16210        |
|               |             | Tape and reel | SN74CBTD16210DLR      |                  |
|               | TSSOP – DGG | Tape and reel | SN74CBTD16210DGGR     | CBTD16210        |
|               |             | TVSOP – DGV   | Tape and reel         | SN74CBTD16210DGV |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE (each 10-bit bus switch)

| INPUT OE | FUNCTION        |
|----------|-----------------|
| L        | A port = B port |
| H        | Z               |



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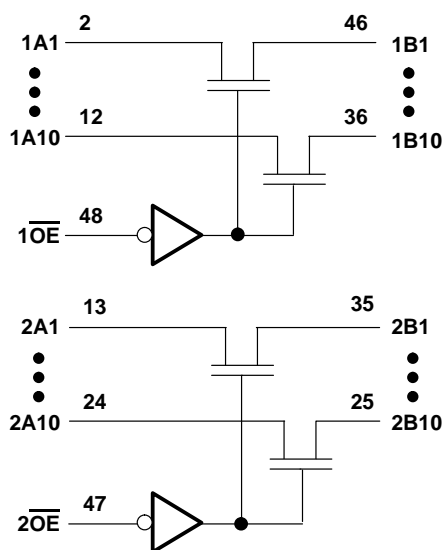
# SN74CBTD16210

## 20-BIT FET BUS SWITCH

### WITH LEVEL SHIFTING

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#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|  |                |
|--|----------------|
| Supply voltage range, $V_{CC}$ .....                   | -0.5 V to 7 V  |
| Input voltage range, $V_I$ (see Note 1) .....          | -0.5 V to 7 V  |
| Continuous channel current .....                       | 128 mA         |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....      | -50 mA         |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): |                |
| DGG package .....                                      | 70°C/W         |
| DGV package .....                                      | 58°C/W         |
| DL package .....                                       | 63°C/W         |
| Storage temperature range, $T_{stg}$ .....             | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 3)

|   | MIN | MAX | UNIT |
|---|-----|-----|------|
| $V_{CC}$ Supply voltage                   | 4.5 | 5.5 | V    |
| $V_{IH}$ High-level control input voltage | 2   |     | V    |
| $V_{IL}$ Low-level control input voltage  |     | 0.8 | V    |
| $T_A$ Operating free-air temperature      | -40 | 85  | °C   |

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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**WITH LEVEL SHIFTING**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                |                | TEST CONDITIONS           |                             | MIN                  | TYP† | MAX     | UNIT          |          |
|--------------------------|----------------|---------------------------|-----------------------------|----------------------|------|---------|---------------|----------|
| $V_{IK}$                 |                | $V_{CC} = 4.5\text{ V}$ , | $I_I = -18\text{ mA}$       |                      |      | -1.2    | V             |          |
| $V_{OH}$                 |                | See Figure 2              |                             |                      |      |         |               |          |
| $I_I$                    |                | $V_{CC} = 0\text{ V}$ ,   | $V_I = 5.5\text{ V}$        |                      |      | 10      | $\mu\text{A}$ |          |
|                          |                | $V_{CC} = 5.5\text{ V}$ , | $V_I = 5.5\text{ V or GND}$ |                      |      | $\pm 1$ |               |          |
| $I_{CC}$                 |                | $V_{CC} = 5.5\text{ V}$ , | $I_O = 0$ ,                 |                      |      | 1.5     | mA            |          |
| $\Delta I_{CC}^\ddagger$ | Control inputs | $V_{CC} = 5.5\text{ V}$ , | One input at 3.4 V,         |                      |      | 2.5     | mA            |          |
| $C_i$                    | Control inputs | $V_I = 3\text{ V or 0}$   |                             |                      |      | 4.5     | pF            |          |
| $C_{io(OFF)}$            |                | $V_O = 3\text{ V or 0}$ , | $\overline{OE} = V_{CC}$    |                      |      | 5.5     | pF            |          |
| $r_{on}^\S$              |                | $V_{CC} = 4.5\text{ V}$   | $V_I = 0$                   |                      |      | 5       | 7             | $\Omega$ |
|                          |                |                           |                             | $I_I = 64\text{ mA}$ |      |         | 5             |          |
|                          |                |                           | $V_I = 2.4\text{ V}$ ,      | $I_I = 15\text{ mA}$ |      |         | 35            |          |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

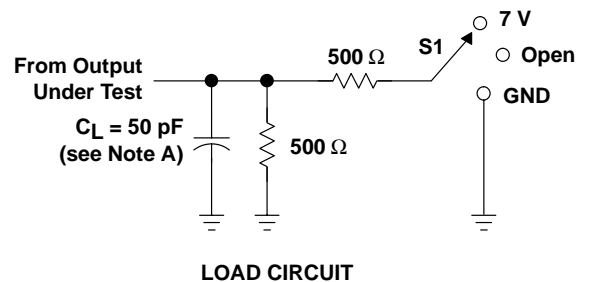
| PARAMETER          | FROM (INPUT)    | TO (OUTPUT) | MIN | MAX  | UNIT |
|--------------------|-----------------|-------------|-----|------|------|
| $t_{pd}^\parallel$ | A or B          | B or A      |     | 0.25 | ns   |
| $t_{en}$           | $\overline{OE}$ | A or B      | 1.5 | 9.8  | ns   |
| $t_{dis}$          | $\overline{OE}$ | A or B      | 1.5 | 8.9  | ns   |

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

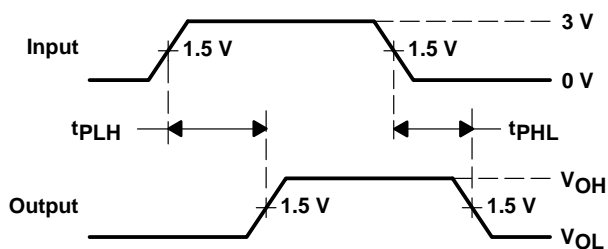
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## PARAMETER MEASUREMENT INFORMATION

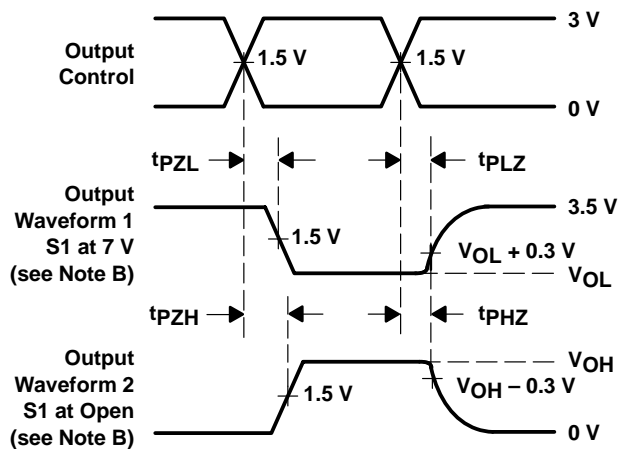


LOAD CIRCUIT



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

| TEST                               | S1   |
|------------------------------------|------|
| t <sub>pd</sub>                    | Open |
| t <sub>PLZ</sub> /t <sub>PZL</sub> | 7 V  |
| t <sub>PHZ</sub> /t <sub>PZH</sub> | Open |



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

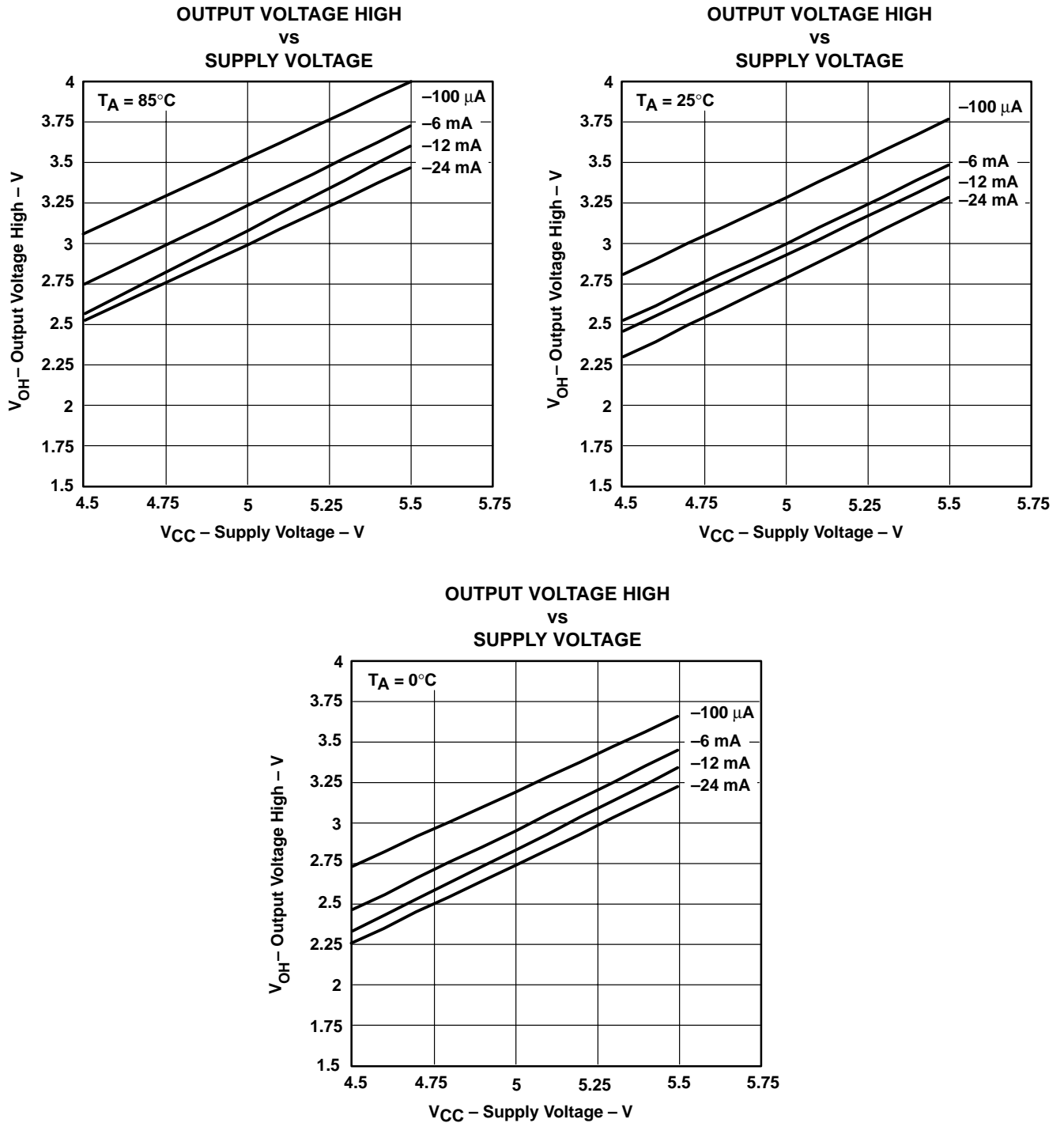


Figure 2.  $V_{OH}$  Values

**PACKAGING INFORMATION**

| Orderable Device  | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74CBTD16210DGGR | ACTIVE                | TSSOP        | DGG             | 48   | 2000        | Pb-Free (RoHS)          | CU NIPDAU        | Level-1-250C-UNLIM           |
| SN74CBTD16210DGVR | ACTIVE                | TVSOP        | DGV             | 48   | 2000        | Pb-Free (RoHS)          | CU NIPDAU        | Level-1-250C-UNLIM           |
| SN74CBTD16210DL   | ACTIVE                | SSOP         | DL              | 48   | 25          | None                    | CU NIPDAU        | Level-1-235C-UNLIM           |
| SN74CBTD16210DLR  | ACTIVE                | SSOP         | DL              | 48   | 1000        | None                    | CU NIPDAU        | Level-1-235C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

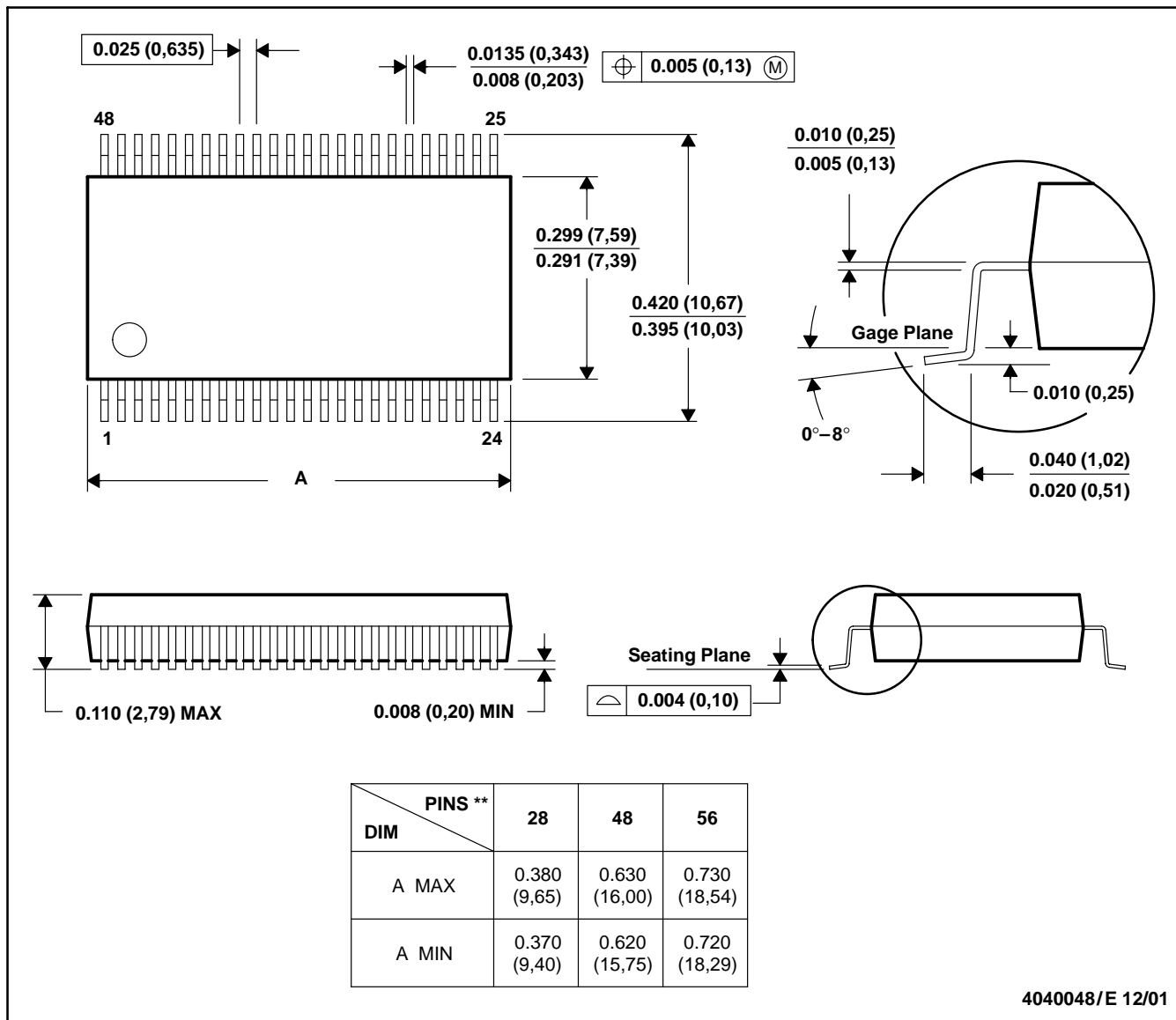


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

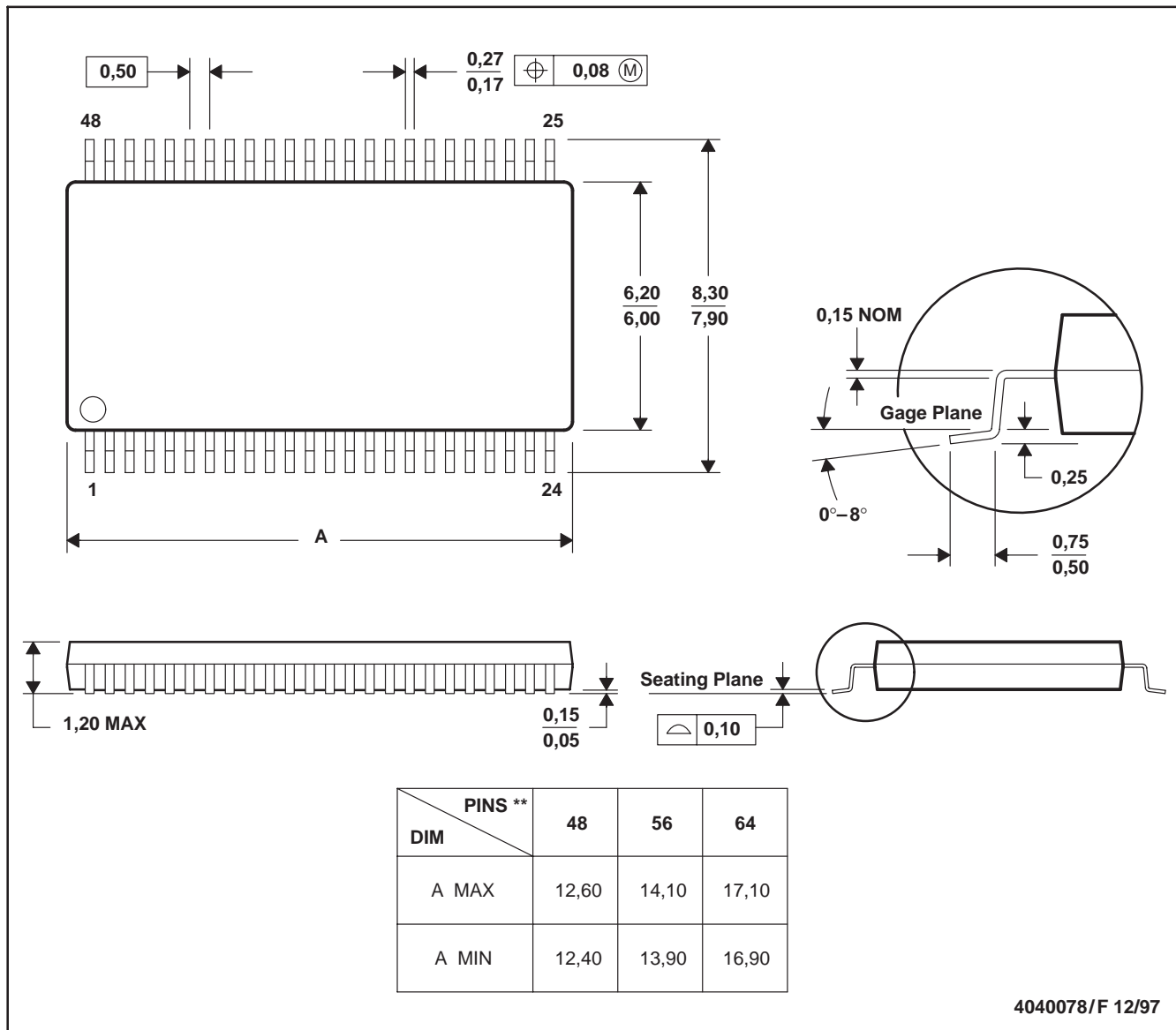


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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