

SN74CBTK16245

16-BIT FET BUS SWITCH

WITH ACTIVE-CLAMP UNDERSHOOT-PROTECTION CIRCUIT

SCDS105D – APRIL 2000 – REVISED NOVEMBER 2001

- Member of the Texas Instruments Widebus™ Family
- Standard '16245-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- I_{off} Supports Partial-Power-Down Mode Operation
- Active-Clamp Undershoot-Protection Circuit on the I/Os Clamps Undershoots up to -2 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description

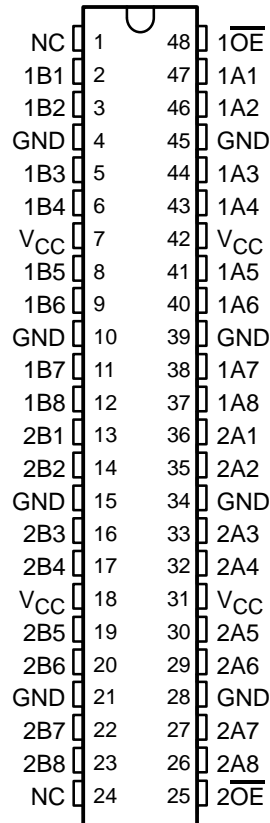
The SN74CBTK16245 device provides 16 bits of high-speed TTL-compatible bus switching in a standard '16245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The A and B ports have an active-clamp undershoot-protection circuit. When there is an undershoot, the active-clamp circuit is enabled, and current from V_{CC} is supplied to clamp the output, preventing the pass transistor from turning on.

The device is organized as two 8-bit low-impedance switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on, and data can flow from the A port to the B port, or vice versa. When \overline{OE} is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBTK16245DL	CBTK16245
		Tape and reel	SN74CBTK16245DLR	
	TSSOP – DGG	Tape and reel	SN74CBTK16245DGGR	CBTK16245
	TVSOP – DGV	Tape and reel	SN74CBTK16245DGVR	CP245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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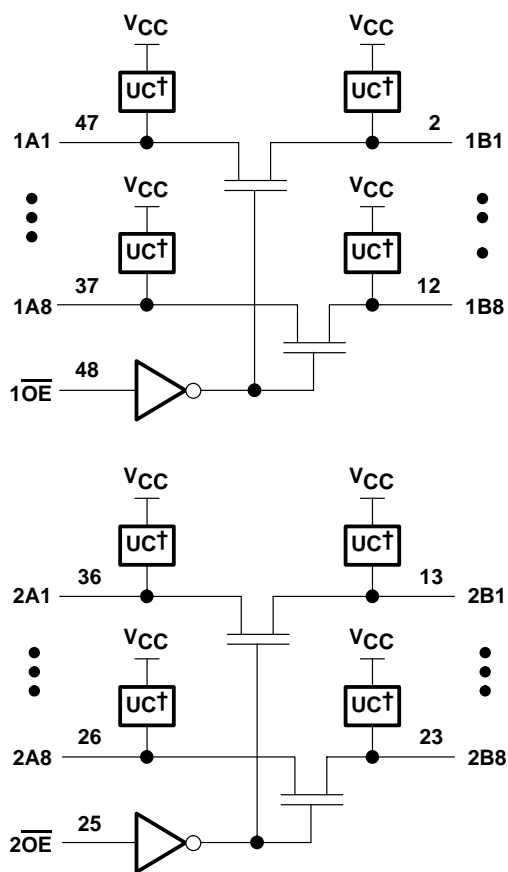
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FUNCTION TABLE
(each 8-bit bus switch)

INPUT OE	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



† Undershoot clamp

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A	0.35		0.25		ns
t _{en}	$\overline{\text{OE}}$	A or B	7.4		1.6	4.9	ns
t _{dis}	$\overline{\text{OE}}$	A or B	7.4		4.2	7.5	ns

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V _{OUTU}	See Figures 1 and 2, and Table 1	2	V _{OH} -0.3		V

‡ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

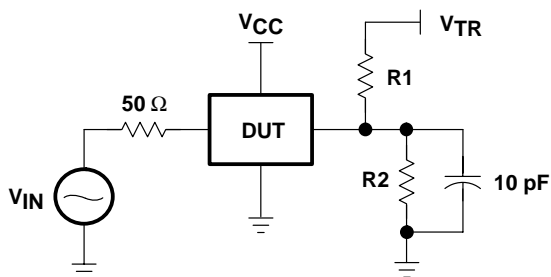


Figure 1. Device Test Setup

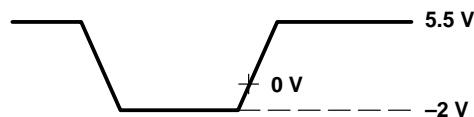


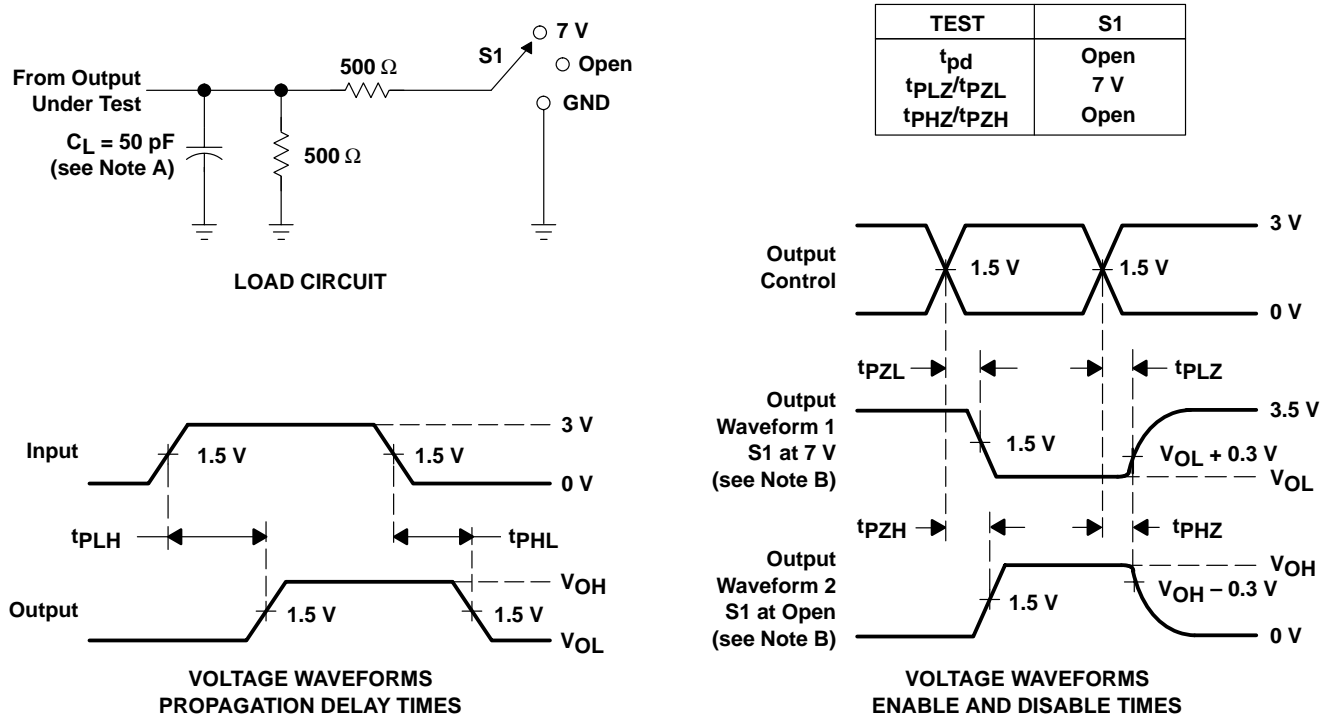
Figure 2. Transient Input Voltage Waveform

Table 1. Device Test Conditions

PARAMETER	VALUE	UNIT
B port under test§	See Figure 1	
V _{IN}	See Figure 2	V
t _w	20	ns
t _r	2	ns
t _f	2	ns
R1 = R2	100	kΩ
V _{TR}	11	V
V _{CC}	5.5	V

§ Other B-port outputs are open.

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74CBTK16245DGGR	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74CBTK16245DGVR	ACTIVE	TVSOP	DGV	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74CBTK16245DL	ACTIVE	SSOP	DL	48	25	None	CU NIPDAU	Level-1-235C-UNLIM
SN74CBTK16245DLR	ACTIVE	SSOP	DL	48	1000	None	CU NIPDAU	Level-1-235C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



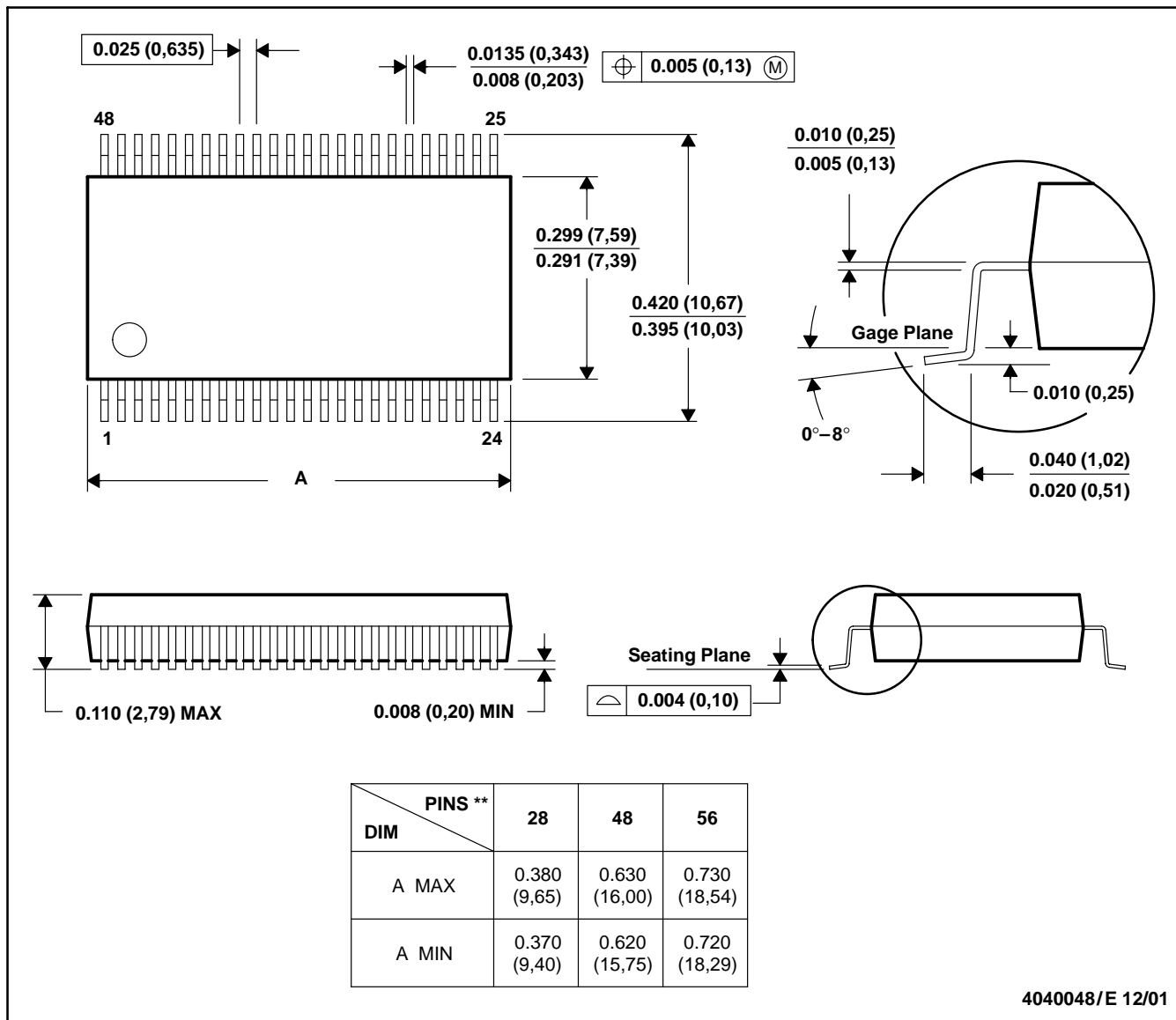
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- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

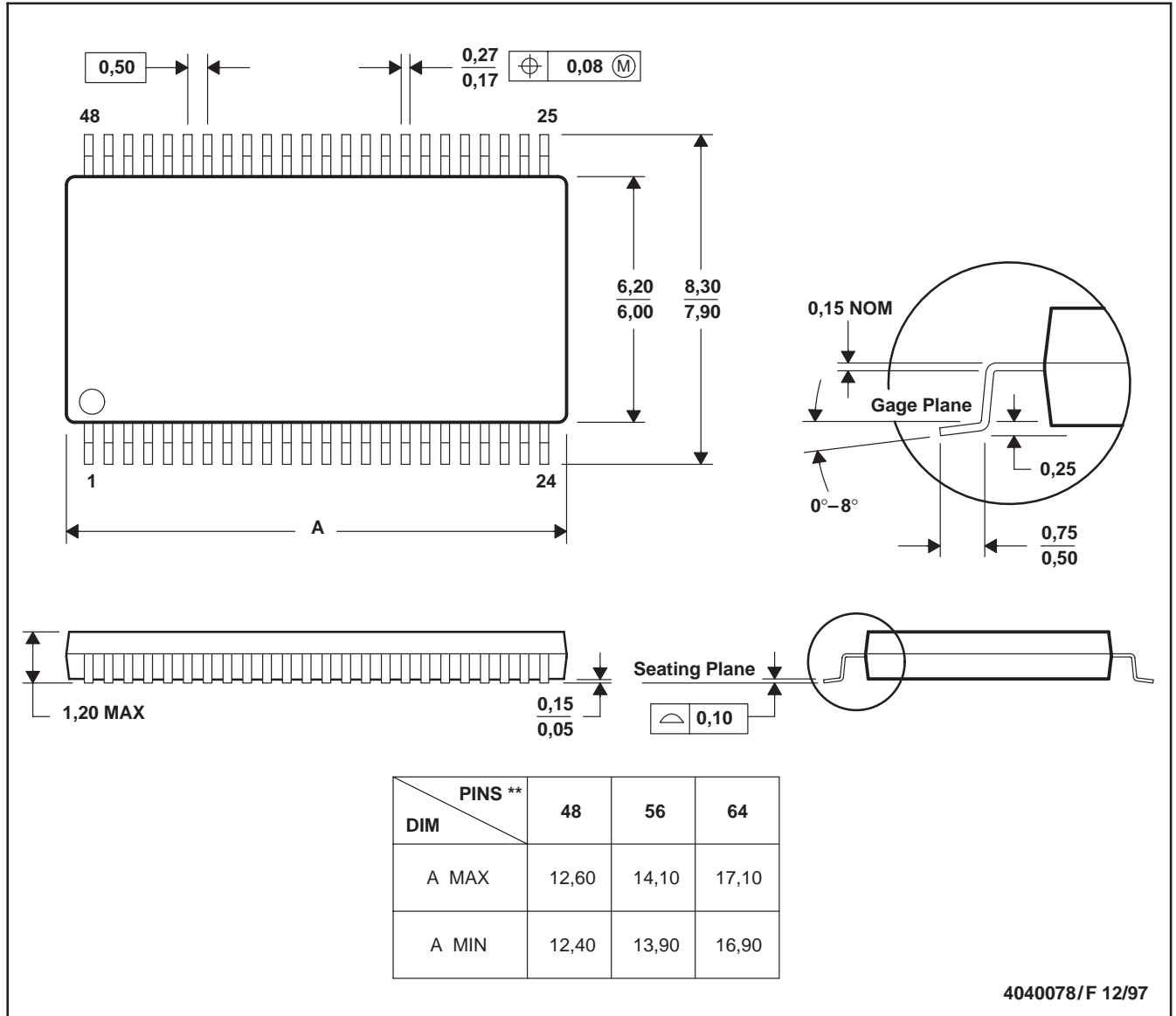


- NOTES: A. All linear dimensions are in inches (millimeters).
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 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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