

# SN74CBTLV16210 LOW-VOLTAGE 20-BIT FET BUS SWITCH

SCDS042E – DECEMBER 1997 – REVISED FEBRUARY 1999

- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

## description

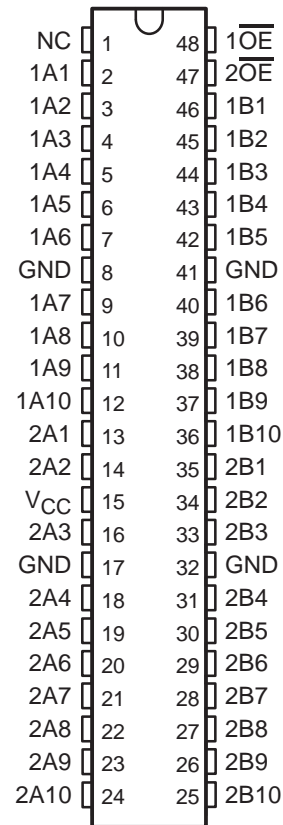
The SN74CBTLV16210 provides 20 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 10-bit bus switches with separate output-enable ( $\overline{OE}$ ) inputs. It can be used as two 10-bit bus switches or one 20-bit bus switch. When  $\overline{OE}$  is low, the associated 10-bit bus switch is on and port A is connected to port B. When  $\overline{OE}$  is high, the switch is open, and the high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV16210 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE  
(each 10-bit bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect



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 **TEXAS  
INSTRUMENTS**

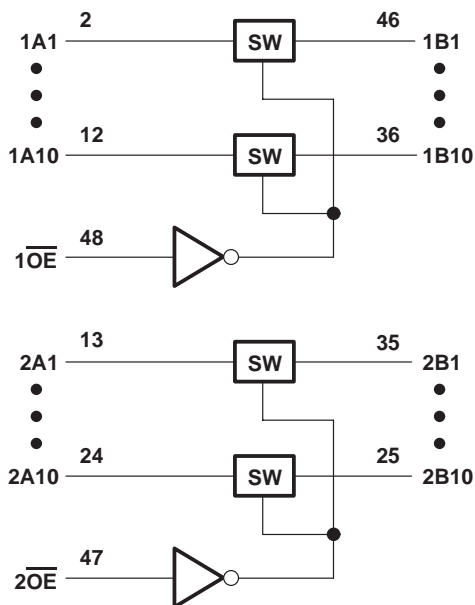
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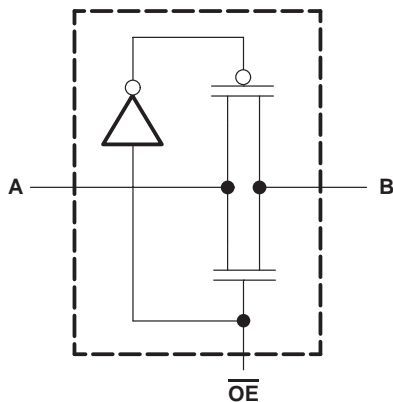
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## logic diagram (positive logic)



## simplified schematic, each FET switch



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 4.6 V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DGG package	89°C/W
DGV package	93°C/W
DL package	94°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.



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### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	3.6	V
V <sub>IH</sub>	High-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	
V <sub>IL</sub>	Low-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 3 V,	I <sub>I</sub> = -18 mA			-1.2	V
I <sub>I</sub>		V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND			±1	μA
I <sub>off</sub>		V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V			10	μA
I <sub>CC</sub>		V <sub>CC</sub> = 3.6 V,	I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND			10	μA
ΔI <sub>CC</sub> ‡	Control inputs	V <sub>CC</sub> = 3.6 V,	One input at 3 V, Other inputs at V <sub>CC</sub> or GND			300	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3 V or 0				4.5	pF
C <sub>io(OFF)</sub>		V <sub>O</sub> = 3 V or 0,	$\overline{\text{OE}} = V_{CC}$			6.5	pF
r <sub>on</sub> §	V <sub>CC</sub> = 2.3 V, TYP at V <sub>CC</sub> = 2.5 V	V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA		5	8	Ω
			I <sub>I</sub> = 24 mA		5	8	
		V <sub>I</sub> = 1.7 V,	I <sub>I</sub> = 15 mA		27	40	
	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA		5	7	
			I <sub>I</sub> = 24 mA		5	7	
		V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA		10	15	

† All typical values are at V<sub>CC</sub> = 3.3 V (unless otherwise noted), T<sub>A</sub> = 25°C.

‡ This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub> ¶	A or B	B or A	0.15		0.25		ns
t <sub>en</sub>	$\overline{\text{OE}}$	A or B	1	6.8	1	6	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	A or B	1	7.3	1	7.4	ns

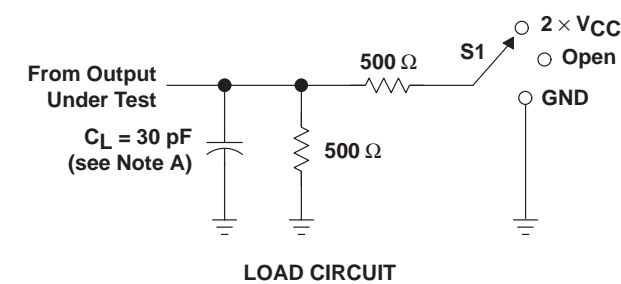
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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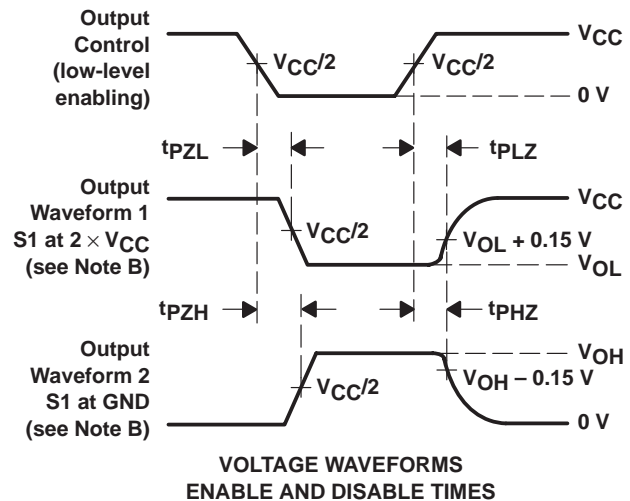
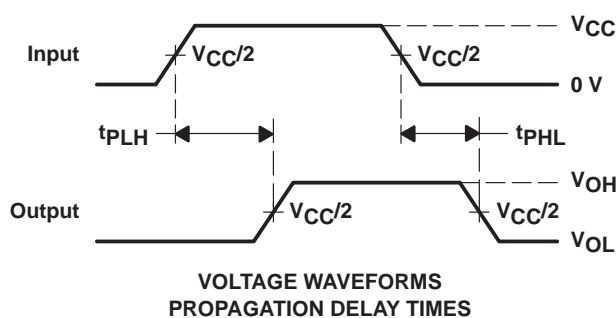
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## PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

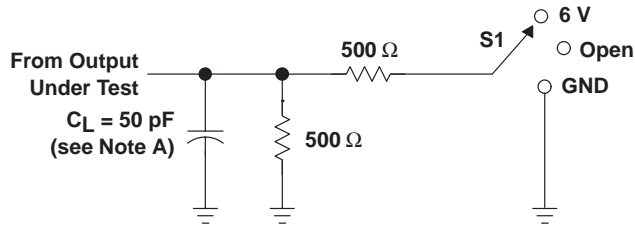


- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

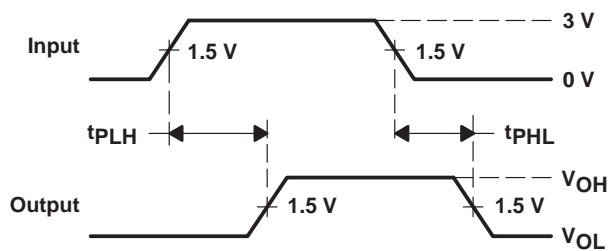
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

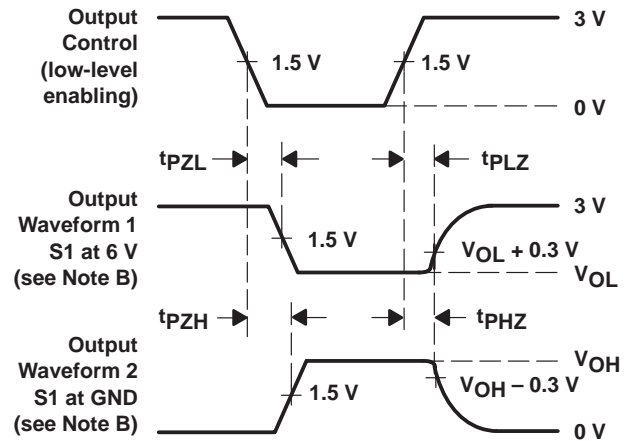


LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

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