

- Member of the Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22 – 2000-V Human-Body Model (A114-A)

## description/ordering information

The SN74CBTLV16211C provides 24 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 12-bit bus switches with separate output-enable ( $\overline{OE}$ ) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When  $\overline{OE}$  is low, the associated 12-bit bus switch is on, and port A is connected to port B. When  $\overline{OE}$  is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	VFBGA – GRD	Tape and reel	74CBTLV16211CGRDR	CN211
	VFBGA – ZRD (Pb-free)	Tape and reel	74CBTLV16211CZRDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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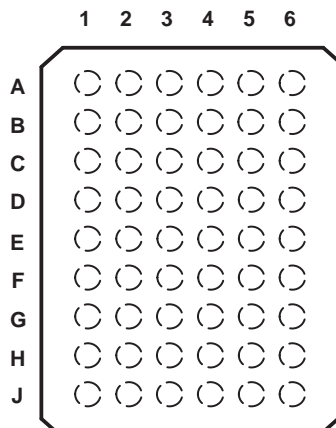
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# SN74CBTLV16211C LOW-VOLTAGE 24-BIT FET BUS SWITCH

SCDS204 – JULY 2005

GRD OR ZRD PACKAGE  
(TOP VIEW)



## terminal assignments

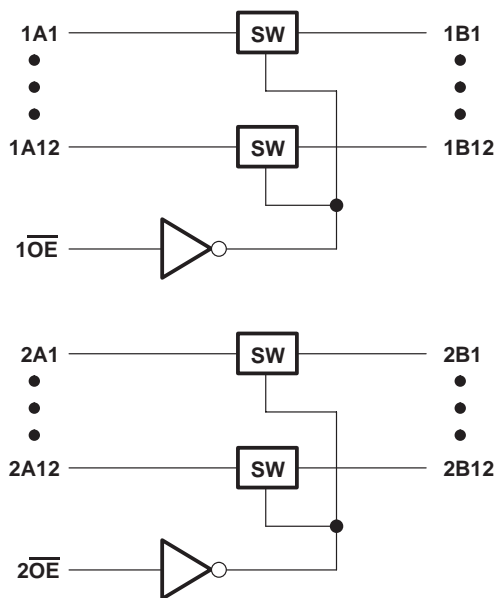
	1	2	3	4	5	6
A	1A2	1A1	NC	$\overline{2OE}$	1B1	1B2
B	1A4	1A3	1A7	$\overline{1OE}$	1B3	1B4
C	1A6	1A5	GND	1B7	1B5	1B6
D	1A10	1A9	1A8	1B8	1B9	1B10
E	1A12	1A11	2A1	2B1	1B11	1B12
F	2A4	2A3	2A2	2B2	2B3	2B4
G	2A6	2A5	V <sub>CC</sub>	GND	2B5	2B6
H	2A8	2A7	2A9	2B9	2B7	2B8
J	2A12	2A11	2A10	2B10	2B11	2B12

NC – No internal connection

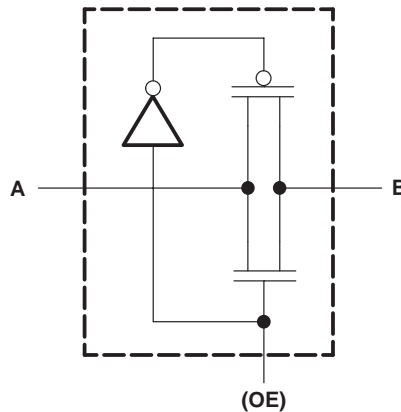
FUNCTION TABLE  
(each 12-bit bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

## logic diagram (positive logic)



**simplified schematic, each FET switch**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 4.6 V
Continuous channel current .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): GRD/ZRD package .....	36°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.3	3.6	V
$V_{IH}$	High-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	
$V_{IL}$	Low-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0.8	
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74CBTLV16211C

## LOW-VOLTAGE 24-BIT FET BUS SWITCH

SCDS204 – JULY 2005

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 3\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$I_I$		$V_{CC} = 3.6\text{ V}$ ,	$V_I = V_{CC}$ or GND			$\pm 1$	$\mu\text{A}$
$I_{off}$		$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to $3.6\text{ V}$			10	$\mu\text{A}$
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ ,	$I_O = 0$ , $V_I = V_{CC}$ or GND			10	$\mu\text{A}$
$\Delta I_{CC}^\ddagger$	Control inputs	$V_{CC} = 3.6\text{ V}$ ,	One input at $3\text{ V}$ , Other inputs at $V_{CC}$ or GND			300	$\mu\text{A}$
$C_i$	Control inputs	$V_I = 3.3\text{ V}$ or $0$				4.5	pF
$C_{io(OFF)}$		$V_O = 3.3\text{ V}$ or $0$ ,	$\overline{OE} = V_{CC}$			6.5	pF
$r_{on}^\S$	$V_{CC} = 2.3\text{ V}$ , TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	8	$\Omega$	
			$I_I = 24\text{ mA}$	5	8		
		$V_I = 1.7\text{ V}$ ,	$I_I = 15\text{ mA}$	27	40		
	$V_{CC} = 3\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	7		
			$I_I = 24\text{ mA}$	5	7		
		$V_I = 2.4\text{ V}$ ,	$I_I = 15\text{ mA}$	10	15		

† All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

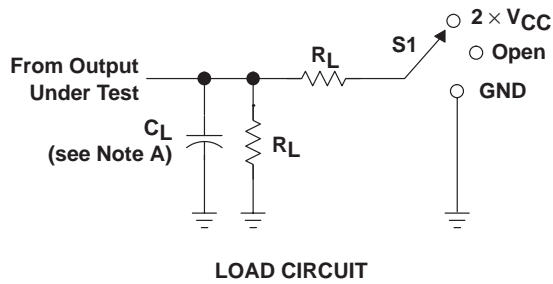
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^\parallel$	A or B	B or A	0.15		0.25		ns
$t_{en}$	$\overline{OE}$	A or B	0.5	6	0.5	5.2	ns
$t_{dis}$	$\overline{OE}$	A or B	0.5	6.2	0.5	6.7	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

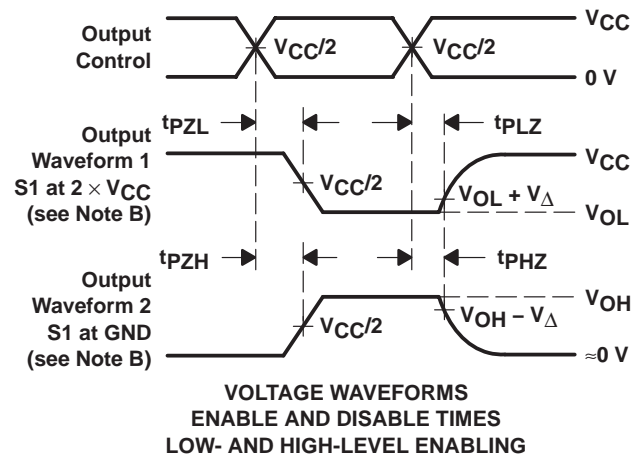
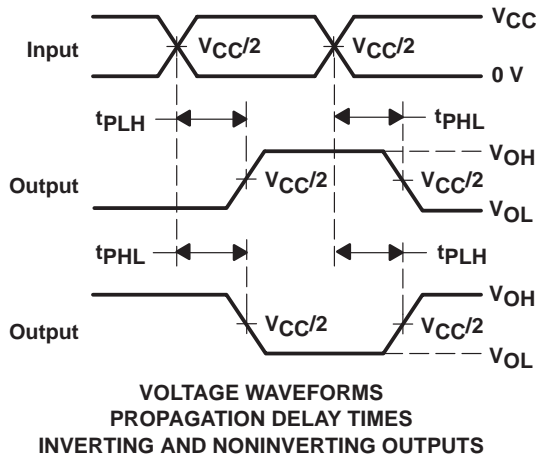
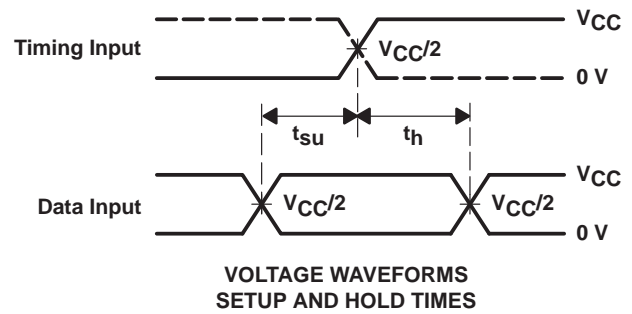
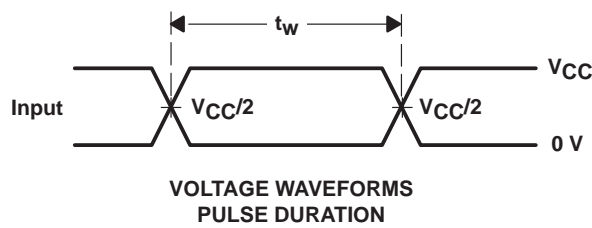


PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
2.5 V $\pm$ 0.2 V	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	50 pF	500 $\Omega$	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2$  ns,  $t_f \leq 2$  ns.  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74CBTLV16211CGRDR	ACTIVE	BGA MI CROSTA R JUNI OR	GRD	54	1000	TBD	SNPB	Level-1-240C-UNLIM
74CBTLV16211CZRDR	ACTIVE	BGA MI CROSTA R JUNI OR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CBTLV16211CGRDR	BGA MICROSTAR JUNIOR	GRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1
74CBTLV16211CZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

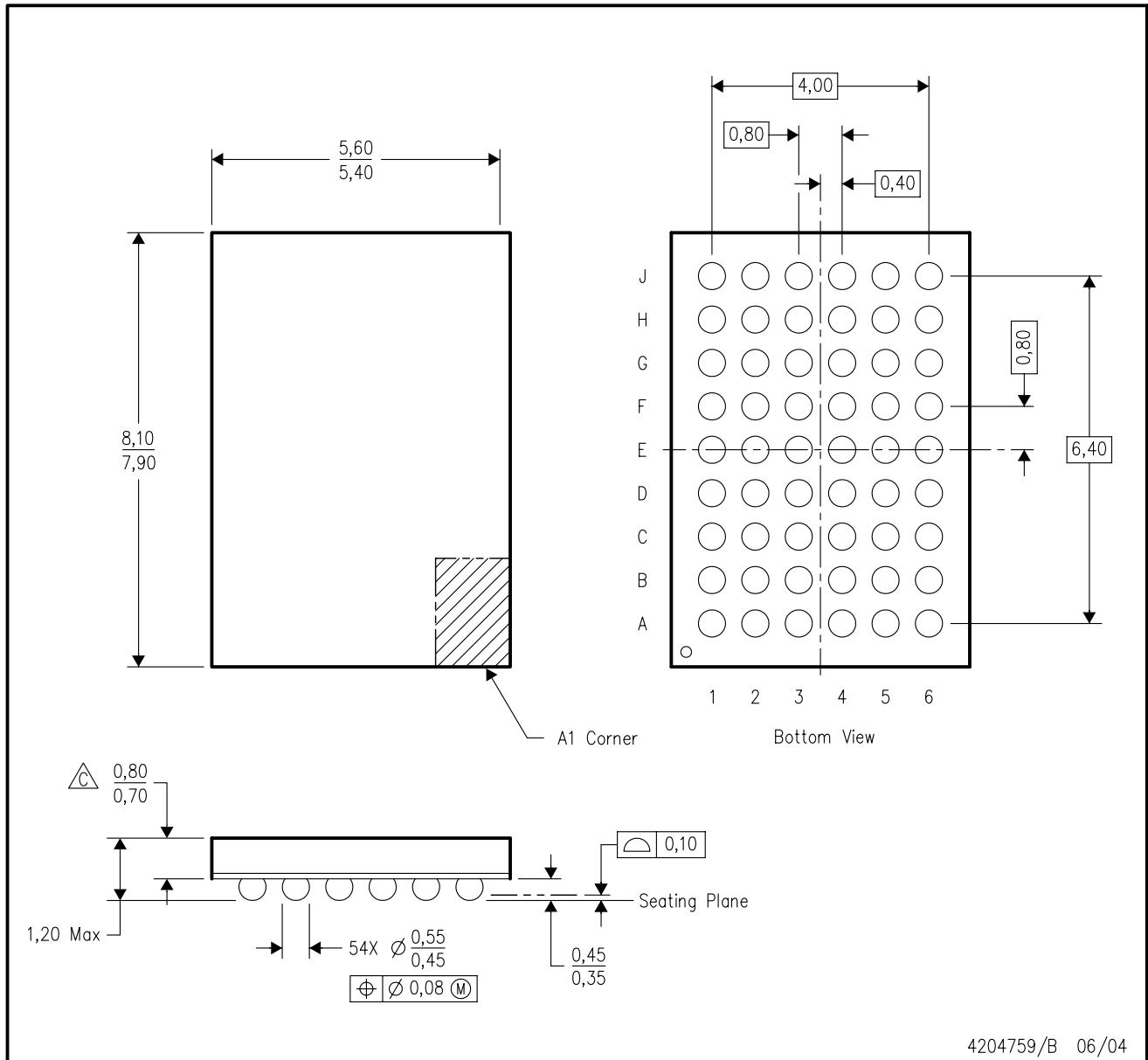


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CBTLV16211CGRDR	BGA MICROSTAR JUNIOR	GRD	54	1000	333.2	345.9	28.6
74CBTLV16211CZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	333.2	345.9	28.6

GRD (R-PBGA-N54)

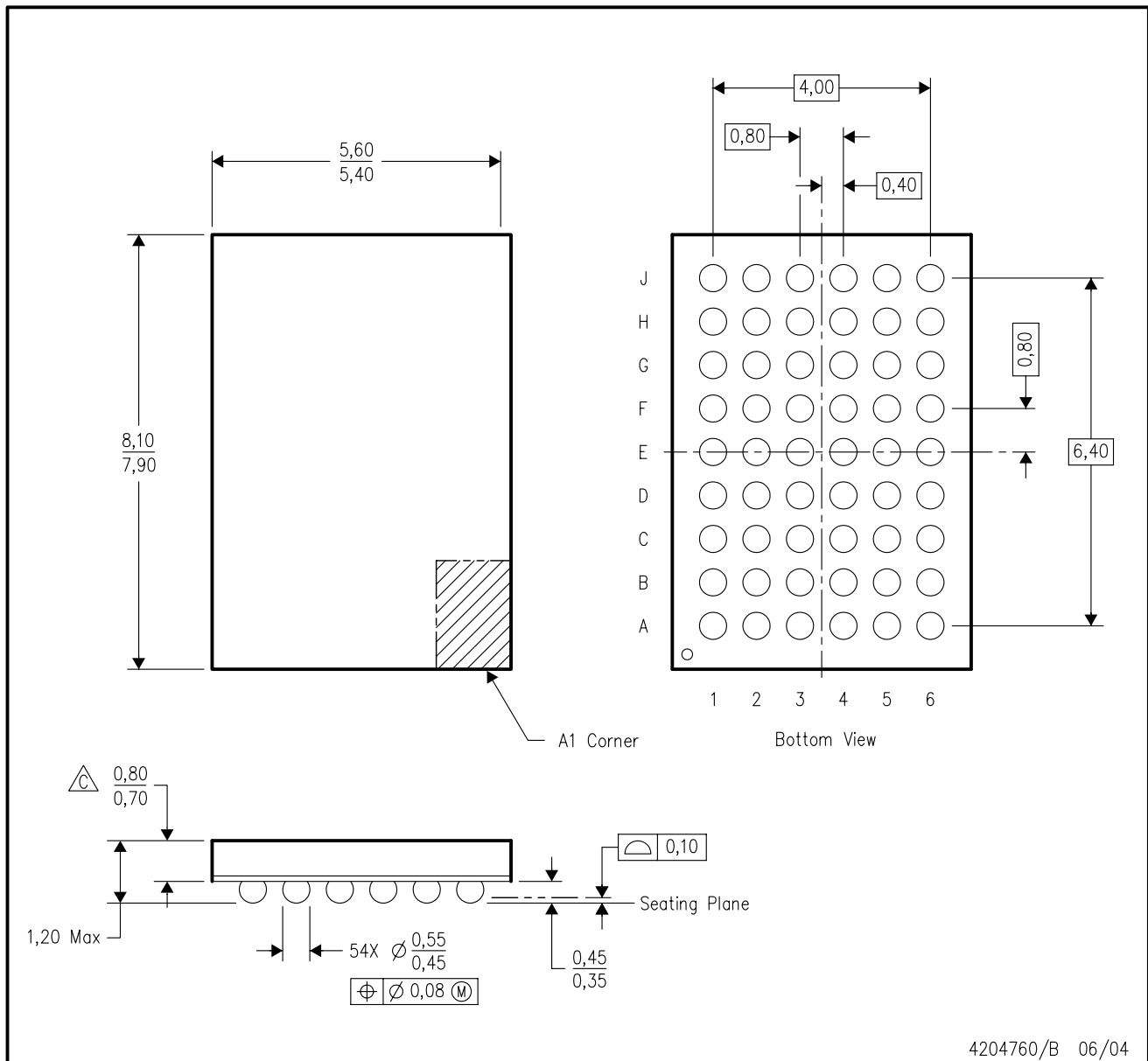
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MO-205 variation DD.
  - D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

ZRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - $\triangle$  Falls within JEDEC MO-205 variation DD.
  - D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

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