

SN74CBTLV16211 LOW-VOLTAGE 24-BIT FET BUS SWITCH

SCDS043E – DECEMBER 1997 – REVISED APRIL 1999

- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

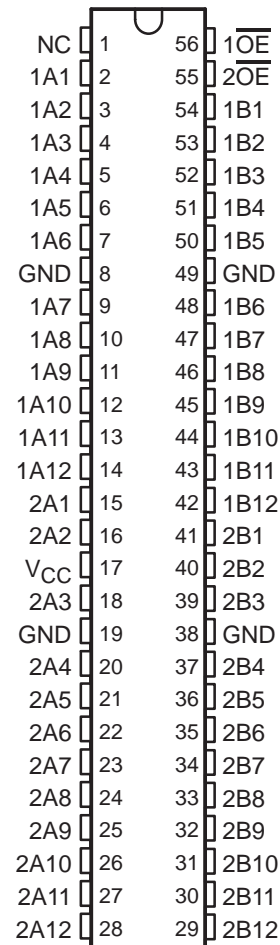
The SN74CBTLV16211 provides 24 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 12-bit bus switches with separate output-enable (\overline{OE}) inputs. It can be used as two 12-bit bus switches or one 24-bit bus switch. When \overline{OE} is low, the associated 12-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open, and the high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV16211 is characterized for operation from -40°C to 85°C .

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each 12-bit bus switch)

INPUT \overline{OE}	FUNCTION
L	A port = B port
H	Disconnect



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	V
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0.7	V
		V _{CC} = 2.7 V to 3.6 V	0.8	
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 3 V,	I _I = -18 mA			-1.2	V
I _I		V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±1	μA
I _{off}		V _{CC} = 0,	V _I or V _O = 0 to 3.6 V			10	μA
I _{CC}		V _{CC} = 3.6 V,	I _O = 0, V _I = V _{CC} or GND			10	μA
ΔI _{CC} ‡	Control inputs	V _{CC} = 3.6 V,	One input at 3 V, Other inputs at V _{CC} or GND			300	μA
C _i	Control inputs	V _I = 3.3 V or 0				4.5	pF
C _{io(OFF)}		V _O = 3.3 V or 0,	$\overline{\text{OE}} = V_{CC}$			6.5	pF
r _{on} §	V _{CC} = 2.3 V, TYP at V _{CC} = 2.5 V	V _I = 0	I _I = 64 mA		5	8	Ω
			I _I = 24 mA		5	8	
	V _I = 1.7 V,	I _I = 15 mA		27	40		
		V _{CC} = 3 V	V _I = 0	I _I = 64 mA		5	
	I _I = 24 mA				5	7	
	V _I = 2.4 V,	I _I = 15 mA		10	15		

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A	0.15		0.25		ns
t _{en}	$\overline{\text{OE}}$	A or B	1	7	1	6.2	ns
t _{dis}	$\overline{\text{OE}}$	A or B	1	7.2	1	7.7	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

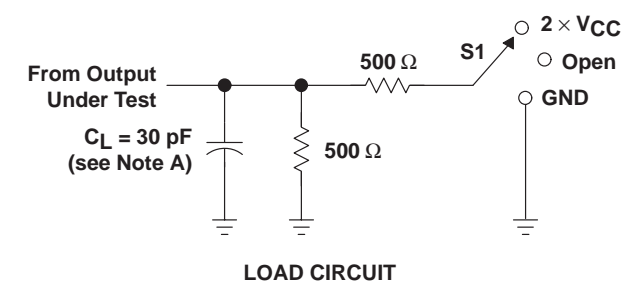


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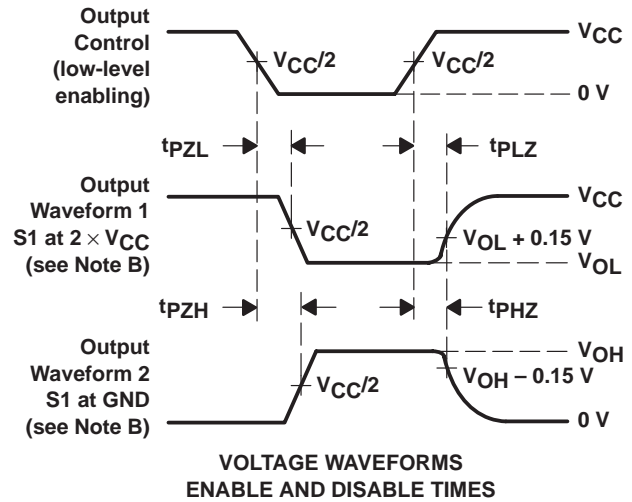
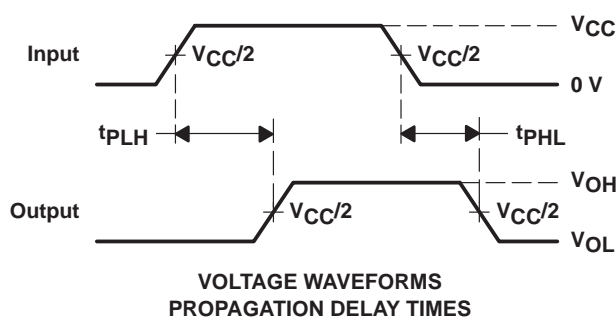
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PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 \times V_{CC}
t_{PHZ}/t_{PZH}	GND

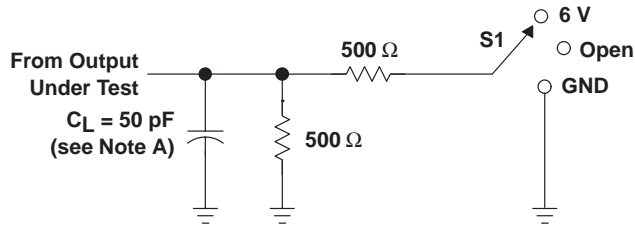


- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

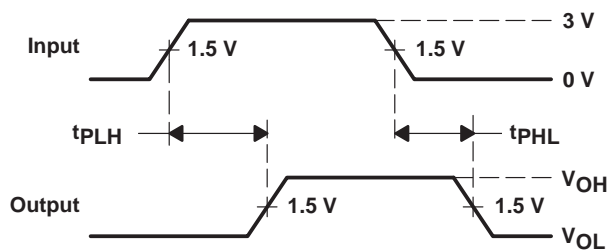
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

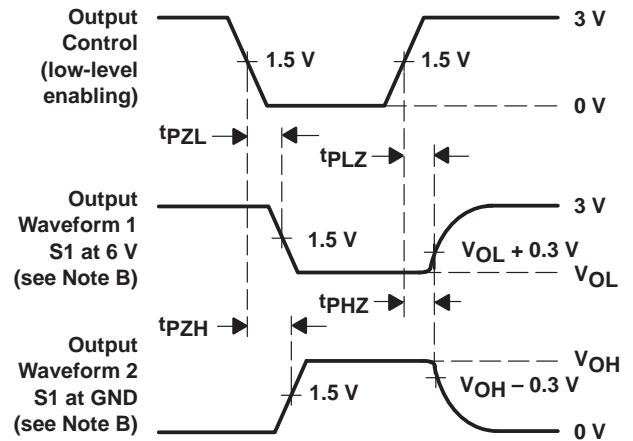


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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