

# SN74CBTLV16292

## LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS055G – MARCH 1998 – REVISED APRIL 1999

- 4- $\Omega$  Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Make-Before-Break Feature
- Internal 500- $\Omega$  Pulldown Resistors to Ground
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

### description

The SN74CBTLV16292 is a 12-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

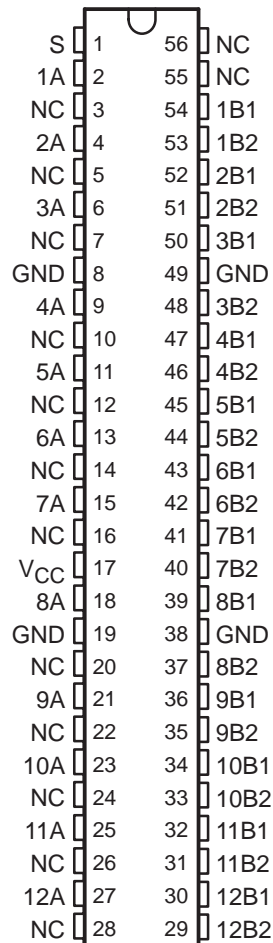
When the select (S) input is low, port A is connected to port B1 and  $R_{INT}$  is connected to port B2. When S is high, port A is connected to port B2 and  $R_{INT}$  is connected to port B1.

The SN74CBTLV16292 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port $R_{INT}$ = B2 port
H	A port = B2 port $R_{INT}$ = B1 port

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



NC – No internal connection



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**TEXAS  
INSTRUMENTS**

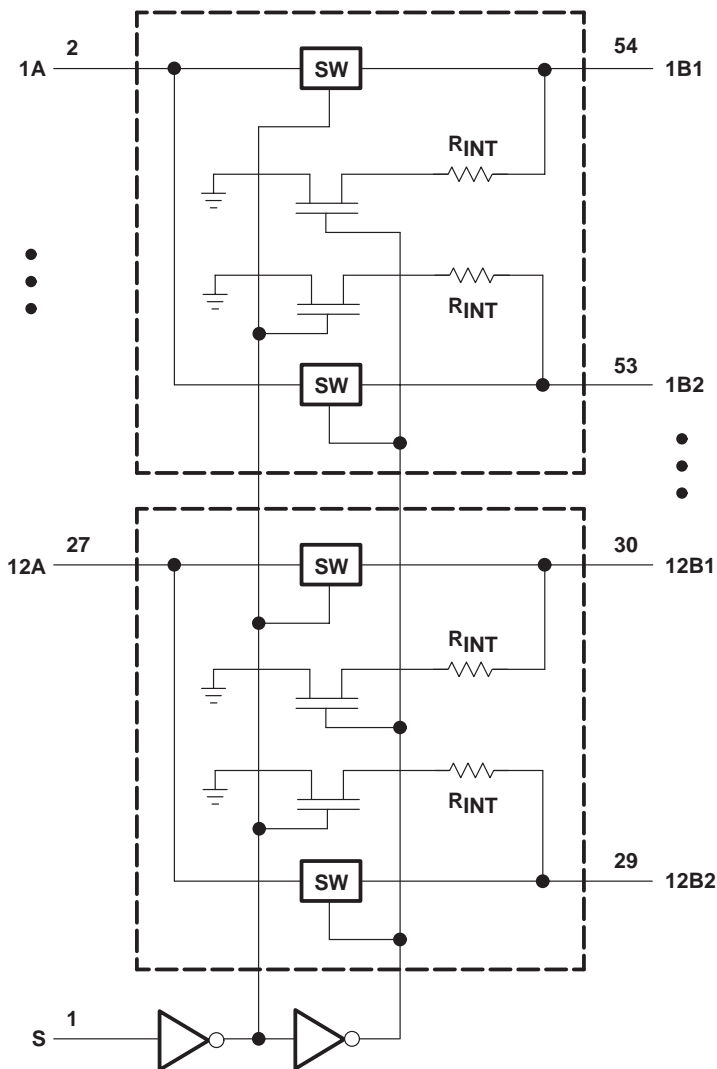
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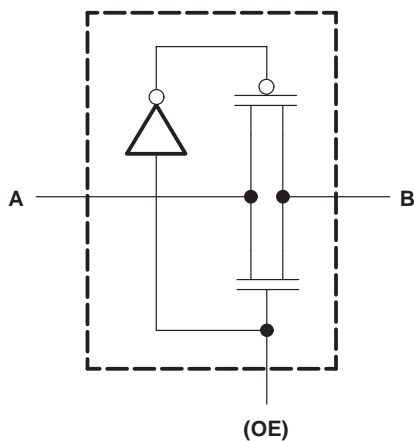
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## logic diagram (positive logic)



## simplified schematic, each FET switch



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 4.6 V	
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 4.6 V	
Continuous channel current .....	128 mA	
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA	
Package thermal impedance, $\theta_{JA}$ (see Note 2):	DGG package .....	81°C/W
	DGV package .....	86°C/W
	DL package .....	74°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.3	3.6	V
$V_{IH}$	High-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	
$V_{IL}$	Low-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0.8	
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
$V_{IK}$		$V_{CC} = 3 \text{ V}$ ,	$I_I = -18 \text{ mA}$			–1.2	V
$I_I$		$V_{CC} = 3.6 \text{ V}$ ,	$V_I = V_{CC}$ or GND			±1	μA
$I_{off}$		$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to 3.6 V			10	μA
$I_{CC}$		$V_{CC} = 3.6 \text{ V}$ ,	$I_O = 0$ , $V_I = V_{CC}$ or GND			10	μA
$\Delta I_{CC}$ §	Control input	$V_{CC} = 3.6 \text{ V}$ ,	One input at 3 V, Other inputs at $V_{CC}$ or GND			300	μA
$C_i$	Control input	$V_I = 3.3 \text{ V}$ or 0				3.5	pF
$C_{io}$	A or B port	$V_O = 3.3 \text{ V}$ or 0				22.5	pF
$r_{on}$ ¶	$V_{CC} = 2.3 \text{ V}$ , TYP at $V_{CC} = 2.5 \text{ V}$	$V_I = 0$	$I_I = 64 \text{ mA}$	5	8	Ω	
			$I_I = 24 \text{ mA}$	5	8		
		$V_I = 1.7 \text{ V}$ ,	$I_I = 15 \text{ mA}$	11	40		
	$V_{CC} = 3 \text{ V}$	$V_I = 0$	$I_I = 64 \text{ mA}$	3	7		
			$I_I = 24 \text{ mA}$	3	7		
		$V_I = 2.4 \text{ V}$ ,	$I_I = 15 \text{ mA}$	7	15		

‡ All typical values are at  $V_{CC} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

§ This is the increase in supply current for each input that is at the specified voltage level rather than  $V_{CC}$  or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub> <sup>†</sup>	A or B	B or A	0.15		0.15		ns
t <sub>pd</sub> <sup>‡</sup>	S	A	2.5	7.1	2.5	6.7	ns
t <sub>en</sub>	S	B	1	5.6	1	5	ns
t <sub>dis</sub>	S	B	1	5	1	4.5	ns

<sup>†</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

<sup>‡</sup> This propagation delay was measured by observing the change of voltage on the A output introduced by static levels equal to 3-V or 0 for 3.3 V ± 0.3 V or V<sub>CC</sub> or 0 for 2.5 V ± 0.2 V on B1 and B2 to achieve the desired transition.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	DESCRIPTION	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	
t <sub>mhb</sub> <sup>§</sup>	Make-before-break time	0	2	0	2	ns

<sup>§</sup> The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.

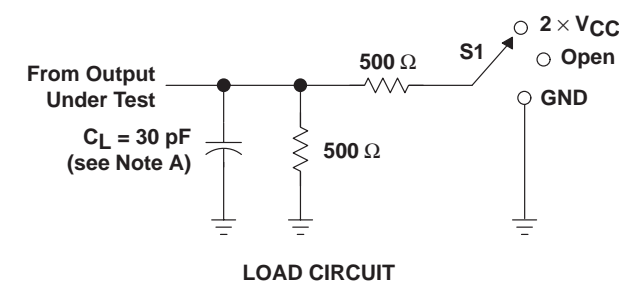


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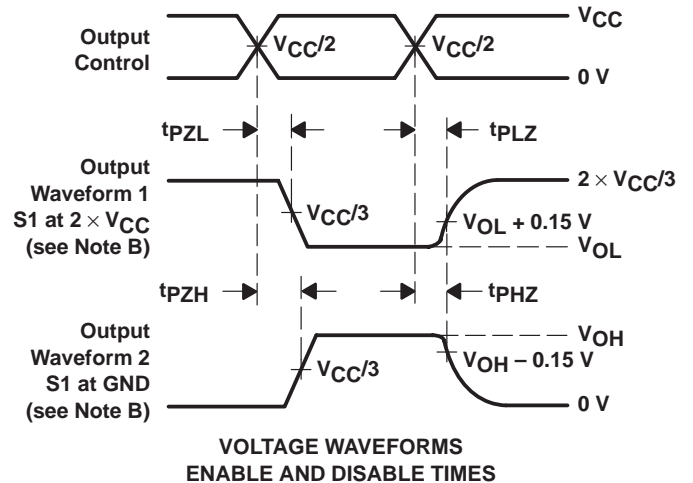
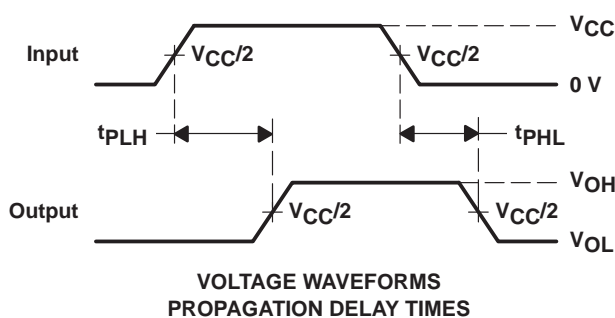
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**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

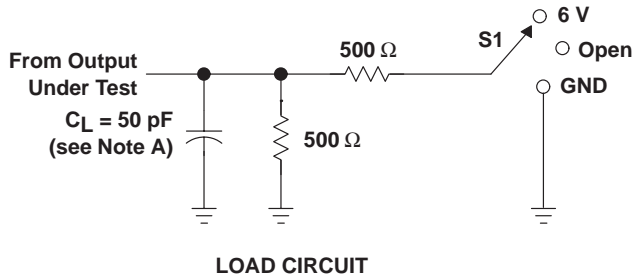
**Figure 1. Load Circuit and Voltage Waveforms**

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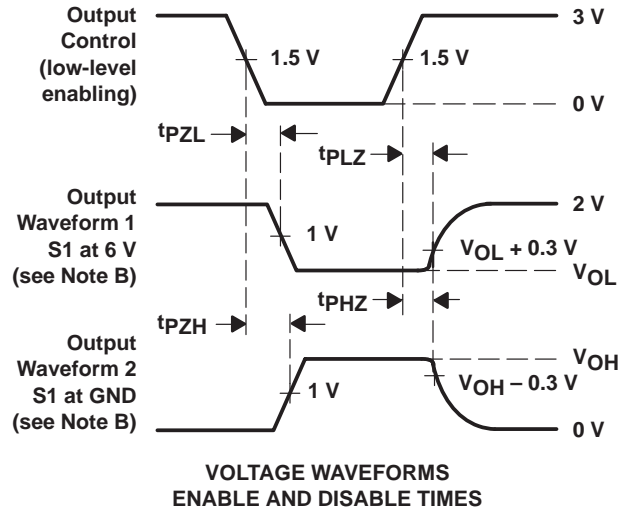
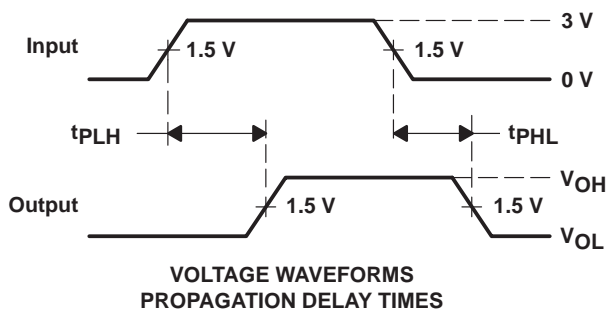
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**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 2. Load Circuit and Voltage Waveforms**

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