

SN74CBTLV3126 LOW-VOLTAGE QUADRUPLE FET BUS SWITCH

SCDS038D – DECEMBER 1997 – REVISED JULY 1999

- Standard '126-Type Pinout
- 5- Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Latch-up Performance Exceeds 100 mA per JESD 78, Class II
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DBQ), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

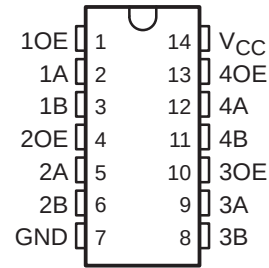
description

The SN74CBTLV3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low.

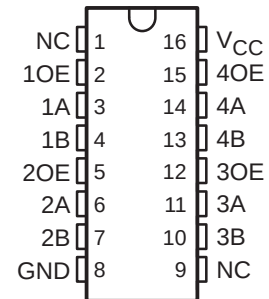
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV3126 is characterized for operation from -40°C to 85°C .

D, DGV, OR PW PACKAGE
(TOP VIEW)



DBQ PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each bus switch)

INPUT OE	FUNCTION
L	Disconnect
H	A port = B port



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

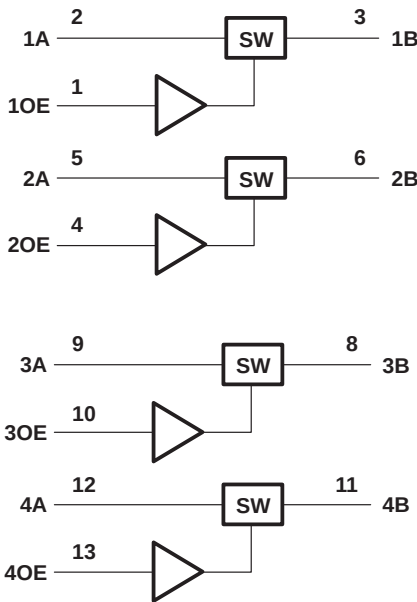
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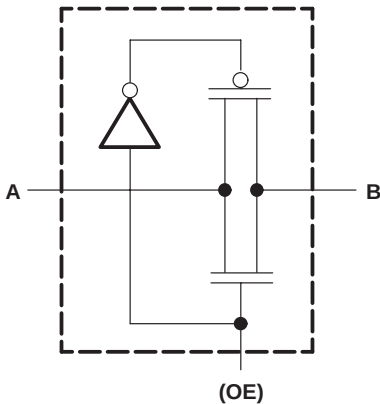
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logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	127°C/W
DBQ package	139°C/W
DGV package	182°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	V
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0.7	V
		V _{CC} = 2.7 V to 3.6 V	0.8	
T _A	Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V _{IK}	V _{CC} = 3 V, I _I = –18 mA			–1.2	V
I _I	V _{CC} = 3.6 V, V _I = V _{CC} or GND			±1	μA
I _{off}	V _{CC} = 0, V _I or V _O = 0 to 4.5 V			10	μA
I _{CC}	V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND			10	μA
ΔI _{CC} [‡]	Control inputs V _{CC} = 3.6 V, One input at 3 V, Other inputs at V _{CC} or GND			300	μA
C _i	Control inputs V _I = 3 V or 0			2.5	pF
C _{io} (OFF)	V _O = 3 V or 0, OE = V _{CC}			7	pF
r _{on} [§]	V _{CC} = 2.3 V, TYP at V _{CC} = 2.5 V	V _I = 0	I _I = 64 mA	5	Ω
			I _I = 24 mA	5	
		V _I = 1.7 V	I _I = 15 mA	27	
	V _{CC} = 3 V	V _I = 0	I _I = 64 mA	5	
			I _I = 24 mA	5	
		V _I = 2.4 V	I _I = 15 mA	10	

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} [¶]	A or B	B or A	0.35		0.25		ns
t _{en}	OE	A or B	1.6	4.5	1.9	4.2	ns
t _{dis}	OE	A or B	1.3	4.7	1	4.8	ns

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



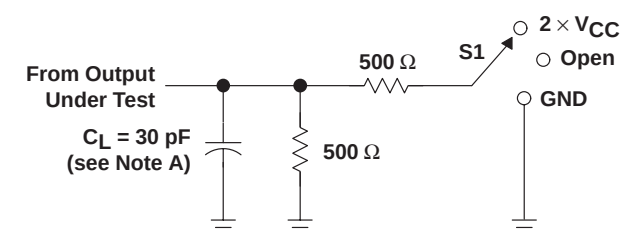
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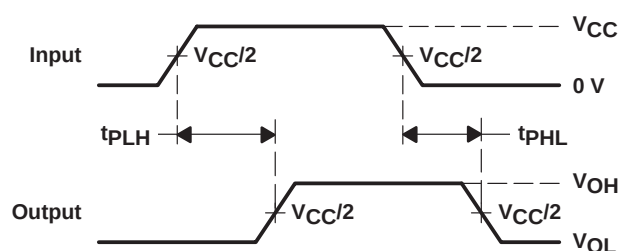
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

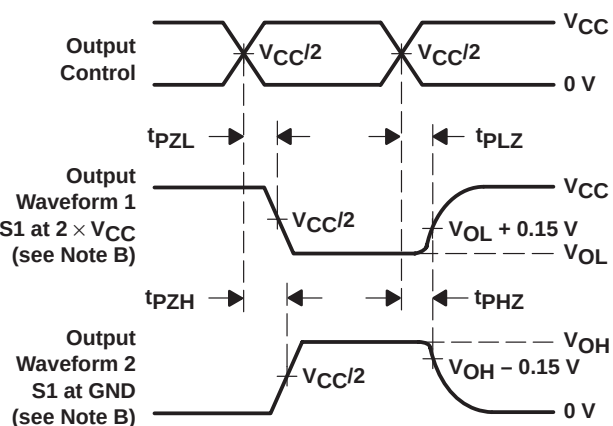


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



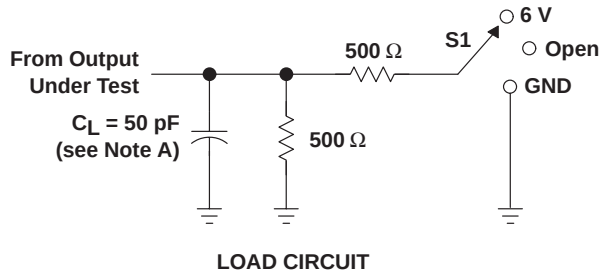
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

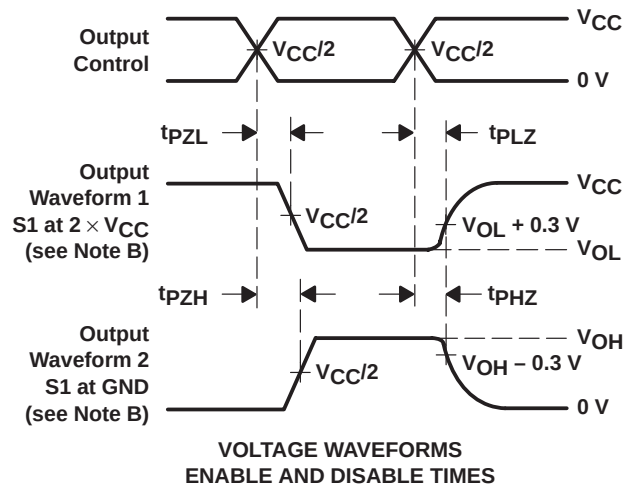
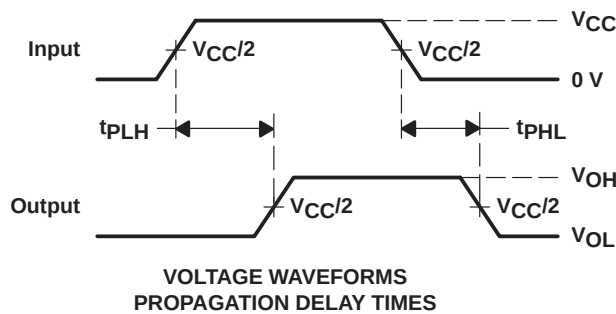
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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